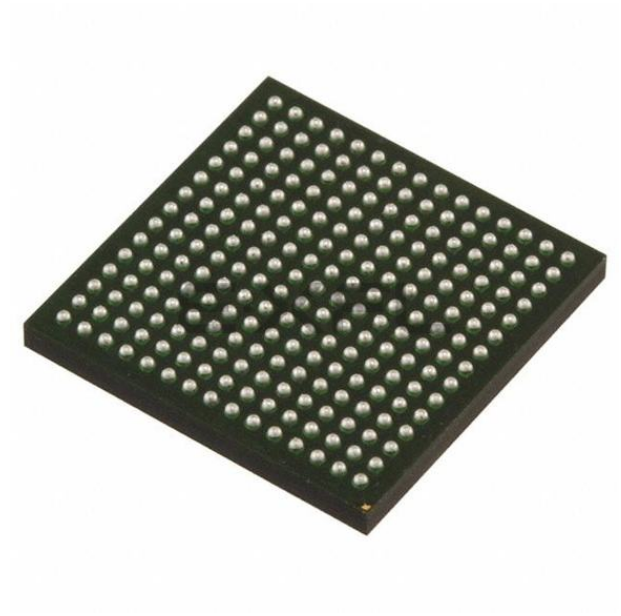
AMD Xilinx - XC7S25-L1CSGA225I Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1825
Number of Logic Elements/Cells	23360
Total RAM Bits	1658880
Number of I/O	150
Number of Gates	-
Voltage - Supply	0.92V ~ 0.98V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	225-LFBGA, CSPBGA
Supplier Device Package	225-CSGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7s25-l1csga225i

Table 3: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Min	Typ[1]	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost).	0.75	–	–	V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost).	1.5	–	–	V
I_{REF}	V_{REF} leakage current per pin.	–	–	15	µA
I_L	Input or output leakage current per pin (sample-tested).	–	–	15	µA
C_{IN}[2]	Die input capacitance at the pad.	–	–	8	pF
I_{RPU}	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 3.3V.	90	–	330	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 2.5V.	68	–	250	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 1.8V.	34	–	220	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 1.5V.	23	–	150	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 1.2V.	12	–	120	µA
I_{RPD}	Pad pull-down (when selected) at V_{IN} = 3.3V.	68	–	330	µA
I_{CCADC}	Analog supply current, analog circuits in powered up state.	–	–	25	mA
I_{BATT}[3]	Battery supply current.	–	–	150	nA
R_{IN_TERM}[4]	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 (UNTUNED_SPLIT_40).	28	40	55	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 (UNTUNED_SPLIT_50).	35	50	65	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 (UNTUNED_SPLIT_60).	44	60	83	Ω
n	Temperature diode ideality factor.	–	1.010	–	–
r	Temperature diode series resistance.	–	2	–	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. This measurement represents the die capacitance at the pad, not including the package.
3. Maximum value specified for worst case process at 25°C.
4. Termination resistance to a V_{CCO}/2 level.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 8: **SelectIO DC Input and Output Levels**(1)(2)(3)

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
HSTL_I	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8.00	–8.00
HSTL_I_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8.00	–8.00
HSTL_II	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	16.00	–16.00
HSTL_II_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	16.00	–16.00
HSUL_12	–0.300	V_{REF} – 0.130	V_{REF} + 0.130	V_{CCO} + 0.300	20% V_{CCO}	80% V_{CCO}	0.10	–0.10
LVCMOS12	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVCMOS15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	25% V_{CCO}	75% V_{CCO}	Note 5	Note 5
LVCMOS18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 6	Note 6
LVCMOS25	–0.300	0.7	1.700	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 5	Note 5
LVCMOS33	–0.300	0.8	2.000	3.450	0.400	V_{CCO} – 0.400	Note 5	Note 5
LVTTL	–0.300	0.8	2.000	3.450	0.400	2.400	Note 6	Note 6
MOBILE_DDR	–0.300	20% V_{CCO}	80% V_{CCO}	V_{CCO} + 0.300	10% V_{CCO}	90% V_{CCO}	0.10	–0.10
PCI33_3	–0.400	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.500	10% V_{CCO}	90% V_{CCO}	1.50	–0.50
SSTL135	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	13.00	–13.00
SSTL135_R	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	8.90	–8.90
SSTL15	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.175	V_{CCO}/2 + 0.175	13.00	–13.00
SSTL15_R	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.175	V_{CCO}/2 + 0.175	8.90	–8.90
SSTL18_I	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 – 0.470	V_{CCO}/2 + 0.470	8.00	–8.00
SSTL18_II	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 – 0.600	V_{CCO}/2 + 0.600	13.40	–13.40

Notes:

1. Tested according to relevant specifications.
2. 3.3V and 2.5V standards are only supported in HR I/O banks.
3. For detailed interface specific DC voltage levels, see the *7 Series FPGAs SelectIO Resources User Guide* (UG471) [Ref 3].
4. Supported drive strengths of 4, 8, or 12 mA in HR I/O banks.
5. Supported drive strengths of 4, 8, 12, or 16 mA in HR I/O banks.
6. Supported drive strengths of 4, 8, 12, 16, or 24 mA in HR I/O banks.

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications from the Vivado® Design Suite as outlined in Table 12.

Table 12: **Speed Specification Version By Device**

2018.2.1	Device
1.23	XC7S6, XC7S15, XC7S25, XC7S50, XC7S75, XC7S100
1.16	XA7S6, XA7S15, XA7S25, XA7S50, XA7S75, XA7S100

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows.

Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Spartan-7 FPGAs.

Table 18: **IOB 3-state Output Switching Characteristics**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
T_{IOTPHZ}	T input to pad high-impedance.	2.19	2.37	2.37	ns
$T_{IOIBUFDISABLE}$	IBUF turn-on time from IBUFDISABLE to O output.	2.30	2.60	2.60	ns

Output Delay Measurements

Output delays are measured with short output traces. Standard termination was used for all testing. The propagation delay of the trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 1 and Figure 2.

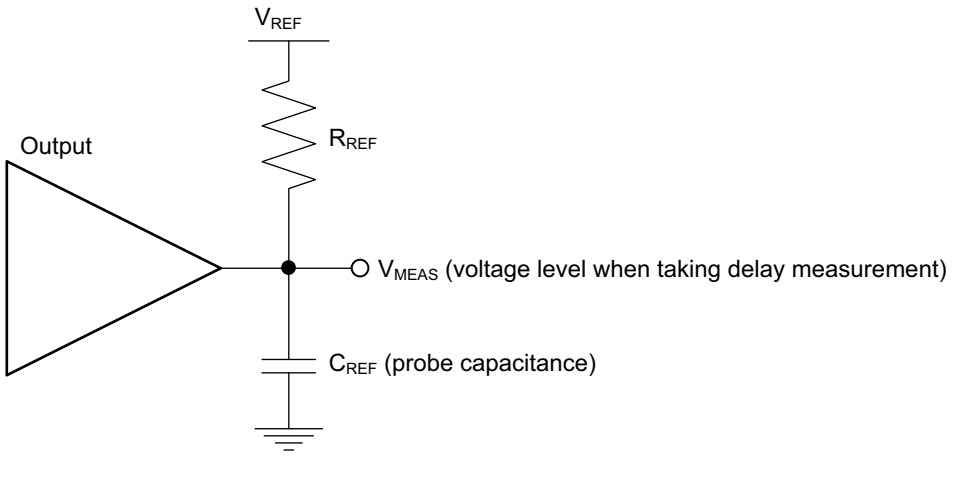

Figure 1: **Single-ended Test Setup**

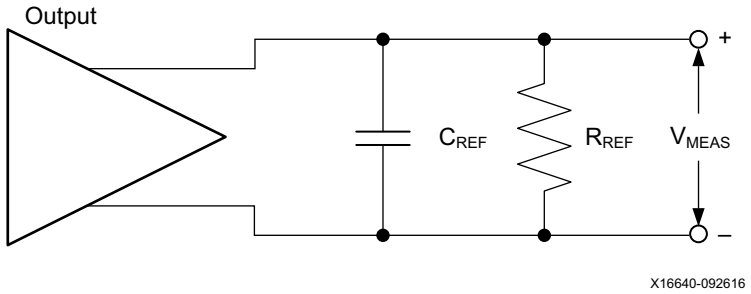

Figure 2: **Differential Test Setup**

Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using this method:

1. Simulate the output driver of choice into the generalized test setup using values from Table 20.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of step 2 and step 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Input/Output Logic Switching Characteristics

Table 21: **ILOGIC Switching Characteristics**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Setup/Hold					
T_{ICE1CK}/T_{ICKCE1}	CE1 pin setup/hold with respect to CLK.	0.54/0.02	0.76/0.02	0.76/0.02	ns
T_{ISRCK}/T_{ICKSR}	SR pin setup/hold with respect to CLK.	0.70/0.01	1.13/0.01	1.13/0.01	ns
T_{IDOCK}/T_{IOCKD}	D pin setup/hold with respect to CLK without delay.	0.01/0.29	0.01/0.33	0.01/0.33	ns
T_{IDOCKD}/T_{IOCKDD}	DDLY pin setup/hold with respect to CLK (using IDELAY).	0.02/0.29	0.02/0.33	0.02/0.33	ns
Combinatorial					
T_{IDI}	D pin to O pin propagation delay, no delay.	0.11	0.13	0.13	ns
T_{IDID}	DDLY pin to O pin propagation delay (using IDELAY).	0.12	0.14	0.14	ns
Sequential Delays					
T_{IDLO}	D pin to Q1 pin using flip-flop as a latch without delay.	0.44	0.51	0.51	ns
T_{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY).	0.44	0.51	0.51	ns
T_{ICKQ}	CLK to Q outputs.	0.57	0.66	0.66	ns
T_{RQ_ILOGIC}	SR pin to OQ/TQ out.	1.08	1.32	1.32	ns
T_{GSRQ_ILOGIC}	Global set/reset to Q outputs.	7.60	10.51	10.51	ns
Set/Reset					
T_{RPW_ILOGIC}	Minimum pulse width, SR inputs.	0.72	0.72	0.72	ns, Min

Input Serializer/Deserializer Switching Characteristics

Table 23: **ISERDES Switching Characteristics**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Setup/Hold for Control Lines					
$T_{ISCCK\_BITSLIP}$/ $T_{ISCKC\_BITSLIP}$	BITSLIP pin setup/hold with respect to CLKDIV.	0.02/0.15	0.02/0.17	0.02/0.17	ns
T_{ISCCK_CE}/ T_{ISCKC_CE}	CE pin setup/hold with respect to CLK (for CE1).	0.50/–0.01	0.72/–0.01	0.72/–0.01	ns
T_{ISCCK_CE2}/ T_{ISCKC_CE2}	CE pin setup/hold with respect to CLKDIV (for CE2).	–0.10/0.36	–0.10/0.40	–0.10/0.40	ns
Setup/Hold for Data Lines					
T_{ISDCK_D}/ T_{ISCKD_D}	D pin setup/hold with respect to CLK.	–0.02/0.14	–0.02/0.17	–0.02/0.17	ns
T_{ISDCK_DDLY}/ T_{ISCKD_DDLY}	DDLY pin setup/hold with respect to CLK (using IDELAY).(1)	–0.02/0.14	–0.02/0.17	–0.02/0.17	ns
$T_{ISDCK\_D\_DDR}$/ $T_{ISCKD\_D\_DDR}$	D pin setup/hold with respect to CLK at DDR mode.	–0.02/0.14	–0.02/0.17	–0.02/0.17	ns
$T_{ISDCK\_DDLY\_DDR}$/ $T_{ISCKD\_DDLY\_DDR}$	D pin setup/hold with respect to CLK at DDR mode (using IDELAY).(1)	0.14/0.14	0.17/0.17	0.17/0.17	ns
Sequential Delays					
T_{ISCKO_Q}	CLKDIV to out at Q pin.	0.54	0.66	0.66	ns
Propagation Delays					
T_{ISDO_DO}	D input to DO output pin.	0.11	0.13	0.13	ns

Notes:

1. Recorded at 0 tap value.

Input/Output Delay Switching Characteristics

Table 25: **Input/Output Delay Switching Characteristics**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
IDELAYCTRL					
T_{DLYCCO_RDY}	Reset to ready for IDELAYCTRL.	3.67	3.67	3.67	µs
$F_{IDELAYCTRL\_REF}$	Attribute REFCLK frequency = 200.00.(1)	200.00	200.00	200.00	MHz
	Attribute REFCLK frequency = 300.00.(1)	300.00	300.00	300.00	MHz
	Attribute REFCLK frequency = 400.00.(1)	400.00	N/A	N/A	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	±10	MHz
$T_{IDELAYCTRL\_RPW}$	Minimum reset pulse width.	59.28	59.28	59.28	ns
IDELAY					
$T_{IDELAYRESOLUTION}$	IDELAY chain delay resolution.	1/(32 x 2 x F_{REF})			µs
$T_{IDELAYPAT\_JIT}$	Pattern dependent period jitter in delay chain for clock pattern.(2)	0	0	0	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23).(3)	±5	±5	±5	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23).(4)	±9	±9	±9	ps per tap
$T_{IDELAY\_CLK\_MAX}$	Maximum frequency of CLK input to IDELAY.	680.00	600.00	600.00	MHz
T_{IDCCK_CE} / T_{IDCKC_CE}	CE pin setup/hold with respect to C for IDELAY.	0.16/0.13	0.21/0.16	0.21/0.16	ns
T_{IDCCK_INC}/ T_{IDCKC_INC}	INC pin setup/hold with respect to C for IDELAY.	0.14/0.18	0.16/0.22	0.16/0.22	ns
T_{IDCCK_RST}/ T_{IDCKC_RST}	RST pin setup/hold with respect to C for IDELAY.	0.16/0.11	0.18/0.14	0.18/0.14	ns
$T_{IDDO\_IDATAIN}$	Propagation delay through IDELAY.	Note 5	Note 5	Note 5	ps

Notes:

1. Average tap delay at 200 MHz = 78 ps, at 300 MHz = 52 ps, and at 400 MHz = 39 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE.
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY tap setting. See the timing report for actual values.

CLB Switching Characteristics

Table 27: **CLB Switching Characteristics**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Combinatorial Delays					
T_{ILO}	An – Dn LUT address to A.	0.11	0.13	0.13	ns, Max
T_{ILO_2}	An – Dn LUT address to AMUX/CMUX.	0.30	0.36	0.36	ns, Max
T_{ILO_3}	An – Dn LUT address to BMUX_A.	0.46	0.55	0.55	ns, Max
T_{ITO}	An – Dn inputs to A – D Q outputs.	1.05	1.27	1.27	ns, Max
T_{AXA}	AX inputs to AMUX output.	0.69	0.84	0.84	ns, Max
T_{AXB}	AX inputs to BMUX output.	0.66	0.83	0.83	ns, Max
T_{AXC}	AX inputs to CMUX output.	0.68	0.82	0.82	ns, Max
T_{AXD}	AX inputs to DMUX output.	0.75	0.90	0.90	ns, Max
T_{BXB}	BX inputs to BMUX output.	0.57	0.69	0.69	ns, Max
T_{BXD}	BX inputs to DMUX output.	0.69	0.82	0.82	ns, Max
T_{CXC}	CX inputs to CMUX output.	0.48	0.58	0.58	ns, Max
T_{CXD}	CX inputs to DMUX output.	0.59	0.71	0.71	ns, Max
T_{DXD}	DX inputs to DMUX output.	0.58	0.70	0.70	ns, Max
Sequential Delays					
T_{CKO}	Clock to AQ – DQ outputs.	0.44	0.53	0.53	ns, Max
T_{SHCKO}	Clock to AMUX – DMUX outputs.	0.53	0.66	0.66	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK					
T_{AS}/T_{AH}	AN – DN input to CLK on A – D flip-flops.	0.09/0.14	0.11/0.18	0.11/0.18	ns, Min
T_{DICK}/T_{CKDI}	AX – DX input to CLK on A – D flip-flops.	0.07/0.21	0.09/0.26	0.09/0.26	ns, Min
	AX – DX input through MUXs and/or carry logic to CLK on A – D flip-flops.	0.66/0.09	0.81/0.11	0.81/0.11	ns, Min
$T_{CECK\_CLB}/T_{CKCE\_CLB}$	CE input to CLK on A – D flip-flops.	0.17/0.00	0.21/0.01	0.21/0.01	ns, Min
T_{SRCK}/T_{CKSR}	SR input to CLK on A – D flip-flops.	0.43/0.04	0.53/0.05	0.53/0.05	ns, Min
Set/Reset					
T_{SRMIN}	SR input minimum pulse width.	0.78	1.04	1.04	ns, Min
T_{RQ}	Delay from SR input to AQ – DQ flip-flops.	0.59	0.71	0.71	ns, Max
T_{CEO}	Delay from CE input to AQ – DQ flip-flops.	0.58	0.70	0.70	ns, Max
F_{TOG}	Toggle frequency (for export control).	1286	1098	1098	MHz

Block RAM and FIFO Switching Characteristics

Table 30: **Block RAM and FIFO Switching Characteristics**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Block RAM and FIFO Clock-to-Out Delays					
T_{RCKO_DO} and $T_{RCKO\_DO\_REG}$	Clock CLK to DOUT output (without output register).(1)(2)	2.13	2.46	2.46	ns, Max
	Clock CLK to DOUT output (with output register).(3)(4)	0.74	0.89	0.89	ns, Max
$T_{RCKO\_DO\_ECC}$ and $T_{RCKO\_DO\_ECC\_REG}$	Clock CLK to DOUT output with ECC (without output register).(1)(2)	3.04	3.84	3.84	ns, Max
	Clock CLK to DOUT output with ECC (with output register).(3)(4)	0.81	0.94	0.94	ns, Max
$T_{RCKO\_DO\_CASCOUT}$ and $T_{RCKO\_DO\_CASCOUT\_REG}$	Clock CLK to DOUT output with cascade (without output register).(1)	2.88	3.30	3.30	ns, Max
	Clock CLK to DOUT output with cascade (with output register).(3)	1.28	1.46	1.46	ns, Max
T_{RCKO_FLAGS}	Clock CLK to FIFO flags outputs.(5)	0.87	1.05	1.05	ns, Max
$T_{RCKO\_POINTERS}$	Clock CLK to FIFO pointers outputs.(6)	1.02	1.15	1.15	ns, Max
$T_{RCKO\_PARITY\_ECC}$	Clock CLK to ECCPARITY in ECC encode only mode.	0.85	0.94	0.94	ns, Max
$T_{RCKO\_SDBIT\_ECC}$ and $T_{RCKO\_SDBIT\_ECC\_REG}$	Clock CLK to BITERR (without output register).	2.81	3.55	3.55	ns, Max
	Clock CLK to BITERR (with output register).	0.76	0.89	0.89	ns, Max
$T_{RCKO\_RDADDR\_ECC}$ and $T_{RCKO\_RDADDR\_ECC\_REG}$	Clock CLK to RDADDR output with ECC (without output register).	0.88	1.07	1.07	ns, Max
	Clock CLK to RDADDR output with ECC (with output register).	0.93	1.08	1.08	ns, Max
Setup and Hold Times Before/After Clock CLK					
T_{RCCK_ADDRA}/ T_{RCKC_ADDRA}	ADDR inputs.(7)	0.49/0.33	0.57/0.36	0.57/0.36	ns, Min
$T_{RDCK\_DI\_WF\_NC}$/ $T_{RCKD\_DI\_WF\_NC}$	Data input setup/hold time when block RAM is configured in WRITE_FIRST or NO_CHANGE mode.(8)	0.65/0.63	0.74/0.67	0.74/0.67	ns, Min
$T_{RDCK\_DI\_RF}$/ $T_{RCKD\_DI\_RF}$	Data input setup/hold time when block RAM is configured in READ_FIRST mode.(8)	0.22/0.34	0.25/0.41	0.25/0.41	ns, Min
$T_{RDCK\_DI\_ECC}$/ $T_{RCKD\_DI\_ECC}$	DIN inputs with block RAM ECC in standard mode.(8)	0.55/0.46	0.63/0.50	0.63/0.50	ns, Min
$T_{RDCK\_DI\_ECCW}$/ $T_{RCKD\_DI\_ECCW}$	DIN inputs with block RAM ECC encode only.(8)	1.02/0.46	1.17/0.50	1.17/0.50	ns, Min

Table 30: **Block RAM and FIFO Switching Characteristics *(Cont'd)***

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
$T_{RDCK\_DI\_ECC\_FIFO}$/ $T_{RCKD\_DI\_ECC\_FIFO}$	DIN inputs with FIFO ECC in standard mode.(8)	1.15/0.59	1.32/0.64	1.32/0.64	ns, Min
$T_{RCCK\_INJECTBITERR}$/ $T_{RCKC\_INJECTBITERR}$	Inject single/double bit error in ECC mode.	0.64/0.37	0.74/0.40	0.74/0.40	ns, Min
T_{RCCK_EN}/T_{RCKC_EN}	Block RAM enable (EN) input.	0.39/0.21	0.45/0.23	0.45/0.23	ns, Min
T_{RCCK_REGCE}/ T_{RCKC_REGCE}	CE input of output register.	0.29/0.15	0.36/0.16	0.36/0.16	ns, Min
T_{RCCK_RSTREG}/ T_{RCKC_RSTREG}	Synchronous RSTREG input.	0.32/0.07	0.35/0.07	0.35/0.07	ns, Min
T_{RCCK_RSTRAM}/ T_{RCKC_RSTRAM}	Synchronous RSTRAM input.	0.34/0.43	0.36/0.46	0.36/0.46	ns, Min
T_{RCCK_WEA}/T_{RCKC_WEA}	Write enable (WE) input (block RAM only).	0.48/0.19	0.54/0.20	0.54/0.20	ns, Min
T_{RCCK_WREN}/ T_{RCKC_WREN}	WREN FIFO inputs.	0.46/0.35	0.47/0.43	0.47/0.43	ns, Min
T_{RCCK_RDEN}/ T_{RCKC_RDEN}	RDEN FIFO inputs.	0.43/0.35	0.43/0.43	0.43/0.43	ns, Min
Reset Delays					
T_{RCO_FLAGS}	Reset RST to FIFO flags/pointers.(9)	0.98	1.10	1.10	ns, Max
T_{RREC_RST}/T_{RREM_RST}	FIFO reset recovery and removal timing.(10)	2.07/–0.81	2.37/–0.81	2.37/–0.81	ns, Max
Maximum Frequency					
$F_{MAX\_BRAM\_WF\_NC}$	Block RAM (write first and no change modes) when not in SDP RF mode.	460.83	388.20	388.20	MHz
$F_{MAX\_BRAM\_RF\_PERFORMANCE}$	Block RAM (read first, performance mode) when in SDP RF mode but no address overlap between port A and port B.	460.83	388.20	388.20	MHz
$F_{MAX\_BRAM\_RF\_DELAYED\_WRITE}$	Block RAM (read first, delayed write mode) when in SDP RF mode and there is possibility of overlap between port A and port B addresses.	404.53	339.67	339.67	MHz
$F_{MAX\_CAS\_WF\_NC}$	Block RAM cascade (write first, no change mode) when cascade but not in RF mode.	418.59	345.78	345.78	MHz
$F_{MAX\_CAS\_RF\_PERFORMANCE}$	Block RAM cascade (read first, performance mode) when in cascade with RF mode and no possibility of address overlap/one port is disabled.	418.59	345.78	345.78	MHz

Clock Buffers and Networks

Table 32: **Global Clock Switching Characteristics (Including BUFGCTRL)**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
$T_{BCCCK\_CE}/T_{BCCKC\_CE}$(1)	CE pins setup/hold.	0.13/0.40	0.16/0.41	0.16/0.41	ns
T_{BCCCK_S}/T_{BCCKC_S}(1)	S pins setup/hold.	0.13/0.40	0.16/0.41	0.16/0.41	ns
T_{BCCKO_O}(2)	BUFGCTRL delay from I0/I1 to O.	0.09	0.10	0.10	ns
Maximum Frequency					
F_{MAX_BUFG}	Global clock tree (BUFG).	628.00	464.00	464.00	MHz

Notes:

1. T_{BCCCK_CE} and T_{BCCKC_CE} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. T_{BGCKO_O} (BUFG delay from I0 to O) values are the same as T_{BCCKO_O} values.

Table 33: **Input/Output Clock Switching Characteristics (BUFIO)**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
T_{BIOCKO_O}	Clock to out delay from I to O.	1.26	1.54	1.54	ns
Maximum Frequency					
F_{MAX_BUFIO}	I/O clock tree (BUFIO).	680.00	600.00	600.00	MHz

Table 34: **Regional Clock Buffer Switching Characteristics (BUFR)**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
T_{BRCKO_O}	Clock to out delay from I to O.	0.76	0.99	0.99	ns
$T_{BRCKO\_O\_BYP}$	Clock to out delay from I to O with Divide Bypass attribute set.	0.39	0.52	0.52	ns
T_{BRDO_O}	Propagation delay from CLR to O.	0.85	1.09	1.09	ns
Maximum Frequency					
F_{MAX_BUFR}(1)	Regional clock tree (BUFR).	375.00	315.00	315.00	MHz

Notes:

1. The maximum input frequency to the BUFR is the BUFIO F_{MAX} frequency.

MMCM Switching Characteristics

Table 37: **MMCM Specification**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
MMCM_F_{INMAX}	Maximum input clock frequency.	800.00	800.00	800.00	MHz
MMCM_F_{INMIN}	Minimum input clock frequency.	10.00	10.00	10.00	MHz
MMCM_$F_{INJITTER}$	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max			
MMCM_F_{INDUTY}	Allowable input duty cycle: 10—49 MHz.	25	25	25	%
	Allowable input duty cycle: 50—199 MHz.	30	30	30	%
	Allowable input duty cycle: 200—399 MHz.	35	35	35	%
	Allowable input duty cycle: 400—499 MHz.	40	40	40	%
	Allowable input duty cycle: > 500 MHz.	45	45	45	%
MMCM_F_{MIN_PSCLK}	Minimum dynamic phase-shift clock frequency.	0.01	0.01	0.01	MHz
MMCM_F_{MAX_PSCLK}	Maximum dynamic phase-shift clock frequency.	500.00	450.00	450.00	MHz
MMCM_F_{VCOMIN}	Minimum MMCM VCO frequency.	600.00	600.00	600.00	MHz
MMCM_F_{VCOMAX}	Maximum MMCM VCO frequency.	1440.00	1200.00	1200.00	MHz
MMCM_$F_{BANDWIDTH}$	Low MMCM bandwidth at typical.(1)	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical.(1)	4.00	4.00	4.00	MHz
MMCM_$T_{STATPHAOFFSET}$	Static phase offset of the MMCM outputs.(2)	0.12	0.12	0.12	ns
MMCM_$T_{OUTJITTER}$	MMCM output jitter.	Note 3			
MMCM_$T_{OUTDUTY}$	MMCM output clock duty-cycle precision.(4)	0.20	0.20	0.20	ns
MMCM_$T_{LOCKMAX}$	MMCM maximum lock time.	100.00	100.00	100.00	µs
MMCM_F_{OUTMAX}	MMCM maximum output frequency.	800.00	800.00	800.00	MHz
MMCM_F_{OUTMIN}	MMCM minimum output frequency.(5)(6)	4.69	4.69	4.69	MHz
MMCM_$T_{EXTFDVAR}$	External clock feedback variation.	< 20% of clock input period or 1 ns Max			
MMCM_$RST_{MINPULSE}$	Minimum reset pulse width.	5.00	5.00	5.00	ns
MMCM_F_{PFDMAX}	Maximum frequency at the phase frequency detector.	500.00	450.00	450.00	MHz
MMCM_F_{PFDMIN}	Minimum frequency at the phase frequency detector.	10.00	10.00	10.00	MHz
MMCM_$T_{FBDELAY}$	Maximum delay in the feedback path.	3 ns Max or one CLKIN cycle			
MMCM Switching Characteristics Setup and Hold					
$T_{MMCMDCK\_PSEN}$/ $T_{MMCMCKD\_PSEN}$	Setup and hold of phase-shift enable.	1.04/0.00	1.04/0.00	1.04/0.00	ns

Device Pin-to-Pin Output Parameter Guidelines

Table 39: **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)[1]**

Symbol	Description	Device	V_{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM/PLL.						
T_{ICKOF}	Clock-capable clock input and OUTFF at pins/banks closest to the BUFGs *without* MMCM/PLL (near clock region).[2]	XC7S6	5.55	6.50	6.50	ns
		XC7S15	5.55	6.50	6.50	ns
		XC7S25	5.55	6.44	6.44	ns
		XC7S50	5.71	6.62	6.62	ns
		XC7S75	5.73	6.71	6.71	ns
		XC7S100	5.73	6.71	6.71	ns
		XA7S6	5.55	6.50	N/A	ns
		XA7S15	5.55	6.50	N/A	ns
		XA7S25	5.55	6.44	N/A	ns
		XA7S50	5.71	6.62	N/A	ns
		XA7S75	5.73	6.71	N/A	ns
		XA7S100	5.73	6.71	N/A	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Refer to the *Die Level Bank Numbering Overview* section of the *7 Series FPGA Packaging and Pinout Specification* (UG475) [Ref 4].

Table 42: **Clock-Capable Clock Input to Output Delay With PLL(1)**

Symbol	Description	Device	V_{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *with* PLL.						
$T_{ICKOFPLLCC}$	Clock-capable clock input and OUTFF *with* PLL.(2)	XC7S6	0.85	0.85	0.85	ns
		XC7S15	0.85	0.85	0.85	ns
		XC7S25	0.83	0.83	0.83	ns
		XC7S50	0.83	0.83	0.83	ns
		XC7S75	0.83	0.83	0.83	ns
		XC7S100	0.83	0.83	0.83	ns
		XA7S6	0.85	0.85	N/A	ns
		XA7S15	0.85	0.85	N/A	ns
		XA7S25	0.83	0.83	N/A	ns
		XA7S50	0.83	0.83	N/A	ns
		XA7S75	0.83	0.83	N/A	ns
		XA7S100	0.83	0.83	N/A	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is already included in the timing calculation.

Table 43: **Pin-to-Pin, Clock-to-Out using BUFIO**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with BUFIO.					
$T_{ICKOFCS}$	Clock to out of I/O clock.	5.61	6.64	6.64	ns

Table 45: **Clock-Capable Clock Input Setup and Hold With MMCM**

Symbol	Description	Device	V_{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1)(2)						
$T_{PSMMCMCC}$/ $T_{PHMMCMCC}$	No delay clock-capable clock input and IFF(3) with MMCM.	XC7S6	2.73/–0.59	3.27/–0.59	3.27/–0.59	ns
		XC7S15	2.73/–0.59	3.27/–0.59	3.27/–0.59	ns
		XC7S25	2.69/–0.61	3.21/–0.61	3.21/–0.61	ns
		XC7S50	2.81/–0.62	3.35/–0.62	3.35/–0.62	ns
		XC7S75	2.81/–0.62	3.36/–0.62	3.36/–0.62	ns
		XC7S100	2.81/–0.62	3.36/–0.62	3.36/–0.62	ns
		XA7S6	2.73/–0.59	3.27/–0.59	N/A	ns
		XA7S15	2.73/–0.59	3.27/–0.59	N/A	ns
		XA7S25	2.69/–0.61	3.21/–0.61	N/A	ns
		XA7S50	2.81/–0.62	3.35/–0.62	N/A	ns
		XA7S75	2.81/–0.62	3.36/–0.62	N/A	ns
		XA7S100	2.81/–0.62	3.36/–0.62	N/A	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. Use IBIS to determine any duty-cycle distortion incurred using various standards.
3. IFF = Input flip-flop or latch.

XADC Specifications

The *7 Series FPGAs Overview* (DS180) [Ref 1] and *XA Spartan-7 Automotive FPGA Data Sheet: Overview* (DS171) [Ref 2] list the devices that contain a 7 series XADC dual 12-Bit 1 MSPS analog-to-digital converter.

Table 50: **XADC Specifications**

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
V_{CCADC} = 1.8V ± 5%, V_{REFP} = 1.25V, V_{REFN} = 0V, ADCCLK = 26 MHz, –55°C ≤ T_j ≤ 125°C. Typical values at T_j = +40°C.						
ADC Accuracy(1)						
Resolution			12	–	–	Bits
Integral nonlinearity(2)	INL	–40°C ≤ T_j ≤ 100°C	–	–	±2	LSBs
		–55°C ≤ T_j < –40°C; 100°C < T_j ≤ 125°C	–	–	±3	LSBs
Differential nonlinearity	DNL	No missing codes, guaranteed monotonic.	–	–	±1	LSBs
Offset error	Unipolar	–40°C ≤ T_j ≤ 100°C	–	–	±8	LSBs
		–55°C ≤ T_j < –40°C; 100°C < T_j ≤ 125°C	–	–	±12	LSBs
	Bipolar	–55°C ≤ T_j ≤ 125°C	–	–	±4	LSBs
Gain error			–	–	±0.5	%
Offset matching			–	–	4	LSBs
Gain matching			–	–	0.3	%
Sample rate			–	–	1	MS/s
Signal to noise ratio(2)	SNR	F_{SAMPLE} = 500 KS/s, F_{IN} = 20 kHz	60	–	–	dB
RMS code noise		External 1.25V reference.	–	–	2	LSBs
		On-chip reference.	–	3	–	LSBs
Total harmonic distortion(2)	THD	F_{SAMPLE} = 500 KS/s, F_{IN} = 20 kHz	70	–	–	dB
Analog Inputs(3)						
ADC input ranges		Unipolar operation.	0	–	1	V
		Bipolar operation.	–0.5	–	+0.5	V
		Unipolar common mode range (FS input).	0	–	+0.5	V
		Bipolar common mode range (FS input).	+0.5	–	+0.6	V
Maximum external channel input ranges		Adjacent analog channels set within these ranges should not corrupt measurements on adjacent channels.	–0.1	–	V_{CCADC}	V
Full-resolution bandwidth	FRBW	Auxiliary channel full resolution bandwidth.	250	–	–	kHz
On-chip Sensors						
Temperature sensor error		–40°C ≤ T_j ≤ 100°C	–	–	±4	°C
		–55°C ≤ T_j < –40°C; 100°C < T_j ≤ 125°C	–	–	±6	°C
Supply sensor error		–40°C ≤ T_j ≤ 100°C	–	–	±1	%
		–55°C ≤ T_j < –40°C; 100°C < T_j ≤ 125°C	–	–	±2	%

Table 50: **XADC Specifications *(Cont'd)***

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Conversion Rate(4)						
Conversion time: continuous	t_{CONV}	Number of ADCCLK cycles.	26	–	32	Cycles
Conversion time: event	t_{CONV}	Number of CLK cycles.	–	–	21	Cycles
DRP clock frequency	DCLK	DRP clock frequency.	8	–	250	MHz
ADC clock frequency	ADCCLK	Derived from DCLK.	1	–	26	MHz
DCLK duty cycle			40	–	60	%
XADC Reference(5)						
External reference	V_{REFP}	Externally supplied reference voltage.	1.20	1.25	1.30	V
On-chip reference		Ground V_{REFP} pin to AGND, $-40°C \le T_j \le 100°C$	1.2375	1.25	1.2625	V
		Ground VREFP pin to AGND, $-55°C \le T_j < -40°C$; $100°C < T_j \le 125°C$	1.225	1.25	1.275	V

Notes:

1. Offset and gain errors are removed by enabling the XADC automatic gain calibration feature. The values are specified for when this feature is enabled.
2. Only specified for bitstream option XADCEnhancedLinearity = ON.
3. For a detailed description, see the *ADC* chapter in the *7 Series FPGAs and Zynq-7000 AP SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480) [Ref 9].
4. For a detailed description, see the *Timing* chapter in the *7 Series FPGAs and Zynq-7000 AP SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480) [Ref 9].
5. Any variation in the reference voltage from the nominal V_{REFP} = 1.25V and V_{REFN} = 0V will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted.

Table 51: **Configuration Switching Characteristics *(Cont'd)***

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
$T_{SMCSCCK}$/ $T_{SMCCKCS}$	CSI_B setup/hold.	4.00/0.00	4.00/0.00	4.00/0.00	ns, Min
T_{SMWCCK}/ T_{SMCCKW}	RDWR_B setup/hold.	10.00/0.00	10.00/0.00	10.00/0.00	ns, Min
$T_{SMCKCSO}$	CSO_B clock to out (330 Ω pull-up resistor required).	7.00	7.00	7.00	ns, Max
T_{SMCO}	D[31:00] clock to out in readback.	8.00	8.00	8.00	ns, Max
F_{RBCCK}	Readback frequency.	100.00	100.00	100.00	MHz, Max
Boundary-Scan Port Timing Specifications					
T_{TAPTCK}/ T_{TCKTAP}	TMS and TDI setup/hold.	3.00/2.00	3.00/2.00	3.00/2.00	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output.	7.00	7.00	7.00	ns, Max
F_{TCK}	TCK frequency.	66.00	66.00	66.00	MHz, Max
SPI Flash Master Mode Programming Switching					
T_{SPIDCC}/ T_{SPICCD}	D[03:00] setup/hold.	3.00/0.00	3.00/0.00	3.00/0.00	ns, Min
T_{SPICCM}	MOSI clock to out.	8.00	8.00	8.00	ns, Max
$T_{SPICCFC}$	FCS_B clock to out.	8.00	8.00	8.00	ns, Max
STARTUPE2 Ports					
$T_{USRCCLKO}$	STARTUPE2 USRCCLKO input to CCLK output.	0.50/6.70	0.50/7.50	0.50/7.50	ns, Min/Max
$F_{CFGMCLK}$	STARTUPE2 CFGMCLK output frequency.	65.00	65.00	65.00	MHz, Typ
$F_{CFGMCLKTOL}$	STARTUPE2 CFGMCLK output frequency tolerance.	±50	±50	±50	%, Max
Device DNA Access Port					
F_{DNACK}	DNA access port (DNA_PORT).	100.00	100.00	100.00	MHz, Max

Notes:

1. To support longer delays in configuration, use the design solutions described in the *7 Series FPGA Configuration User Guide* (UG470) [Ref 10].
2. See the *7 Series FPGAs Overview* (DS180) [Ref 1] and *XA Spartan-7 Automotive FPGA Data Sheet: Overview* (DS171) [Ref 2] for a list of devices that support bitstream encryption.

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