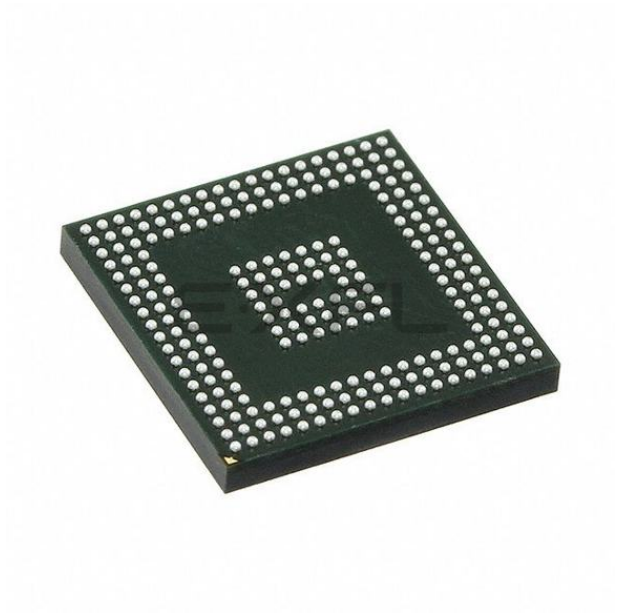
AMD Xilinx - XC7S25-L1CSGA324I Datasheet



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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1825
Number of Logic Elements/Cells	23360
Total RAM Bits	1658880
Number of I/O	150
Number of Gates	-
Voltage - Supply	0.92V ~ 0.98V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	324-LFBGA, CSPBGA
Supplier Device Package	324-CSGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7s25-l1csga324i

Table 2: **Recommended Operating Conditions(1)(2)**

Symbol	Description	Min	Typ	Max	Units
FPGA Logic					
V_{CCINT}(3)	For -2 and -1 (1.0V) devices: internal supply voltage.	0.95	1.00	1.05	V
	For -1L (0.95V) devices: internal supply voltage.	0.92	0.95	0.98	V
V_{CCAUX}	Auxiliary supply voltage.	1.71	1.80	1.89	V
V_{CCBRAM}(3)	For -2 and -1 (1.0V) devices: block RAM supply voltage.	0.95	1.00	1.05	V
	For -1L (0.95V) devices: block RAM supply voltage.	0.92	0.95	0.98	V
V_{CCO}(4)(5)	Supply voltage for HR I/O banks.	1.14	–	3.465	V
V_{IN}(6)	I/O input voltage.	–0.20	–	V_{CCO} + 0.20	V
	I/O input voltage (when V_{CCO} = 3.3V) for V_{REF} and differential I/O standards except TMDS_33.(7)	–0.20	–	2.625	V
I_{IN}(8)	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	–	–	10	mA
V_{CCBATT}(9)	Battery voltage.	1.0	–	1.89	V
XADC					
V_{CCADC}	XADC supply relative to GNDADC.	1.71	1.80	1.89	V
V_{REFP}	Externally supplied reference voltage.	1.20	1.25	1.30	V
Temperature					
T_j	Junction temperature operating range for commercial (C) temperature devices.	0	–	85	°C
	Junction temperature operating range for industrial (I) temperature devices.	–40	–	100	°C
	Junction temperature operating range for expanded (Q) temperature devices.	–40	–	125	°C

Notes:

1. All voltages are relative to ground.
2. For the design of the power distribution system consult the *7 Series FPGAs PCB Design Guide* (UG483) [Ref 5].
3. If V_{CCINT} and V_{CCBRAM} are operating at the same voltage, V_{CCINT} and V_{CCBRAM} should be connected to the same supply.
4. Configuration data is retained even if V_{CCO} drops to 0V.
5. Includes V_{CCO} of 1.2V, 1.35V, 1.5V, 1.8V, 2.5V, and 3.3V at ±5%.
6. The lower absolute voltage specification always applies.
7. See Table 9 for TMDS_33 specifications.
8. A total of 200 mA per bank should not be exceeded.
9. V_{CCBATT} is required only when using bitstream encryption. If battery is not used, connect V_{CCBATT} to either ground or V_{CCAUX}.

Table 5: **Typical Quiescent Supply Current[(1)(2)(3)] *(Cont'd)***

Symbol	Description	Device	Speed Grade						Units
			1.0V					0.95V	
			-2C	-2I	-1C	-1I	-1Q	-1LI	
I_{CCOQ}	Quiescent V_{CCO} supply current.	XC7S6	1	1	1	1	1	1	mA
		XC7S15	1	1	1	1	1	1	mA
		XC7S25	1	1	1	1	1	1	mA
		XC7S50	1	1	1	1	1	1	mA
		XC7S75	4	4	4	4	4	4	mA
		XC7S100	4	4	4	4	4	4	mA
		XA7S6	N/A	1	N/A	1	1	N/A	mA
		XA7S15	N/A	1	N/A	1	1	N/A	mA
		XA7S25	N/A	1	N/A	1	1	N/A	mA
		XA7S50	N/A	1	N/A	1	1	N/A	mA
		XA7S75	N/A	4	N/A	4	4	N/A	mA
		XA7S100	N/A	4	N/A	4	4	N/A	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current.	XC7S6	10	10	10	10	10	10	mA
		XC7S15	10	10	10	10	10	10	mA
		XC7S25	13	13	13	13	13	13	mA
		XC7S50	22	22	22	22	22	20	mA
		XC7S75	43	43	43	43	43	43	mA
		XC7S100	43	43	43	43	43	43	mA
		XA7S6	N/A	10	N/A	10	10	N/A	mA
		XA7S15	N/A	10	N/A	10	10	N/A	mA
		XA7S25	N/A	13	N/A	13	13	N/A	mA
		XA7S50	N/A	22	N/A	22	22	N/A	mA
		XA7S75	N/A	43	N/A	43	43	N/A	mA
		XA7S100	N/A	43	N/A	43	43	N/A	mA

Table 6 shows the minimum current, in addition to I_{CCQ} maximum, that is required by Spartan-7 devices for proper power-on and configuration. If the current minimums shown in Table 6 are met, the device powers on after all four supplies have passed through their power-on reset threshold voltages. The FPGA must not be configured until after V_{CCINT} is applied. Once initialized and configured, use the *Xilinx Power Estimator* spreadsheet tool [Ref 6] to estimate current drain on these supplies.

Table 6: **Power-On Current**

Device	$I_{CCINTMIN}$	$I_{CCAUXMIN}$	I_{CCOMIN}	$I_{CCBRAMMIN}$	Units
XC7S6	I_{CCINTQ} + 120	I_{CCAUXQ} + 40	I_{CCOQ} + 40 mA per bank	$I_{CCBRAMQ}$ + 60	mA
XC7S15	I_{CCINTQ} + 120	I_{CCAUXQ} + 40	I_{CCOQ} + 40 mA per bank	$I_{CCBRAMQ}$ + 60	mA
XC7S25	I_{CCINTQ} + 120	I_{CCAUXQ} + 40	I_{CCOQ} + 40 mA per bank	$I_{CCBRAMQ}$ + 60	mA
XC7S50	I_{CCINTQ} + 120	I_{CCAUXQ} + 40	I_{CCOQ} + 40 mA per bank	$I_{CCBRAMQ}$ + 60	mA
XC7S75	I_{CCINTQ} + 300	I_{CCAUXQ} + 140	I_{CCOQ} + 40 mA per bank	$I_{CCBRAMQ}$ + 60	mA
XC7S100	I_{CCINTQ} + 300	I_{CCAUXQ} + 140	I_{CCOQ} + 40 mA per bank	$I_{CCBRAMQ}$ + 60	mA
XA7S6	I_{CCINTQ} + 120	I_{CCAUXQ} + 40	I_{CCOQ} + 40 mA per bank	$I_{CCBRAMQ}$ + 60	mA
XA7S15	I_{CCINTQ} + 120	I_{CCAUXQ} + 40	I_{CCOQ} + 40 mA per bank	$I_{CCBRAMQ}$ + 60	mA
XA7S25	I_{CCINTQ} + 120	I_{CCAUXQ} + 40	I_{CCOQ} + 40 mA per bank	$I_{CCBRAMQ}$ + 60	mA
XA7S50	I_{CCINTQ} + 120	I_{CCAUXQ} + 40	I_{CCOQ} + 40 mA per bank	$I_{CCBRAMQ}$ + 60	mA
XA7S75	I_{CCINTQ} + 300	I_{CCAUXQ} + 140	I_{CCOQ} + 40 mA per bank	$I_{CCBRAMQ}$ + 60	mA
XA7S100	I_{CCINTQ} + 300	I_{CCAUXQ} + 140	I_{CCOQ} + 40 mA per bank	$I_{CCBRAMQ}$ + 60	mA

Table 7: **Power Supply Ramp Time**

Symbol	Description	Conditions	Min	Max	Units
T_{VCCINT}	Ramp time from GND to 90% of V_{CCINT}.		0.2	50	ms
T_{VCCO}	Ramp time from GND to 90% of V_{CCO}.		0.2	50	ms
T_{VCCAUX}	Ramp time from GND to 90% of V_{CCAUX}.		0.2	50	ms
$T_{VCCBRAM}$	Ramp time from GND to 90% of V_{CCBRAM}.		0.2	50	ms
$T_{VCCO2VCCAUX}$	Allowed time per power cycle for $V_{CCO} - V_{CCAUX} > 2.625V$.	T_J = 125°C(1)	–	300	ms
		T_J = 100°C(1)	–	500	ms
		T_J = 85°C(1)	–	800	ms

Notes:

1. Based on 240,000 power cycles with a nominal V_{CCO} of 3.3V or 36,500 power cycles with a worst case V_{CCO} of 3.465V.

Table 9: **Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM}[1]			V_{ID}[2]			V_{OCM}[3]			V_{OD}[4]		
	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max
BLVDS_25	0.300	1.200	1.425	0.100	–	–	–	1.250	–	Note 5		
MINI_LVDS_25	0.300	1.200	V_{CCAUX}	0.200	0.400	0.600	1.000	1.200	1.400	0.300	0.450	0.600
PPDS_25	0.200	0.900	V_{CCAUX}	0.100	0.250	0.400	0.500	0.950	1.400	0.100	0.250	0.400
RSDS_25	0.300	0.900	1.500	0.100	0.350	0.600	1.000	1.200	1.400	0.100	0.350	0.600
TMDS_33	2.700	2.965	3.230	0.150	0.675	1.200	V_{CCO} – 0.405	V_{CCO} – 0.300	V_{CCO} – 0.190	0.400	0.600	0.800

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q – $\overline{Q}$).
3. V_{OCM} is the output common mode voltage.
4. V_{OD} is the output differential voltage (Q – $\overline{Q}$).
5. V_{OD} for BLVDS will vary significantly depending on topology and loading.

Table 10: **Complementary Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM}[1]			V_{ID}[2]		V_{OL}[3]	V_{OH}[4]	I_{OL}	I_{OH}
	V, Min	V, Typ	V, Max	V, Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
DIFF_HSTL_I	0.300	0.750	1.125	0.100	–	0.400	V_{CCO} – 0.400	8.00	–8.00
DIFF_HSTL_I_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO} – 0.400	8.00	–8.00
DIFF_HSTL_II	0.300	0.750	1.125	0.100	–	0.400	V_{CCO} – 0.400	16.00	–16.00
DIFF_HSTL_II_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO} – 0.400	16.00	–16.00
DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% V_{CCO}	80% V_{CCO}	0.100	–0.100
DIFF_MOBILE_DDR	0.300	0.900	1.425	0.100	–	10% V_{CCO}	90% V_{CCO}	0.100	–0.100
DIFF_SSTL135	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	13.0	–13.0
DIFF_SSTL135_R	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	8.9	–8.9
DIFF_SSTL15	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	13.0	–13.0
DIFF_SSTL15_R	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	8.9	–8.9
DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.470	(V_{CCO}/2) + 0.470	8.00	–8.00
DIFF_SSTL18_II	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.600	(V_{CCO}/2) + 0.600	13.4	–13.4

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q – $\overline{Q}$).
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

Table 19 shows the test setup parameters used for measuring input delay.

Table 19: **Input Delay Measurement Methodology**

Description	I/O Standard Attribute	V_L[1]	V_H[1]	V_{MEAS}[3][5]	V_{REF}[2][4]
LVCMOS, 1.2V	LVCMOS12	0.1	1.1	0.6	–
LVCMOS, 1.5V	LVCMOS15	0.1	1.4	0.75	–
LVCMOS, 1.8V	LVCMOS18	0.1	1.7	0.9	–
LVCMOS, 2.5V	LVCMOS25	0.1	2.4	1.25	–
LVCMOS, 3.3V	LVCMOS33	0.1	3.2	1.65	–
LVTTL, 3.3V	LVTTL	0.1	3.2	1.65	–
MOBILE_DDR, 1.8V	MOBILE_DDR	0.1	1.7	0.9	–
PCI33, 3.3V	PCI33_3	0.1	3.2	1.65	–
HSTL (high-speed transceiver logic), Class I, 1.2V	HSTL_I_12	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.60
HSTL, Class I & II, 1.5V	HSTL_I, HSTL_II	V_{REF} – 0.65	V_{REF} + 0.65	V_{REF}	0.75
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	V_{REF} – 0.8	V_{REF} + 0.8	V_{REF}	0.90
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.60
SSTL (stub-terminated transceiver logic), 1.2V	SSTL12	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.60
SSTL, 1.35V	SSTL135, SSTL135_R	V_{REF} – 0.575	V_{REF} + 0.575	V_{REF}	0.675
SSTL, 1.5V	SSTL15, SSTL15_R	V_{REF} – 0.65	V_{REF} + 0.65	V_{REF}	0.75
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	V_{REF} – 0.8	V_{REF} + 0.8	V_{REF}	0.90
DIFF_MOBILE_DDR, 1.8V	DIFF_MOBILE_DDR	0.9 – 0.125	0.9 + 0.125	0[5]	–
DIFF_HSTL, Class I, 1.2V	DIFF_HSTL_I_12	0.6 – 0.125	0.6 + 0.125	0[5]	–
DIFF_HSTL, Class I & II,1.5V	DIFF_HSTL_I, DIFF_HSTL_II	0.75 – 0.125	0.75 + 0.125	0[5]	–
DIFF_HSTL, Class I & II, 1.8V	DIFF_HSTL_I_18, DIFF_HSTL_II_18	0.9 – 0.125	0.9 + 0.125	0[5]	–
DIFF_HSUL, 1.2V	DIFF_HSUL_12	0.6 – 0.125	0.6 + 0.125	0[5]	–
DIFF_SSTL135/ DIFF_SSTL135_R, 1.35V	DIFF_SSTL135, DIFF_SSTL135_R	0.675 – 0.125	0.675 + 0.125	0[5]	–
DIFF_SSTL15/ DIFF_SSTL15_R, 1.5V	DIFF_SSTL15, DIFF_SSTL15_R	0.75 – 0.125	0.75 + 0.125	0[5]	–
DIFF_SSTL18_I/ DIFF_SSTL18_II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	0.9 – 0.125	0.9 + 0.125	0[5]	–
LVDS_25, 2.5V	LVDS_25	1.2 – 0.125	1.2 + 0.125	0[5]	–
BLVDS_25, 2.5V	BLVDS_25	1.25 – 0.125	1.25 + 0.125	0[5]	–
MINI_LVDS_25, 2.5V	MINI_LVDS_25	1.25 – 0.125	1.25 + 0.125	0[5]	–

CLB Switching Characteristics

Table 27: **CLB Switching Characteristics**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Combinatorial Delays					
T_{ILO}	An – Dn LUT address to A.	0.11	0.13	0.13	ns, Max
T_{ILO_2}	An – Dn LUT address to AMUX/CMUX.	0.30	0.36	0.36	ns, Max
T_{ILO_3}	An – Dn LUT address to BMUX_A.	0.46	0.55	0.55	ns, Max
T_{ITO}	An – Dn inputs to A – D Q outputs.	1.05	1.27	1.27	ns, Max
T_{AXA}	AX inputs to AMUX output.	0.69	0.84	0.84	ns, Max
T_{AXB}	AX inputs to BMUX output.	0.66	0.83	0.83	ns, Max
T_{AXC}	AX inputs to CMUX output.	0.68	0.82	0.82	ns, Max
T_{AXD}	AX inputs to DMUX output.	0.75	0.90	0.90	ns, Max
T_{BXB}	BX inputs to BMUX output.	0.57	0.69	0.69	ns, Max
T_{BXD}	BX inputs to DMUX output.	0.69	0.82	0.82	ns, Max
T_{CXC}	CX inputs to CMUX output.	0.48	0.58	0.58	ns, Max
T_{CXD}	CX inputs to DMUX output.	0.59	0.71	0.71	ns, Max
T_{DXD}	DX inputs to DMUX output.	0.58	0.70	0.70	ns, Max
Sequential Delays					
T_{CKO}	Clock to AQ – DQ outputs.	0.44	0.53	0.53	ns, Max
T_{SHCKO}	Clock to AMUX – DMUX outputs.	0.53	0.66	0.66	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK					
T_{AS}/T_{AH}	AN – DN input to CLK on A – D flip-flops.	0.09/0.14	0.11/0.18	0.11/0.18	ns, Min
T_{DICK}/T_{CKDI}	AX – DX input to CLK on A – D flip-flops.	0.07/0.21	0.09/0.26	0.09/0.26	ns, Min
	AX – DX input through MUXs and/or carry logic to CLK on A – D flip-flops.	0.66/0.09	0.81/0.11	0.81/0.11	ns, Min
$T_{CECK\_CLB}/T_{CKCE\_CLB}$	CE input to CLK on A – D flip-flops.	0.17/0.00	0.21/0.01	0.21/0.01	ns, Min
T_{SRCK}/T_{CKSR}	SR input to CLK on A – D flip-flops.	0.43/0.04	0.53/0.05	0.53/0.05	ns, Min
Set/Reset					
T_{SRMIN}	SR input minimum pulse width.	0.78	1.04	1.04	ns, Min
T_{RQ}	Delay from SR input to AQ – DQ flip-flops.	0.59	0.71	0.71	ns, Max
T_{CEO}	Delay from CE input to AQ – DQ flip-flops.	0.58	0.70	0.70	ns, Max
F_{TOG}	Toggle frequency (for export control).	1286	1098	1098	MHz

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 28: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Sequential Delays					
T_{SHCKO}	Clock to A – B outputs.	1.09	1.32	1.32	ns, Max
T_{SHCKO_1}	Clock to AMUX – BMUX outputs.	1.53	1.86	1.86	ns, Max
Setup and Hold Times Before/After Clock CLK					
T_{DS_LRAM}/T_{DH_LRAM}	A – D inputs to CLK.	0.60/0.30	0.72/0.35	0.72/0.35	ns, Min
T_{AS_LRAM}/T_{AH_LRAM}	Address An inputs to clock.	0.30/0.60	0.37/0.70	0.37/0.70	ns, Min
	Address An inputs through MUXs and/or carry logic to clock.	0.77/0.21	0.94/0.26	0.94/0.26	ns, Min
T_{WS_LRAM}/T_{WH_LRAM}	WE input to clock.	0.43/0.12	0.53/0.17	0.53/0.17	ns, Min
$T_{CECK\_LRAM}/T_{CKCE\_LRAM}$	CE input to CLK.	0.44/0.11	0.53/0.17	0.53/0.17	ns, Min
Clock CLK					
T_{MPW_LRAM}	Minimum pulse width.	1.13	1.25	1.25	ns, Min
T_{MCP}	Minimum clock period.	2.26	2.50	2.50	ns, Min

Notes:

1. T_{SHCKO} also represents the CLK to XMUX output. Refer to the timing report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 29: **CLB Shift Register Switching Characteristics**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Sequential Delays					
T_{REG}	Clock to A – D outputs.	1.33	1.61	1.61	ns, Max
T_{REG_MUX}	Clock to AMUX – DMUX output.	1.77	2.15	2.15	ns, Max
T_{REG_M31}	Clock to DMUX output via M31 output.	1.23	1.46	1.46	ns, Max
Setup and Hold Times Before/After Clock CLK					
$T_{WS\_SHFREG}/ T_{WH\_SHFREG}$	WE input.	0.41/0.12	0.51/0.17	0.51/0.17	ns, Min
$T_{CECK\_SHFREG}/ T_{CKCE\_SHFREG}$	CE input to CLK.	0.42/0.11	0.52/0.17	0.52/0.17	ns, Min
$T_{DS\_SHFREG}/ T_{DH\_SHFREG}$	A – D inputs to CLK.	0.37/0.37	0.44/0.43	0.44/0.43	ns, Min
Clock CLK					
T_{MPW_SHFREG}	Minimum pulse width.	0.86	0.98	0.98	ns, Min

Table 31: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
$T_{DSPDCK\_CEM\_MREG}$/ $T_{DSPCKD\_CEM\_MREG}$	CEM input to M register CLK.	0.21/ 0.20	0.27/ 0.23	0.27/ 0.23	ns
$T_{DSPDCK\_CEP\_PREG}$/ $T_{DSPCKD\_CEP\_PREG}$	CEP input to P register CLK.	0.43/ 0.01	0.53/ 0.01	0.53/ 0.01	ns
Setup and Hold Times of the RST Pins					
$T_{DSPDCK\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$/ $T_{DSPCKD\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$	{RSTA, RSTB} input to {A, B} register CLK.	0.46/ 0.13	0.55/ 0.15	0.55/ 0.15	ns
$T_{DSPDCK\_RSTC\_CREG}$/ $T_{DSPCKD\_RSTC\_CREG}$	RSTC input to C register CLK.	0.08/ 0.11	0.09/ 0.12	0.09/ 0.12	ns
$T_{DSPDCK\_RSTD\_DREG}$/ $T_{DSPCKD\_RSTD\_DREG}$	RSTD input to D register CLK	0.50/ 0.08	0.59/ 0.09	0.59/ 0.09	ns
$T_{DSPDCK\_RSTM\_MREG}$/ $T_{DSPCKD\_RSTM\_MREG}$	RSTM input to M register CLK	0.23/ 0.24	0.27/ 0.28	0.27/ 0.28	ns
$T_{DSPDCK\_RSTP\_PREG}$/ $T_{DSPCKD\_RSTP\_PREG}$	RSTP input to P register CLK	0.30/ 0.01	0.35/ 0.01	0.35/ 0.01	ns
Combinatorial Delays from Input Pins to Output Pins					
$T_{DSPDO\_A\_CARRYOUT\_MULT}$	A input to CARRYOUT output using multiplier.	4.35	5.18	5.18	ns
$T_{DSPDO\_D\_P\_MULT}$	D input to P output using multiplier.	4.26	5.07	5.07	ns
$T_{DSPDO\_B\_P}$	B input to P output not using multiplier.	1.75	2.08	2.08	ns
$T_{DSPDO\_C\_P}$	C input to P output.	1.53	1.82	1.82	ns
Combinatorial Delays from Input Pins to Cascading Output Pins					
$T_{DSPDO\_\{A; B\}\_\{ACOUT; BCOUT\}}$	{A, B} input to {ACOUT, BCOUT} output.	0.63	0.74	0.74	ns
$T_{DSPDO\_\{A, B\}\_CARRYCASCOUT\_MULT}$	{A, B} input to CARRYCASCOUT output using multiplier.	4.65	5.54	5.54	ns
$T_{DSPDO\_D\_CARRYCASCOUT\_MULT}$	D input to CARRYCASCOUT output using multiplier.	4.54	5.40	5.40	ns
$T_{DSPDO\_\{A, B\}\_CARRYCASCOUT}$	{A, B} input to CARRYCASCOUT output not using multiplier.	2.03	2.41	2.41	ns
$T_{DSPDO\_C\_CARRYCASCOUT}$	C input to CARRYCASCOUT output.	1.81	2.15	2.15	ns
Combinatorial Delays from Cascading Input Pins to All Output Pins					
$T_{DSPDO\_ACIN\_P\_MULT}$	ACIN input to P output using multiplier.	4.19	5.00	5.00	ns
$T_{DSPDO\_ACIN\_P}$	ACIN input to P output not using multiplier.	1.57	1.88	1.88	ns
$T_{DSPDO\_ACIN\_ACOUT}$	ACIN input to ACOUT output.	0.44	0.53	0.53	ns
$T_{DSPDO\_ACIN\_CARRYCASCOUT\_MULT}$	ACIN input to CARRYCASCOUT output using multiplier.	4.47	5.33	5.33	ns
$T_{DSPDO\_ACIN\_CARRYCASCOUT}$	ACIN input to CARRYCASCOUT output not using multiplier.	1.85	2.21	2.21	ns
$T_{DSPDO\_PCIN\_P}$	PCIN input to P output.	1.28	1.52	1.52	ns

Table 31: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
$T_{DSPDO\_PCIN\_CARRYCASCOUT}$	PCIN input to CARRYCASCOUT output.	1.56	1.85	1.85	ns
Clock to Outs from Output Register Clock to Output Pins					
$T_{DSPCKO\_P\_PREG}$	CLK PREG to P output.	0.37	0.44	0.44	ns
$T_{DSPCKO\_CARRYCASCOUT\_PREG}$	CLK PREG to CARRYCASCOUT output.	0.59	0.69	0.69	ns
Clock to Outs from Pipeline Register Clock to Output Pins					
$T_{DSPCKO\_P\_MREG}$	CLK MREG to P output.	1.93	2.31	2.31	ns
$T_{DSPCKO\_CARRYCASCOUT\_MREG}$	CLK MREG to CARRYCASCOUT output.	2.21	2.64	2.64	ns
$T_{DSPCKO\_P\_ADREG\_MULT}$	CLK ADREG to P output using multiplier.	3.10	3.69	3.69	ns
$T_{DSPCKO\_CARRYCASCOUT\_ADREG\_MULT}$	CLK ADREG to CARRYCASCOUT output using multiplier.	3.38	4.02	4.02	ns
Clock to Outs from Input Register Clock to Output Pins					
$T_{DSPCKO\_P\_AREG\_MULT}$	CLK AREG to P output using multiplier.	4.51	5.37	5.37	ns
$T_{DSPCKO\_P\_BREG}$	CLK BREG to P output not using multiplier.	1.87	2.22	2.22	ns
$T_{DSPCKO\_P\_CREG}$	CLK CREG to P output not using multiplier.	1.93	2.30	2.30	ns
$T_{DSPCKO\_P\_DREG\_MULT}$	CLK DREG to P output using multiplier.	4.48	5.32	5.32	ns
Clock to Outs from Input Register Clock to Cascading Output Pins					
$T_{DSPCKO\_\{ACOUT;\ BCOUT\}\_\{AREG;\ BREG\}}$	CLK (ACOUT, BCOUT) to {A,B} register output.	0.73	0.87	0.87	ns
$T_{DSPCKO\_CARRYCASCOUT\_\{AREG,\ BREG\}\_MULT}$	CLK (AREG, BREG) to CARRYCASCOUT output using multiplier.	4.79	5.70	5.70	ns
$T_{DSPCKO\_CARRYCASCOUT\_\ BREG}$	CLK BREG to CARRYCASCOUT output not using multiplier.	2.15	2.55	2.55	ns
$T_{DSPCKO\_CARRYCASCOUT\_\ DREG\_MULT}$	CLK DREG to CARRYCASCOUT output using multiplier.	4.76	5.65	5.65	ns
$T_{DSPCKO\_CARRYCASCOUT\_\ CREG}$	CLK CREG to CARRYCASCOUT output.	2.21	2.63	2.63	ns
Maximum Frequency					
F_{MAX}	With all registers used.	550.66	464.25	464.25	MHz
F_{MAX_PATDET}	With pattern detector.	465.77	392.93	392.93	MHz
$F_{MAX\_MULT\_NOMREG}$	Two register multiply without MREG.	305.62	257.47	257.47	MHz
$F_{MAX\_MULT\_NOMREG\_PATDET}$	Two register multiply without MREG with pattern detect.	277.62	233.92	233.92	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG}$	Without ADREG.	346.26	290.44	290.44	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG\_PATDET}$	Without ADREG with pattern detect.	346.26	290.44	290.44	MHz
$F_{MAX\_NOPIPELINEREG}$	Without pipeline registers (MREG, ADREG).	227.01	190.69	190.69	MHz
$F_{MAX\_NOPIPELINEREG\_PATDET}$	Without pipeline registers (MREG, ADREG) with pattern detect.	211.15	177.43	177.43	MHz

Table 38: **PLL Specification**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
PLL_$F_{BANDWIDTH}$	Low PLL bandwidth at typical.	1.00	1.00	1.00	MHz
	High PLL bandwidth at typical.(1)	4.00	4.00	4.00	MHz
PLL_$T_{STATPHAOFFSET}$	Static phase offset of the PLL outputs.(2)	0.12	0.12	0.12	ns
PLL_$T_{OUTJITTER}$	PLL output jitter.	Note 3			
PLL_$T_{OUTDUTY}$	PLL output clock duty-cycle precision.(4)	0.20	0.20	0.20	ns
PLL_$T_{LOCKMAX}$	PLL maximum lock time.	100.00	100.00	100.00	µs
PLL_F_{OUTMAX}	PLL maximum output frequency.	800.00	800.00	800.00	MHz
PLL_F_{OUTMIN}	PLL minimum output frequency.(5)	6.25	6.25	6.25	MHz
PLL_$T_{EXTFDVAR}$	External clock feedback variation.	< 20% of clock input period or 1 ns Max			
PLL_$RST_{MINPULSE}$	Minimum reset pulse width.	5.00	5.00	5.00	ns
PLL_F_{PFDMAX}	Maximum frequency at the phase frequency detector.	500.00	450.00	450.00	MHz
PLL_F_{PFDMIN}	Minimum frequency at the phase frequency detector.	19.00	19.00	19.00	MHz
PLL_$T_{FBDELAY}$	Maximum delay in the feedback path.	3 ns Max or one CLKIN cycle			
Dynamic Reconfiguration Port (DRP) for PLL Before and After DCLK					
T_{PLLDCK_DADDR}/ T_{PLLCKD_DADDR}	Setup and hold of D address.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
T_{PLLDCK_DI}/ T_{PLLCKD_DI}	Setup and hold of D input.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
T_{PLLDCK_DEN}/ T_{PLLCKD_DEN}	Setup and hold of D enable.	1.97/0.00	2.29/0.00	2.29/0.00	ns, Min
T_{PLLDCK_DWE}/ T_{PLLCKD_DWE}	Setup and hold of D write enable.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
T_{PLLCKO_DRDY}	CLK to out of DRDY.	0.72	0.99	0.99	ns, Max
F_{DCK}	DCLK frequency.	200.00	200.00	200.00	MHz, Max

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the *Clocking Wizard* [Ref 8].
4. Includes global clock buffer.
5. Calculated as FVCO/128 assuming output duty cycle is 50%.

Device Pin-to-Pin Output Parameter Guidelines

Table 39: **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)[1]**

Symbol	Description	Device	V_{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM/PLL.						
T_{ICKOF}	Clock-capable clock input and OUTFF at pins/banks closest to the BUFGs *without* MMCM/PLL (near clock region).[2]	XC7S6	5.55	6.50	6.50	ns
		XC7S15	5.55	6.50	6.50	ns
		XC7S25	5.55	6.44	6.44	ns
		XC7S50	5.71	6.62	6.62	ns
		XC7S75	5.73	6.71	6.71	ns
		XC7S100	5.73	6.71	6.71	ns
		XA7S6	5.55	6.50	N/A	ns
		XA7S15	5.55	6.50	N/A	ns
		XA7S25	5.55	6.44	N/A	ns
		XA7S50	5.71	6.62	N/A	ns
		XA7S75	5.73	6.71	N/A	ns
		XA7S100	5.73	6.71	N/A	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Refer to the *Die Level Bank Numbering Overview* section of the *7 Series FPGA Packaging and Pinout Specification* (UG475) [Ref 4].

Table 40: **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Far Clock Region)[1]**

Symbol	Description	Device	V_{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM/PLL.						
$T_{ICKOFFAR}$	Clock-capable clock input and OUTFF at pins/banks farthest from the BUFGs *without* MMCM/PLL (far clock region).[2]	XC7S6	5.55	6.50	6.50	ns
		XC7S15	5.55	6.50	6.50	ns
		XC7S25	5.55	6.44	6.44	ns
		XC7S50	5.71	6.62	6.62	ns
		XC7S75	6.01	7.02	7.02	ns
		XC7S100	6.01	7.02	7.02	ns
		XA7S6	5.55	6.50	N/A	ns
		XA7S15	5.55	6.50	N/A	ns
		XA7S25	5.55	6.44	N/A	ns
		XA7S50	5.71	6.62	N/A	ns
		XA7S75	6.01	7.02	N/A	ns
		XA7S100	6.01	7.02	N/A	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Refer to the *Die Level Bank Numbering Overview* section of the *7 Series FPGA Packaging and Pinout Specification* (UG475) [Ref 4].

Table 41: **Clock-Capable Clock Input to Output Delay With MMCM(1)**

Symbol	Description	Device	V_{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *with* MMCM.						
$T_{ICKOFMMCMCC}$	Clock-capable clock input and OUTFF *with* MMCM.(2)	XC7S6	1.03	1.03	1.03	ns
		XC7S15	1.03	1.03	1.03	ns
		XC7S25	1.00	1.00	1.00	ns
		XC7S50	1.00	1.00	1.00	ns
		XC7S75	1.00	1.00	1.00	ns
		XC7S100	1.00	1.00	1.00	ns
		XA7S6	1.03	1.03	N/A	ns
		XA7S15	1.03	1.03	N/A	ns
		XA7S25	1.00	1.00	N/A	ns
		XA7S50	1.00	1.00	N/A	ns
		XA7S75	1.00	1.00	N/A	ns
		XA7S100	1.00	1.00	N/A	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 42: **Clock-Capable Clock Input to Output Delay With PLL(1)**

Symbol	Description	Device	V_{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *with* PLL.						
$T_{ICKOFPLLCC}$	Clock-capable clock input and OUTFF *with* PLL.(2)	XC7S6	0.85	0.85	0.85	ns
		XC7S15	0.85	0.85	0.85	ns
		XC7S25	0.83	0.83	0.83	ns
		XC7S50	0.83	0.83	0.83	ns
		XC7S75	0.83	0.83	0.83	ns
		XC7S100	0.83	0.83	0.83	ns
		XA7S6	0.85	0.85	N/A	ns
		XA7S15	0.85	0.85	N/A	ns
		XA7S25	0.83	0.83	N/A	ns
		XA7S50	0.83	0.83	N/A	ns
		XA7S75	0.83	0.83	N/A	ns
		XA7S100	0.83	0.83	N/A	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is already included in the timing calculation.

Table 43: **Pin-to-Pin, Clock-to-Out using BUFIO**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with BUFIO.					
$T_{ICKOFCS}$	Clock to out of I/O clock.	5.61	6.64	6.64	ns

Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

Table 44: **Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks**

Symbol	Description	Device	V_{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1)						
T_{PSFD}/ T_{PHFD}	Full delay (legacy delay or default delay) global clock input and IFF(2) without MMCM/PLL with ZHOLD_DELAY on HR I/O banks.	XC7S6	2.76/–0.40	3.17/–0.40	3.17/–0.40	ns
		XC7S15	2.76/–0.40	3.17/–0.40	3.17/–0.40	ns
		XC7S25	2.67/–0.37	3.12/–0.37	3.12/–0.37	ns
		XC7S50	2.66/–0.28	3.11/–0.28	3.11/–0.28	ns
		XC7S75	2.91/–0.33	3.36/–0.33	3.36/–0.33	ns
		XC7S100	2.91/–0.33	3.36/–0.33	3.36/–0.33	ns
		XA7S6	2.76/–0.40	3.17/–0.40	N/A	ns
		XA7S15	2.76/–0.40	3.17/–0.40	N/A	ns
		XA7S25	2.67/–0.37	3.12/–0.37	N/A	ns
		XA7S50	2.66/–0.28	3.11/–0.28	N/A	ns
		XA7S75	2.91/–0.33	3.36/–0.33	N/A	ns
		XA7S100	2.91/–0.33	3.36/–0.33	N/A	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch.

Table 48: **Sample Window**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
T_{SAMP}	Sampling error at receiver pins.(1)	0.64	0.70	0.70	ns
T_{SAMP_BUFIO}	Sampling error at receiver pins using BUFIO.(2)	0.40	0.46	0.46	ns

Notes:

1. This parameter indicates the total sampling error of the Spartan-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 MMCM jitter
   - MMCM accuracy (phase offset)
   - MMCM phase shift resolution

   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of the Spartan-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

XADC Specifications

The *7 Series FPGAs Overview* (DS180) [Ref 1] and *XA Spartan-7 Automotive FPGA Data Sheet: Overview* (DS171) [Ref 2] list the devices that contain a 7 series XADC dual 12-Bit 1 MSPS analog-to-digital converter.

Table 50: **XADC Specifications**

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
V_{CCADC} = 1.8V ± 5%, V_{REFP} = 1.25V, V_{REFN} = 0V, ADCCLK = 26 MHz, –55°C ≤ T_j ≤ 125°C. Typical values at T_j = +40°C.						
ADC Accuracy(1)						
Resolution			12	–	–	Bits
Integral nonlinearity(2)	INL	–40°C ≤ T_j ≤ 100°C	–	–	±2	LSBs
		–55°C ≤ T_j < –40°C; 100°C < T_j ≤ 125°C	–	–	±3	LSBs
Differential nonlinearity	DNL	No missing codes, guaranteed monotonic.	–	–	±1	LSBs
Offset error	Unipolar	–40°C ≤ T_j ≤ 100°C	–	–	±8	LSBs
		–55°C ≤ T_j < –40°C; 100°C < T_j ≤ 125°C	–	–	±12	LSBs
	Bipolar	–55°C ≤ T_j ≤ 125°C	–	–	±4	LSBs
Gain error			–	–	±0.5	%
Offset matching			–	–	4	LSBs
Gain matching			–	–	0.3	%
Sample rate			–	–	1	MS/s
Signal to noise ratio(2)	SNR	F_{SAMPLE} = 500 KS/s, F_{IN} = 20 kHz	60	–	–	dB
RMS code noise		External 1.25V reference.	–	–	2	LSBs
		On-chip reference.	–	3	–	LSBs
Total harmonic distortion(2)	THD	F_{SAMPLE} = 500 KS/s, F_{IN} = 20 kHz	70	–	–	dB
Analog Inputs(3)						
ADC input ranges		Unipolar operation.	0	–	1	V
		Bipolar operation.	–0.5	–	+0.5	V
		Unipolar common mode range (FS input).	0	–	+0.5	V
		Bipolar common mode range (FS input).	+0.5	–	+0.6	V
Maximum external channel input ranges		Adjacent analog channels set within these ranges should not corrupt measurements on adjacent channels.	–0.1	–	V_{CCADC}	V
Full-resolution bandwidth	FRBW	Auxiliary channel full resolution bandwidth.	250	–	–	kHz
On-chip Sensors						
Temperature sensor error		–40°C ≤ T_j ≤ 100°C	–	–	±4	°C
		–55°C ≤ T_j < –40°C; 100°C < T_j ≤ 125°C	–	–	±6	°C
Supply sensor error		–40°C ≤ T_j ≤ 100°C	–	–	±1	%
		–55°C ≤ T_j < –40°C; 100°C < T_j ≤ 125°C	–	–	±2	%

eFUSE Programming Conditions

Table 52 lists the programming conditions specifically for eFUSE. For more information, see the *7 Series FPGA Configuration User Guide* (UG470) [Ref 10].

Table 52: **eFUSE Programming Conditions(1)**

Symbol	Description	Min	Typ	Max	Units
I_{FS}	V_{CCAUX} supply current	–	–	115	mA
T_j	Temperature range	15	–	125	°C

Notes:

1. The FPGA must not be configured during eFUSE programming.

References

1. *7 Series FPGAs Overview* (DS180)
2. *XA Spartan-7 Automotive FPGA Data Sheet: Overview* (DS171)
3. *7 Series FPGAs SelectIO Resources User Guide* (UG471)
4. *7 Series FPGA Packaging and Pinout Specification* (UG475)
5. *7 Series FPGAs PCB Design Guide* (UG483)
6. *Xilinx Power Estimator* spreadsheet tool (XPE)
7. *Zynq-7000 AP SoC and 7 Series FPGAs Memory Interface Solutions User Guide* (UG586)
8. See the Clocking Wizard in Vivado software.
9. *7 Series FPGAs and Zynq-7000 AP SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480)
10. *7 Series FPGA Configuration User Guide* (UG470)

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
07/31/2018	1.7	In Table 12, updated Vivado tools version to 2018.2.1. In Table 13, moved all speed grades for all devices to Production. In Table 14, added Vivado tools version for XC7S6, XC7S15, XC7S75, XC7S100, XA7S6, XA7S15, XA7S75, and XA7S100.
06/18/2018	1.6	In Table 12, updated Vivado tools version to 2018.2. In Table 13, moved all speed grades except -1Q (1.0V) for XC7S6 and XC7S15 to Production. In Table 14, added Vivado tools version for XC7S6 and XC7S15.
04/04/2018	1.5	Added XA7S6, XA7S15, XA7S25, XA7S75, and XA7S100 devices throughout. In Table 5, updated typical quiescent supply current values for XC7S25 and XC7S50 devices, and added values for XC7S6, XC7S15, XC7S75, and XC7S100 devices. In Table 6, updated table title and $I_{CCINTMIN}$ and $I_{CCAUXMIN}$ for XC7S75 and XC7S100 devices. In Table 13, moved all speed grades for XC7S6 and XC7S15 to Preliminary, moved -1LI (0.95V) speed grade for XC7S25 to Production, and moved all speed grades except -1Q (1.0V) for XC7S75 and XC7S100 from Preliminary to Production. In Table 14, added Vivado tools version for XC7S25, XC7S75, and XC7S100. In Table 36, Table 39, Table 40, Table 41, Table 42, Table 44, Table 45, and Table 46, changed parameter value for XA7S50 to N/A. In Table 49, added package skew values for XC7S6 and XC7S15 devices.
12/22/2017	1.4	In Table 12, updated Vivado tools version to 2017.4. In Table 13, moved all speed grades for XC7S75 and XC7S100 from Advance to Preliminary and all speed grades except -1LI (0.95V) for XC7S25 from Advance to Production. In Table 14, added Vivado tools version for XC7S25. Added Note 2 to Table 16. In Table 49, added package skew values for XC7S25 device in CSGA324 package and XC7S75 and XC7S100 devices in FGGA676 package.
11/20/2017	1.3	Added XA7S50 device throughout. Updated description of offered temperature ranges in second paragraph of Introduction. Added row for junction temperature (T_j) at expanded (Q) temperature to Table 2. Added -1Q (1.0V) speed grade to Table 5, and Table 13 to Table 16. In Table 12, updated Vivado tools version to 2017.3. In Table 49, added package skew values for XC7S25, XC7S50, XC7S75, and XC7S100 devices in CSGA225, FTGB196, and FGGA484 packages. Added *XA Spartan-7 Automotive FPGA Data Sheet: Overview* (DS171) to References.
06/20/2017	1.2	Updated paragraph before Table 6. In Table 12, updated Vivado tools version to 2017.2. In Table 13, moved all speed grades for XC7S50 from Preliminary to Production and updated Note 1. In Table 14, added Vivado tools version for XC7S50. In Table 49, added package skew value for XC7S50 device in FGGA484 package.
04/07/2017	1.1	Added 1.35V to Note 5 in Table 2. In Table 12, updated Vivado tools version to 2016.4. In Table 13, moved all speed grades for XC7S50 from Advance to Preliminary. Removed SFI-4.1 and SPI-4.2 from descriptions of SDR LVDS receiver and DDR LVDS receiver, respectively, in Table 15. In Table 25, changed $T_{IDELAYRESOLUTION}$ units from ps to µs. Removed BUFMR from Note 1 in Table 34. In Table 49, replaced TQGA144 with FTGB196 for XC7S6, XC7S15, and XC7S25 devices, added FTGB196 package for XC7S50 device, and added package skew value for XC7S50 device in CSGA324 package.
09/27/2016	1.0	Initial Xilinx release.

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