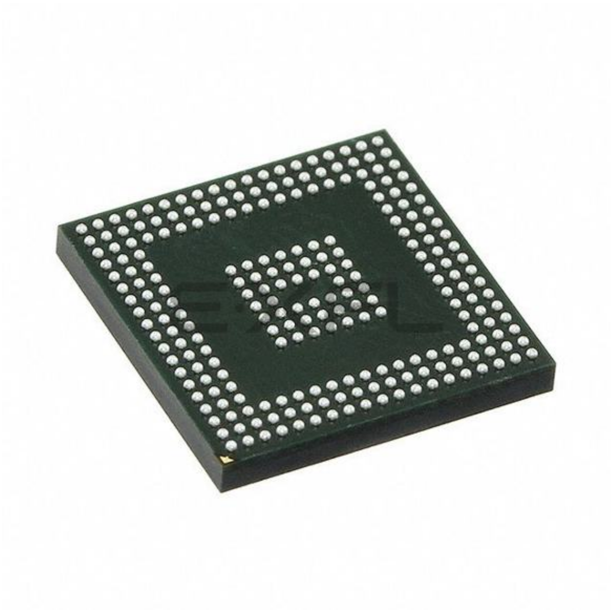
AMD Xilinx - XC7S50-1CSGA324Q Datasheet



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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	4075
Number of Logic Elements/Cells	52160
Total RAM Bits	2764800
Number of I/O	-
Number of Gates	-
Voltage - Supply	0.95V ~ 1.05V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TJ)
Package / Case	324-LFBGA, CSPBGA
Supplier Device Package	324-CSGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7s50-1csga324q

Table 4: **V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for HR I/O Banks[(1)(2)]**

AC Voltage Overshoot	% of UI at –40°C to 125°C	AC Voltage Undershoot	% of UI at –40°C to 125°C
V_{CCO} + 0.55	100	–0.40	100
		–0.45	61.7
		–0.50	25.8
		–0.55	11.0
V_{CCO} + 0.60	46.6	–0.60	4.77
V_{CCO} + 0.65	21.2	–0.65	2.10
V_{CCO} + 0.70	9.75	–0.70	0.94
V_{CCO} + 0.75	4.55	–0.75	0.43
V_{CCO} + 0.80	2.15	–0.80	0.20
V_{CCO} + 0.85	1.02	–0.85	0.09
V_{CCO} + 0.90	0.49	–0.90	0.04
V_{CCO} + 0.95	0.24	–0.95	0.02

Notes:

1. A total of 200 mA per bank should not be exceeded.
2. The peak voltage of the overshoot or undershoot, and the duration above V_{CCO} + 0.20V or below GND – 0.20V, must not exceed the values in this table.

Table 5: **Typical Quiescent Supply Current[(1)(2)(3)]**

Symbol	Description	Device	Speed Grade						Units
			1.0V					0.95V	
			-2C	-2I	-1C	-1I	-1Q	-1LI	
I_{CCINTQ}	Quiescent V_{CCINT} supply current.	XC7S6	36	36	36	36	36	32	mA
		XC7S15	36	36	36	36	36	32	mA
		XC7S25	48	48	48	48	48	43	mA
		XC7S50	95	95	95	95	95	59	mA
		XC7S75	148	148	148	148	148	134	mA
		XC7S100	148	148	148	148	148	134	mA
		XA7S6	N/A	36	N/A	36	36	N/A	mA
		XA7S15	N/A	36	N/A	36	36	N/A	mA
		XA7S25	N/A	48	N/A	48	48	N/A	mA
		XA7S50	N/A	95	N/A	95	95	N/A	mA
		XA7S75	N/A	148	N/A	148	148	N/A	mA
		XA7S100	N/A	148	N/A	148	148	N/A	mA

Table 5: **Typical Quiescent Supply Current[1][2][3]** ***(Cont'd)***

Symbol	Description	Device	Speed Grade						Units
			1.0V					0.95V	
			-2C	-2I	-1C	-1I	-1Q	-1LI	
I_{CCOQ}	Quiescent V_{CCO} supply current.	XC7S6	1	1	1	1	1	1	mA
		XC7S15	1	1	1	1	1	1	mA
		XC7S25	1	1	1	1	1	1	mA
		XC7S50	1	1	1	1	1	1	mA
		XC7S75	4	4	4	4	4	4	mA
		XC7S100	4	4	4	4	4	4	mA
		XA7S6	N/A	1	N/A	1	1	N/A	mA
		XA7S15	N/A	1	N/A	1	1	N/A	mA
		XA7S25	N/A	1	N/A	1	1	N/A	mA
		XA7S50	N/A	1	N/A	1	1	N/A	mA
		XA7S75	N/A	4	N/A	4	4	N/A	mA
		XA7S100	N/A	4	N/A	4	4	N/A	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current.	XC7S6	10	10	10	10	10	10	mA
		XC7S15	10	10	10	10	10	10	mA
		XC7S25	13	13	13	13	13	13	mA
		XC7S50	22	22	22	22	22	20	mA
		XC7S75	43	43	43	43	43	43	mA
		XC7S100	43	43	43	43	43	43	mA
		XA7S6	N/A	10	N/A	10	10	N/A	mA
		XA7S15	N/A	10	N/A	10	10	N/A	mA
		XA7S25	N/A	13	N/A	13	13	N/A	mA
		XA7S50	N/A	22	N/A	22	22	N/A	mA
		XA7S75	N/A	43	N/A	43	43	N/A	mA
		XA7S100	N/A	43	N/A	43	43	N/A	mA

Table 5: **Typical Quiescent Supply Current[(1)(2)(3)] *(Cont'd)***

Symbol	Description	Device	Speed Grade						Units
			1.0V					0.95V	
			-2C	-2I	-1C	-1I	-1Q	-1LI	
$I_{CCBRAMQ}$	Quiescent V_{CCBRAM} supply current.	XC7S6	1	1	1	1	1	1	mA
		XC7S15	1	1	1	1	1	1	mA
		XC7S25	1	1	1	1	1	1	mA
		XC7S50	2	2	2	2	2	1	mA
		XC7S75	9	9	9	9	9	8	mA
		XC7S100	9	9	9	9	9	8	mA
		XA7S6	N/A	1	N/A	1	1	N/A	mA
		XA7S15	N/A	1	N/A	1	1	N/A	mA
		XA7S25	N/A	1	N/A	1	1	N/A	mA
		XA7S50	N/A	2	N/A	2	2	N/A	mA
		XA7S75	N/A	9	N/A	9	9	N/A	mA
		XA7S100	N/A	9	N/A	9	9	N/A	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperature (T_j) with single-ended SelectIO™ resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the *Xilinx Power Estimator* spreadsheet tool [Ref 6] to estimate static power consumption for conditions other than those specified.

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCBRAM} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If V_{CCAUX} and V_{CCO} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously.

For V_{CCO} voltages of 3.3V in HR I/O banks and configuration bank 0 the following conditions apply.

- The voltage difference between V_{CCO} and V_{CCAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

There is no recommended sequence for supplies not discussed in this section.

Table 9: **Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM}[(1)]			V_{ID}[(2)]			V_{OCM}[(3)]			V_{OD}[(4)]		
	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max
BLVDS_25	0.300	1.200	1.425	0.100	–	–	–	1.250	–	Note 5		
MINI_LVDS_25	0.300	1.200	V_{CCAUX}	0.200	0.400	0.600	1.000	1.200	1.400	0.300	0.450	0.600
PPDS_25	0.200	0.900	V_{CCAUX}	0.100	0.250	0.400	0.500	0.950	1.400	0.100	0.250	0.400
RSDS_25	0.300	0.900	1.500	0.100	0.350	0.600	1.000	1.200	1.400	0.100	0.350	0.600
TMDS_33	2.700	2.965	3.230	0.150	0.675	1.200	V_{CCO} – 0.405	V_{CCO} – 0.300	V_{CCO} – 0.190	0.400	0.600	0.800

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage ($Q - \overline{Q}$).
3. V_{OCM} is the output common mode voltage.
4. V_{OD} is the output differential voltage ($Q - \overline{Q}$).
5. V_{OD} for BLVDS will vary significantly depending on topology and loading.

Table 10: **Complementary Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM}[(1)]			V_{ID}[(2)]		V_{OL}[(3)]	V_{OH}[(4)]	I_{OL}	I_{OH}
	V, Min	V, Typ	V, Max	V, Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
DIFF_HSTL_I	0.300	0.750	1.125	0.100	–	0.400	V_{CCO} – 0.400	8.00	–8.00
DIFF_HSTL_I_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO} – 0.400	8.00	–8.00
DIFF_HSTL_II	0.300	0.750	1.125	0.100	–	0.400	V_{CCO} – 0.400	16.00	–16.00
DIFF_HSTL_II_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO} – 0.400	16.00	–16.00
DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% V_{CCO}	80% V_{CCO}	0.100	–0.100
DIFF_MOBILE_DDR	0.300	0.900	1.425	0.100	–	10% V_{CCO}	90% V_{CCO}	0.100	–0.100
DIFF_SSTL135	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	13.0	–13.0
DIFF_SSTL135_R	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	8.9	–8.9
DIFF_SSTL15	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	13.0	–13.0
DIFF_SSTL15_R	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	8.9	–8.9
DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.470	(V_{CCO}/2) + 0.470	8.00	–8.00
DIFF_SSTL18_II	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.600	(V_{CCO}/2) + 0.600	13.4	–13.4

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage ($Q - \overline{Q}$).
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

Table 14: **Spartan-7 Device Production Software and Speed Specification Release**

Device	V_{CCINT} Operating Voltage, Speed Grade, and Temperature Range					
	1.0V					0.95V
	-2C	-2I	-1C	-1I	-1Q	-1LI
XC7S6	Vivado tools 2018.2 v1.22				Vivado tools 2018.2.1 v1.23	Vivado tools 2018.2 v1.22
XC7S15	Vivado tools 2018.2 v1.22				Vivado tools 2018.2.1 v1.23	Vivado tools 2018.2 v1.22
XC7S25	Vivado tools 2017.4 v1.20				Vivado tools 2018.1 v1.21	Vivado tools 2017.4 v1.20
XC7S50	Vivado tools 2017.2 v1.17				Vivado tools 2017.3 v1.19	Vivado tools 2017.2 v1.17
XC7S75	Vivado tools 2018.1 v1.21				Vivado tools 2018.2.1 v1.23	Vivado tools 2018.1 v1.21
XC7S100	Vivado tools 2018.1 v1.21				Vivado tools 2018.2.1 v1.23	Vivado tools 2018.1 v1.21
XA7S6	N/A	Vivado tools 2018.2.1 v1.16	N/A	Vivado tools 2018.2.1 v1.16		N/A
XA7S15	N/A	Vivado tools 2018.2.1 v1.16	N/A	Vivado tools 2018.2.1 v1.16		N/A
XA7S25	N/A	Vivado tools 2018.1 v1.15	N/A	Vivado tools 2018.1 v1.15		N/A
XA7S50	N/A	Vivado tools 2017.3 v1.12	N/A	Vivado tools 2017.3 v1.12		N/A
XA7S75	N/A	Vivado tools 2018.2.1 v1.16	N/A	Vivado tools 2018.2.1 v1.16		N/A
XA7S100	N/A	Vivado tools 2018.2.1 v1.16	N/A	Vivado tools 2018.2.1 v1.16		N/A

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Spartan-7 FPGAs. These values are subject to the same guidelines as the AC Switching Characteristics, page 12.

Table 15: **Networking Applications Interface Performances**

Description	V_{CCINT} Operating Voltage, Speed Grade, and Temperature Range			Units
	1.0V		0.95V	
	-2C/-2I	-1C/-1I/-1Q	-1LI	
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	680	600	600	Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14)	1250	950	950	Mb/s
SDR LVDS receiver[(1)]	680	600	600	Mb/s

Table 15: **Networking Applications Interface Performances *(Cont'd)***

Description	V_{CCINT} Operating Voltage, Speed Grade, and Temperature Range			Units
	1.0V		0.95V	
	-2C/-2I	-1C/-1I/-1Q	-1LI	
DDR LVDS receiver[1]	1250	950	950	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

Table 16: **Maximum Physical Interface (PHY) Rate for Memory Interface IP available with the Memory Interface Generator[1]**

Memory Standard	V_{CCINT} Operating Voltage, Speed Grade, and Temperature Range			Units
	1.0V		0.95V	
	-2C/-2I	-1C/-1I/-1Q	-1LI	
4:1 Memory Controllers				
DDR3	800[2]	667	667	Mb/s
DDR3L	800[2]	667	667	Mb/s
DDR2	800[2]	667	667	Mb/s
2:1 Memory Controllers				
DDR3	800[2]	667	667	Mb/s
DDR3L	800[2]	667	667	Mb/s
DDR2	800[2]	667	667	Mb/s
LPDDR2	667	533	533	Mb/s

Notes:

1. V_{REF} tracking is required. For more information, see the *Zynq-7000 AP SoC and 7 Series FPGAs Memory Interface Solutions User Guide* (UG586) [Ref 7].
2. The maximum PHY rate is 667 Mb/s in the FTGB196 package.

IOB Pad Input/Output/3-State

Table 17 summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HR I/O banks, the IN_TERM termination turn-on time is always faster than T_{IOTP} when the INTERMDISABLE pin is used.

Table 17: **IOB High Range (HR) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}			T_{IOOP}			T_{IOTP}			Units
	V_{CCINT} Operating Voltage and Speed Grade									
	1.0V		0.95V	1.0V		0.95V	1.0V		0.95V	
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
LVCMOS15_F8	0.86	0.93	0.93	1.72	1.98	1.98	1.75	1.99	1.99	ns
LVCMOS15_F12	0.86	0.93	0.93	1.47	1.73	1.73	1.50	1.74	1.74	ns
LVCMOS15_F16	0.86	0.93	0.93	1.46	1.71	1.71	1.49	1.73	1.73	ns
LVCMOS12_S4	0.95	1.02	1.02	2.69	2.95	2.95	2.72	2.96	2.96	ns
LVCMOS12_S8	0.95	1.02	1.02	2.21	2.46	2.46	2.24	2.48	2.48	ns
LVCMOS12_S12	0.95	1.02	1.02	1.91	2.17	2.17	1.94	2.18	2.18	ns
LVCMOS12_F4	0.95	1.02	1.02	2.10	2.35	2.35	2.13	2.37	2.37	ns
LVCMOS12_F8	0.95	1.02	1.02	1.66	1.92	1.92	1.69	1.93	1.93	ns
LVCMOS12_F12	0.95	1.02	1.02	1.51	1.76	1.76	1.54	1.77	1.77	ns
SSTL135_S	0.75	0.82	0.82	1.47	1.73	1.73	1.50	1.74	1.74	ns
SSTL15_S	0.68	0.75	0.75	1.43	1.68	1.68	1.46	1.69	1.69	ns
SSTL18_I_S	0.75	0.82	0.82	1.79	2.04	2.04	1.82	2.06	2.06	ns
SSTL18_II_S	0.75	0.82	0.82	1.43	1.68	1.68	1.46	1.70	1.70	ns
DIFF_SSTL135_S	0.76	0.83	0.83	1.47	1.73	1.73	1.50	1.74	1.74	ns
DIFF_SSTL15_S	0.76	0.83	0.83	1.43	1.68	1.68	1.46	1.69	1.69	ns
DIFF_SSTL18_I_S	0.79	0.86	0.86	1.80	2.06	2.06	1.83	2.07	2.07	ns
DIFF_SSTL18_II_S	0.79	0.86	0.86	1.51	1.76	1.76	1.54	1.77	1.77	ns
SSTL135_F	0.75	0.82	0.82	1.24	1.49	1.49	1.27	1.51	1.51	ns
SSTL15_F	0.68	0.75	0.75	1.19	1.45	1.45	1.22	1.46	1.46	ns
SSTL18_I_F	0.75	0.82	0.82	1.24	1.49	1.49	1.27	1.51	1.51	ns
SSTL18_II_F	0.75	0.82	0.82	1.24	1.49	1.49	1.27	1.51	1.51	ns
DIFF_SSTL135_F	0.76	0.83	0.83	1.24	1.49	1.49	1.27	1.51	1.51	ns
DIFF_SSTL15_F	0.76	0.83	0.83	1.19	1.45	1.45	1.22	1.46	1.46	ns
DIFF_SSTL18_I_F	0.79	0.86	0.86	1.35	1.60	1.60	1.38	1.62	1.62	ns
DIFF_SSTL18_II_F	0.79	0.86	0.86	1.33	1.59	1.59	1.36	1.60	1.60	ns

Table 18 specifies the values of T_{IOTPHZ} and $T_{IOIBUFDISABLE}$. T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). $T_{IOIBUFDISABLE}$ is described as the IOB delay from IBUFDISABLE to O output. In HR I/O banks, the internal IN_TERM termination turn-off time is always faster than T_{IOTPHZ} when the INTERMDISABLE pin is used.

I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

Table 19 shows the test setup parameters used for measuring input delay.

Table 19: **Input Delay Measurement Methodology**

Description	I/O Standard Attribute	V_L (1)	V_H (1)	V_{MEAS} (3)(5)	V_{REF} (2)(4)
LVCMOS, 1.2V	LVCMOS12	0.1	1.1	0.6	–
LVCMOS, 1.5V	LVCMOS15	0.1	1.4	0.75	–
LVCMOS, 1.8V	LVCMOS18	0.1	1.7	0.9	–
LVCMOS, 2.5V	LVCMOS25	0.1	2.4	1.25	–
LVCMOS, 3.3V	LVCMOS33	0.1	3.2	1.65	–
LVTTL, 3.3V	LVTTL	0.1	3.2	1.65	–
MOBILE_DDR, 1.8V	MOBILE_DDR	0.1	1.7	0.9	–
PCI33, 3.3V	PCI33_3	0.1	3.2	1.65	–
HSTL (high-speed transceiver logic), Class I, 1.2V	HSTL_I_12	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.60
HSTL, Class I & II, 1.5V	HSTL_I, HSTL_II	V_{REF} – 0.65	V_{REF} + 0.65	V_{REF}	0.75
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	V_{REF} – 0.8	V_{REF} + 0.8	V_{REF}	0.90
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.60
SSTL (stub-terminated transceiver logic), 1.2V	SSTL12	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.60
SSTL, 1.35V	SSTL135, SSTL135_R	V_{REF} – 0.575	V_{REF} + 0.575	V_{REF}	0.675
SSTL, 1.5V	SSTL15, SSTL15_R	V_{REF} – 0.65	V_{REF} + 0.65	V_{REF}	0.75
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	V_{REF} – 0.8	V_{REF} + 0.8	V_{REF}	0.90
DIFF_MOBILE_DDR, 1.8V	DIFF_MOBILE_DDR	0.9 – 0.125	0.9 + 0.125	0(5)	–
DIFF_HSTL, Class I, 1.2V	DIFF_HSTL_I_12	0.6 – 0.125	0.6 + 0.125	0(5)	–
DIFF_HSTL, Class I & II,1.5V	DIFF_HSTL_I, DIFF_HSTL_II	0.75 – 0.125	0.75 + 0.125	0(5)	–
DIFF_HSTL, Class I & II, 1.8V	DIFF_HSTL_I_18, DIFF_HSTL_II_18	0.9 – 0.125	0.9 + 0.125	0(5)	–
DIFF_HSUL, 1.2V	DIFF_HSUL_12	0.6 – 0.125	0.6 + 0.125	0(5)	–
DIFF_SSTL135/ DIFF_SSTL135_R, 1.35V	DIFF_SSTL135, DIFF_SSTL135_R	0.675 – 0.125	0.675 + 0.125	0(5)	–
DIFF_SSTL15/ DIFF_SSTL15_R, 1.5V	DIFF_SSTL15, DIFF_SSTL15_R	0.75 – 0.125	0.75 + 0.125	0(5)	–
DIFF_SSTL18_I/ DIFF_SSTL18_II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	0.9 – 0.125	0.9 + 0.125	0(5)	–
LVDS_25, 2.5V	LVDS_25	1.2 – 0.125	1.2 + 0.125	0(5)	–
BLVDS_25, 2.5V	BLVDS_25	1.25 – 0.125	1.25 + 0.125	0(5)	–
MINI_LVDS_25, 2.5V	MINI_LVDS_25	1.25 – 0.125	1.25 + 0.125	0(5)	–

Table 19: **Input Delay Measurement Methodology *(Cont'd)***

Description	I/O Standard Attribute	V_L[(1)]	V_H[(1)]	V_{MEAS}[(3)(5)]	V_{REF}[(2)(4)]
PPDS_25	PPDS_25	1.25 – 0.125	1.25 + 0.125	0[(5)]	–
RSDS_25	RSDS_25	1.25 – 0.125	1.25 + 0.125	0[(5)]	–
TMDS_33	TMDS_33	3 – 0.125	3 + 0.125	0[(5)]	–

Notes:

1. Input waveform switches between V_L and V_H.
2. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
3. Input voltage level from which measurement starts.
4. This is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 1.
5. The value given is the differential input voltage.

Table 22: **OLOGIC Switching Characteristics**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Setup/Hold					
T_{ODCK}/T_{OCKD}	D1/D2 pins setup/hold with respect to CLK.	0.71/–0.11	0.84/–0.11	0.84/–0.11	ns
T_{OOCECK}/T_{OCKOCE}	OCE pin setup/hold with respect to CLK.	0.34/0.58	0.51/0.58	0.51/0.58	ns
T_{OSRCK}/T_{OCKSR}	SR pin setup/hold with respect to CLK.	0.44/0.21	0.80/0.21	0.80/0.21	ns
T_{OTCK}/T_{OCKT}	T1/T2 pins setup/hold with respect to CLK.	0.73/–0.14	0.89/–0.14	0.89/–0.14	ns
T_{OTCECK}/T_{OCKTCE}	TCE pin setup/hold with respect to CLK.	0.34/0.01	0.51/0.01	0.51/0.01	ns
Combinatorial					
T_{ODQ}	D1 to OQ out or T1 to TQ out.	0.96	1.16	1.16	ns
Sequential Delays					
T_{OCKQ}	CLK to OQ/TQ out.	0.49	0.56	0.56	ns
T_{RQ_OLOGIC}	SR pin to OQ/TQ out.	0.80	0.95	0.95	ns
T_{GSRQ_OLOGIC}	Global set/reset to Q outputs.	7.60	10.51	10.51	ns
Set/Reset					
T_{RPW_OLOGIC}	Minimum pulse width, SR inputs.	0.74	0.74	0.74	ns, Min

Input/Output Delay Switching Characteristics

Table 25: **Input/Output Delay Switching Characteristics**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
IDELAYCTRL					
T_{DLYCCO_RDY}	Reset to ready for IDELAYCTRL.	3.67	3.67	3.67	µs
$F_{IDELAYCTRL\_REF}$	Attribute REFCLK frequency = 200.00.[1]	200.00	200.00	200.00	MHz
	Attribute REFCLK frequency = 300.00.[1]	300.00	300.00	300.00	MHz
	Attribute REFCLK frequency = 400.00.[1]	400.00	N/A	N/A	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	±10	MHz
$T_{IDELAYCTRL\_RPW}$	Minimum reset pulse width.	59.28	59.28	59.28	ns
IDELAY					
$T_{IDELAYRESOLUTION}$	IDELAY chain delay resolution.	1/(32 x 2 x F_{REF})			µs
$T_{IDELAYPAT\_JIT}$	Pattern dependent period jitter in delay chain for clock pattern.[2]	0	0	0	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23).[3]	±5	±5	±5	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23).[4]	±9	±9	±9	ps per tap
$T_{IDELAY\_CLK\_MAX}$	Maximum frequency of CLK input to IDELAY.	680.00	600.00	600.00	MHz
T_{IDCCK_CE} / T_{IDCKC_CE}	CE pin setup/hold with respect to C for IDELAY.	0.16/0.13	0.21/0.16	0.21/0.16	ns
T_{IDCCK_INC}/ T_{IDCKC_INC}	INC pin setup/hold with respect to C for IDELAY.	0.14/0.18	0.16/0.22	0.16/0.22	ns
T_{IDCCK_RST}/ T_{IDCKC_RST}	RST pin setup/hold with respect to C for IDELAY.	0.16/0.11	0.18/0.14	0.18/0.14	ns
$T_{IDDO\_IDATAIN}$	Propagation delay through IDELAY.	Note 5	Note 5	Note 5	ps

Notes:

1. Average tap delay at 200 MHz = 78 ps, at 300 MHz = 52 ps, and at 400 MHz = 39 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE.
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY tap setting. See the timing report for actual values.

Block RAM and FIFO Switching Characteristics

Table 30: **Block RAM and FIFO Switching Characteristics**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Block RAM and FIFO Clock-to-Out Delays					
T_{RCKO_DO} and $T_{RCKO\_DO\_REG}$	Clock CLK to DOUT output (without output register).[1][2]	2.13	2.46	2.46	ns, Max
	Clock CLK to DOUT output (with output register).[3][4]	0.74	0.89	0.89	ns, Max
$T_{RCKO\_DO\_ECC}$ and $T_{RCKO\_DO\_ECC\_REG}$	Clock CLK to DOUT output with ECC (without output register).[1][2]	3.04	3.84	3.84	ns, Max
	Clock CLK to DOUT output with ECC (with output register).[3][4]	0.81	0.94	0.94	ns, Max
$T_{RCKO\_DO\_CASCOUT}$ and $T_{RCKO\_DO\_CASCOUT\_REG}$	Clock CLK to DOUT output with cascade (without output register).[1]	2.88	3.30	3.30	ns, Max
	Clock CLK to DOUT output with cascade (with output register).[3]	1.28	1.46	1.46	ns, Max
T_{RCKO_FLAGS}	Clock CLK to FIFO flags outputs.[5]	0.87	1.05	1.05	ns, Max
$T_{RCKO\_POINTERS}$	Clock CLK to FIFO pointers outputs.[6]	1.02	1.15	1.15	ns, Max
$T_{RCKO\_PARITY\_ECC}$	Clock CLK to ECCPARITY in ECC encode only mode.	0.85	0.94	0.94	ns, Max
$T_{RCKO\_SDBIT\_ECC}$ and $T_{RCKO\_SDBIT\_ECC\_REG}$	Clock CLK to BITERR (without output register).	2.81	3.55	3.55	ns, Max
	Clock CLK to BITERR (with output register).	0.76	0.89	0.89	ns, Max
$T_{RCKO\_RDADDR\_ECC}$ and $T_{RCKO\_RDADDR\_ECC\_REG}$	Clock CLK to RDADDR output with ECC (without output register).	0.88	1.07	1.07	ns, Max
	Clock CLK to RDADDR output with ECC (with output register).	0.93	1.08	1.08	ns, Max
Setup and Hold Times Before/After Clock CLK					
T_{RCCK_ADDRA}/ T_{RCKC_ADDRA}	ADDR inputs.[7]	0.49/0.33	0.57/0.36	0.57/0.36	ns, Min
$T_{RDCK\_DI\_WF\_NC}$/ $T_{RCKD\_DI\_WF\_NC}$	Data input setup/hold time when block RAM is configured in WRITE_FIRST or NO_CHANGE mode.[8]	0.65/0.63	0.74/0.67	0.74/0.67	ns, Min
$T_{RDCK\_DI\_RF}$/ $T_{RCKD\_DI\_RF}$	Data input setup/hold time when block RAM is configured in READ_FIRST mode.[8]	0.22/0.34	0.25/0.41	0.25/0.41	ns, Min
$T_{RDCK\_DI\_ECC}$/ $T_{RCKD\_DI\_ECC}$	DIN inputs with block RAM ECC in standard mode.[8]	0.55/0.46	0.63/0.50	0.63/0.50	ns, Min
$T_{RDCK\_DI\_ECCW}$/ $T_{RCKD\_DI\_ECCW}$	DIN inputs with block RAM ECC encode only.[8]	1.02/0.46	1.17/0.50	1.17/0.50	ns, Min

Table 30: **Block RAM and FIFO Switching Characteristics *(Cont'd)***

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
$F_{MAX\_CAS\_RF\_DELAYED\_WRITE}$	When in cascade RF mode and there is a possibility of address overlap between port A and port B.	362.19	297.35	297.35	MHz
F_{MAX_FIFO}	FIFO in all modes without ECC.	460.83	388.20	388.20	MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration.	365.10	297.53	297.53	MHz

Notes:

1. T_{RCKO_DOR} includes T_{RCKO_DOW}, T_{RCKO_DOPR}, and T_{RCKO_DOPW} as well as the B port equivalent timing parameters.
2. These parameters also apply to synchronous FIFO with DO_REG = 0.
3. T_{RCKO_DO} includes T_{RCKO_DOP} as well as the B port equivalent timing parameters.
4. These parameters also apply to multi-rate (asynchronous) and synchronous FIFO with DO_REG = 1.
5. T_{RCKO_FLAGS} includes the following parameters: T_{RCKO_AEMPTY}, T_{RCKO_AFULL}, T_{RCKO_EMPTY}, T_{RCKO_FULL}, T_{RCKO_RDERR}, T_{RCKO_WRERR}.
6. $T_{RCKO\_POINTERS}$ includes both $T_{RCKO\_RDCOUNT}$ and $T_{RCKO\_WRCOUNT}$.
7. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
8. These parameters include both A and B inputs as well as the parity inputs of A and B.
9. T_{RCO_FLAGS} includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
10. RDEN and WREN must be held Low prior to and during reset. The FIFO reset must be asserted for at least five positive clock edges of the slowest clock (WRCLK or RDCLK).

Table 31: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
$T_{DSPDCK\_CEM\_MREG}$/ $T_{DSPCKD\_CEM\_MREG}$	CEM input to M register CLK.	0.21/ 0.20	0.27/ 0.23	0.27/ 0.23	ns
$T_{DSPDCK\_CEP\_PREG}$/ $T_{DSPCKD\_CEP\_PREG}$	CEP input to P register CLK.	0.43/ 0.01	0.53/ 0.01	0.53/ 0.01	ns
Setup and Hold Times of the RST Pins					
$T_{DSPDCK\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$/ $T_{DSPCKD\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$	{RSTA, RSTB} input to {A, B} register CLK.	0.46/ 0.13	0.55/ 0.15	0.55/ 0.15	ns
$T_{DSPDCK\_RSTC\_CREG}$/ $T_{DSPCKD\_RSTC\_CREG}$	RSTC input to C register CLK.	0.08/ 0.11	0.09/ 0.12	0.09/ 0.12	ns
$T_{DSPDCK\_RSTD\_DREG}$/ $T_{DSPCKD\_RSTD\_DREG}$	RSTD input to D register CLK	0.50/ 0.08	0.59/ 0.09	0.59/ 0.09	ns
$T_{DSPDCK\_RSTM\_MREG}$/ $T_{DSPCKD\_RSTM\_MREG}$	RSTM input to M register CLK	0.23/ 0.24	0.27/ 0.28	0.27/ 0.28	ns
$T_{DSPDCK\_RSTP\_PREG}$/ $T_{DSPCKD\_RSTP\_PREG}$	RSTP input to P register CLK	0.30/ 0.01	0.35/ 0.01	0.35/ 0.01	ns
Combinatorial Delays from Input Pins to Output Pins					
$T_{DSPDO\_A\_CARRYOUT\_MULT}$	A input to CARRYOUT output using multiplier.	4.35	5.18	5.18	ns
$T_{DSPDO\_D\_P\_MULT}$	D input to P output using multiplier.	4.26	5.07	5.07	ns
$T_{DSPDO\_B\_P}$	B input to P output not using multiplier.	1.75	2.08	2.08	ns
$T_{DSPDO\_C\_P}$	C input to P output.	1.53	1.82	1.82	ns
Combinatorial Delays from Input Pins to Cascading Output Pins					
$T_{DSPDO\_\{A; B\}\_\{ACOUT; BCOUT\}}$	{A, B} input to {ACOUT, BCOUT} output.	0.63	0.74	0.74	ns
$T_{DSPDO\_\{A, B\}\_CARRYCASCOUT\_MULT}$	{A, B} input to CARRYCASCOUT output using multiplier.	4.65	5.54	5.54	ns
$T_{DSPDO\_D\_CARRYCASCOUT\_MULT}$	D input to CARRYCASCOUT output using multiplier.	4.54	5.40	5.40	ns
$T_{DSPDO\_\{A, B\}\_CARRYCASCOUT}$	{A, B} input to CARRYCASCOUT output not using multiplier.	2.03	2.41	2.41	ns
$T_{DSPDO\_C\_CARRYCASCOUT}$	C input to CARRYCASCOUT output.	1.81	2.15	2.15	ns
Combinatorial Delays from Cascading Input Pins to All Output Pins					
$T_{DSPDO\_ACIN\_P\_MULT}$	ACIN input to P output using multiplier.	4.19	5.00	5.00	ns
$T_{DSPDO\_ACIN\_P}$	ACIN input to P output not using multiplier.	1.57	1.88	1.88	ns
$T_{DSPDO\_ACIN\_ACOUT}$	ACIN input to ACOUT output.	0.44	0.53	0.53	ns
$T_{DSPDO\_ACIN\_CARRYCASCOUT\_MULT}$	ACIN input to CARRYCASCOUT output using multiplier.	4.47	5.33	5.33	ns
$T_{DSPDO\_ACIN\_CARRYCASCOUT}$	ACIN input to CARRYCASCOUT output not using multiplier.	1.85	2.21	2.21	ns
$T_{DSPDO\_PCIN\_P}$	PCIN input to P output.	1.28	1.52	1.52	ns

Table 37: **MMCM Specification *(Cont'd)***

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
$T_{MMCMDCK\_PSINCDEC}$/ $T_{MMCMCKD\_PSINCDEC}$	Setup and hold of phase-shift increment/decrement.	1.04/0.00	1.04/0.00	1.04/0.00	ns
$T_{MMCMCKO\_PSDONE}$	Phase shift clock-to-out of PSDONE.	0.68	0.81	0.81	ns
Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK					
$T_{MMCMDCK\_DADDR}$/ $T_{MMCMCKD\_DADDR}$	DADDR setup/hold.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
$T_{MMCMDCK\_DI}$/ $T_{MMCMCKD\_DI}$	DI setup/hold.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
$T_{MMCMDCK\_DEN}$/ $T_{MMCMCKD\_DEN}$	DEN setup/hold.	1.97/0.00	2.29/0.00	2.29/0.00	ns, Min
$T_{MMCMDCK\_DWE}$/ $T_{MMCMCKD\_DWE}$	DWE setup/hold.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
$T_{MMCMCKO\_DRDY}$	CLK to out of DRDY.	0.72	0.99	0.99	ns, Max
F_{DCK}	DCLK frequency.	200.00	200.00	200.00	MHz, Max

Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the *Clocking Wizard* [Ref 8].
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.
6. When CLKOUT4_CASCADE = TRUE, MMCM_F_{OUTMIN} is 0.036 MHz.

PLL Switching Characteristics

Table 38: **PLL Specification**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
PLL_F_{INMAX}	Maximum input clock frequency.	800.00	800.00	800.00	MHz
PLL_F_{INMIN}	Minimum input clock frequency.	19.00	19.00	19.00	MHz
PLL_$F_{INJITTER}$	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max			
PLL_F_{INDUTY}	Allowable input duty cycle: 19—49 MHz.	25	25	25	%
	Allowable input duty cycle: 50—199 MHz.	30	30	30	%
	Allowable input duty cycle: 200—399 MHz.	35	35	35	%
	Allowable input duty cycle: 400—499 MHz.	40	40	40	%
	Allowable input duty cycle: >500 MHz.	45	45	45	%
PLL_F_{VCOMIN}	Minimum PLL VCO frequency.	800.00	800.00	800.00	MHz
PLL_F_{VCOMAX}	Maximum PLL VCO frequency.	1866.00	1600.00	1600.00	MHz

Table 42: **Clock-Capable Clock Input to Output Delay With PLL[1]**

Symbol	Description	Device	V_{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *with* PLL.						
$T_{ICKOFPLLCC}$	Clock-capable clock input and OUTFF *with* PLL.[2]	XC7S6	0.85	0.85	0.85	ns
		XC7S15	0.85	0.85	0.85	ns
		XC7S25	0.83	0.83	0.83	ns
		XC7S50	0.83	0.83	0.83	ns
		XC7S75	0.83	0.83	0.83	ns
		XC7S100	0.83	0.83	0.83	ns
		XA7S6	0.85	0.85	N/A	ns
		XA7S15	0.85	0.85	N/A	ns
		XA7S25	0.83	0.83	N/A	ns
		XA7S50	0.83	0.83	N/A	ns
		XA7S75	0.83	0.83	N/A	ns
		XA7S100	0.83	0.83	N/A	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is already included in the timing calculation.

Table 43: **Pin-to-Pin, Clock-to-Out using BUFIO**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with BUFIO.					
$T_{ICKOFCS}$	Clock to out of I/O clock.	5.61	6.64	6.64	ns

Table 45: **Clock-Capable Clock Input Setup and Hold With MMCM**

Symbol	Description	Device	V_{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.[1][2]						
$T_{PSMMCMCC}$/ $T_{PHMMCMCC}$	No delay clock-capable clock input and IFF[3] with MMCM.	XC7S6	2.73/–0.59	3.27/–0.59	3.27/–0.59	ns
		XC7S15	2.73/–0.59	3.27/–0.59	3.27/–0.59	ns
		XC7S25	2.69/–0.61	3.21/–0.61	3.21/–0.61	ns
		XC7S50	2.81/–0.62	3.35/–0.62	3.35/–0.62	ns
		XC7S75	2.81/–0.62	3.36/–0.62	3.36/–0.62	ns
		XC7S100	2.81/–0.62	3.36/–0.62	3.36/–0.62	ns
		XA7S6	2.73/–0.59	3.27/–0.59	N/A	ns
		XA7S15	2.73/–0.59	3.27/–0.59	N/A	ns
		XA7S25	2.69/–0.61	3.21/–0.61	N/A	ns
		XA7S50	2.81/–0.62	3.35/–0.62	N/A	ns
		XA7S75	2.81/–0.62	3.36/–0.62	N/A	ns
		XA7S100	2.81/–0.62	3.36/–0.62	N/A	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. Use IBIS to determine any duty-cycle distortion incurred using various standards.
3. IFF = Input flip-flop or latch.

Additional Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for Spartan-7 FPGA clock transmitter and receiver data-valid windows.

Table 49: **Package Skew**[1]

Symbol	Description	Device	Package	Value	Units
$T_{PKGSKEW}$	Package skew.[2]	XC7S6	CPGA196	44	ps
			CSGA225	83	ps
			FTGB196	65	ps
		XC7S15	CPGA196	44	ps
			CSGA225	83	ps
			FTGB196	65	ps
		XC7S25	CSGA225	93	ps
			CSGA324	62	ps
			FTGB196	83	ps
		XC7S50	CSGA324	80	ps
			FGGA484	110	ps
			FTGB196	103	ps
		XC7S75	FGGA484	117	ps
			FGGA676	110	ps
		XC7S100	FGGA484	117	ps
			FGGA676	110	ps
		XA7S6	CPGA196	44	ps
			CSGA225	83	ps
			FTGB196	65	ps
		XA7S15	CPGA196	44	ps
			CSGA225	83	ps
			FTGB196	65	ps
		XA7S25	CSGA225	93	ps
			CSGA324	62	ps
			FTGB196	83	ps
		XA7S50	CSGA324	80	ps
			FGGA484	110	ps
			FTGB196	103	ps
		XA7S75	FGGA484	117	ps
			FGGA676	110	ps
		XC7S100	FGGA484	117	ps
			FGGA676	110	ps

Notes:

1. Package delay information is available for these device/package combinations. This information can be used to deskew the package.
2. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.

Table 51: **Configuration Switching Characteristics *(Cont'd)***

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
$T_{SMCSCCK}$/ $T_{SMCCKCS}$	CSI_B setup/hold.	4.00/0.00	4.00/0.00	4.00/0.00	ns, Min
T_{SMWCCK}/ T_{SMCCKW}	RDWR_B setup/hold.	10.00/0.00	10.00/0.00	10.00/0.00	ns, Min
$T_{SMCKCSO}$	CSO_B clock to out (330 Ω pull-up resistor required).	7.00	7.00	7.00	ns, Max
T_{SMCO}	D[31:00] clock to out in readback.	8.00	8.00	8.00	ns, Max
F_{RBCCK}	Readback frequency.	100.00	100.00	100.00	MHz, Max
Boundary-Scan Port Timing Specifications					
T_{TAPTCK}/ T_{TCKTAP}	TMS and TDI setup/hold.	3.00/2.00	3.00/2.00	3.00/2.00	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output.	7.00	7.00	7.00	ns, Max
F_{TCK}	TCK frequency.	66.00	66.00	66.00	MHz, Max
SPI Flash Master Mode Programming Switching					
T_{SPIDCC}/ T_{SPICCD}	D[03:00] setup/hold.	3.00/0.00	3.00/0.00	3.00/0.00	ns, Min
T_{SPICCM}	MOSI clock to out.	8.00	8.00	8.00	ns, Max
$T_{SPICCFC}$	FCS_B clock to out.	8.00	8.00	8.00	ns, Max
STARTUPE2 Ports					
$T_{USRCCLKO}$	STARTUPE2 USRCCLKO input to CCLK output.	0.50/6.70	0.50/7.50	0.50/7.50	ns, Min/Max
$F_{CFGMCLK}$	STARTUPE2 CFGMCLK output frequency.	65.00	65.00	65.00	MHz, Typ
$F_{CFGMCLKTOL}$	STARTUPE2 CFGMCLK output frequency tolerance.	±50	±50	±50	%, Max
Device DNA Access Port					
F_{DNACK}	DNA access port (DNA_PORT).	100.00	100.00	100.00	MHz, Max

Notes:

1. To support longer delays in configuration, use the design solutions described in the *7 Series FPGA Configuration User Guide* (UG470) [Ref 10].
2. See the *7 Series FPGAs Overview* (DS180) [Ref 1] and *XA Spartan-7 Automotive FPGA Data Sheet: Overview* (DS171) [Ref 2] for a list of devices that support bitstream encryption.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
07/31/2018	1.7	In Table 12, updated Vivado tools version to 2018.2.1. In Table 13, moved all speed grades for all devices to Production. In Table 14, added Vivado tools version for XC7S6, XC7S15, XC7S75, XC7S100, XA7S6, XA7S15, XA7S75, and XA7S100.
06/18/2018	1.6	In Table 12, updated Vivado tools version to 2018.2. In Table 13, moved all speed grades except -1Q (1.0V) for XC7S6 and XC7S15 to Production. In Table 14, added Vivado tools version for XC7S6 and XC7S15.
04/04/2018	1.5	Added XA7S6, XA7S15, XA7S25, XA7S75, and XA7S100 devices throughout. In Table 5, updated typical quiescent supply current values for XC7S25 and XC7S50 devices, and added values for XC7S6, XC7S15, XC7S75, and XC7S100 devices. In Table 6, updated table title and $I_{CCINTMIN}$ and $I_{CCAUXMIN}$ for XC7S75 and XC7S100 devices. In Table 13, moved all speed grades for XC7S6 and XC7S15 to Preliminary, moved -1LI (0.95V) speed grade for XC7S25 to Production, and moved all speed grades except -1Q (1.0V) for XC7S75 and XC7S100 from Preliminary to Production. In Table 14, added Vivado tools version for XC7S25, XC7S75, and XC7S100. In Table 36, Table 39, Table 40, Table 41, Table 42, Table 44, Table 45, and Table 46, changed parameter value for XA7S50 to N/A. In Table 49, added package skew values for XC7S6 and XC7S15 devices.
12/22/2017	1.4	In Table 12, updated Vivado tools version to 2017.4. In Table 13, moved all speed grades for XC7S75 and XC7S100 from Advance to Preliminary and all speed grades except -1LI (0.95V) for XC7S25 from Advance to Production. In Table 14, added Vivado tools version for XC7S25. Added Note 2 to Table 16. In Table 49, added package skew values for XC7S25 device in CSGA324 package and XC7S75 and XC7S100 devices in FGGA676 package.
11/20/2017	1.3	Added XA7S50 device throughout. Updated description of offered temperature ranges in second paragraph of Introduction. Added row for junction temperature (T_j) at expanded (Q) temperature to Table 2. Added -1Q (1.0V) speed grade to Table 5, and Table 13 to Table 16. In Table 12, updated Vivado tools version to 2017.3. In Table 49, added package skew values for XC7S25, XC7S50, XC7S75, and XC7S100 devices in CSGA225, FTGB196, and FGGA484 packages. Added *XA Spartan-7 Automotive FPGA Data Sheet: Overview* (DS171) to References.
06/20/2017	1.2	Updated paragraph before Table 6. In Table 12, updated Vivado tools version to 2017.2. In Table 13, moved all speed grades for XC7S50 from Preliminary to Production and updated Note 1. In Table 14, added Vivado tools version for XC7S50. In Table 49, added package skew value for XC7S50 device in FGGA484 package.
04/07/2017	1.1	Added 1.35V to Note 5 in Table 2. In Table 12, updated Vivado tools version to 2016.4. In Table 13, moved all speed grades for XC7S50 from Advance to Preliminary. Removed SFI-4.1 and SPI-4.2 from descriptions of SDR LVDS receiver and DDR LVDS receiver, respectively, in Table 15. In Table 25, changed $T_{IDELAYRESOLUTION}$ units from ps to µs. Removed BUFMR from Note 1 in Table 34. In Table 49, replaced TQGA144 with FTGB196 for XC7S6, XC7S15, and XC7S25 devices, added FTGB196 package for XC7S50 device, and added package skew value for XC7S50 device in CSGA324 package.
09/27/2016	1.0	Initial Xilinx release.