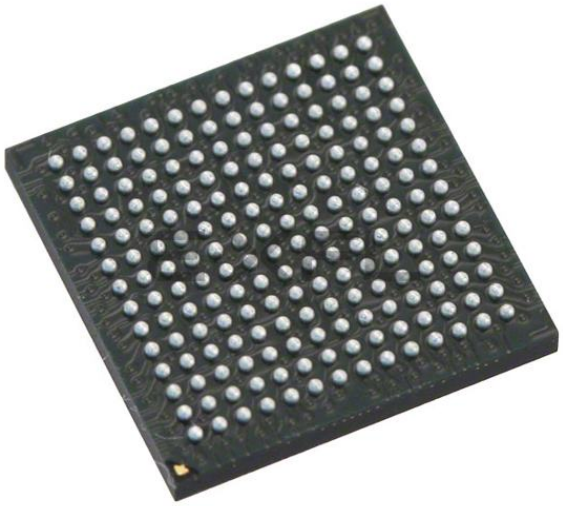

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 6000 |
| Total RAM Bits | 184320 |
| Number of I/O | 100 |
| Number of Gates | - |
| Voltage - Supply | 0.95V ~ 1.05V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 196-TFBGA, CSBGA |
| Supplier Device Package | 196-CSPBGA (8x8) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc7s6-1cpga196i |

*Table 3:* **DC Characteristics Over Recommended Operating Conditions**

| Symbol | Description | Min | Typ[1] | Max | Units |
|---|---|---|---|---|---|
| $V_{DRINT}$ | Data retention $V_{CCINT}$ voltage (below which configuration data might be lost). | 0.75 | – | – | V |
| $V_{DRI}$ | Data retention $V_{CCAUX}$ voltage (below which configuration data might be lost). | 1.5 | – | – | V |
| $I_{REF}$ | $V_{REF}$ leakage current per pin. | – | – | 15 | µA |
| $I_L$ | Input or output leakage current per pin (sample-tested). | – | – | 15 | µA |
| $C_{IN}$[2] | Die input capacitance at the pad. | – | – | 8 | pF |
| $I_{RPU}$ | Pad pull-up (when selected) at $V_{IN}$ = 0V, $V_{CCO}$ = 3.3V. | 90 | – | 330 | µA |
| | Pad pull-up (when selected) at $V_{IN}$ = 0V, $V_{CCO}$ = 2.5V. | 68 | – | 250 | µA |
| | Pad pull-up (when selected) at $V_{IN}$ = 0V, $V_{CCO}$ = 1.8V. | 34 | – | 220 | µA |
| | Pad pull-up (when selected) at $V_{IN}$ = 0V, $V_{CCO}$ = 1.5V. | 23 | – | 150 | µA |
| | Pad pull-up (when selected) at $V_{IN}$ = 0V, $V_{CCO}$ = 1.2V. | 12 | – | 120 | µA |
| $I_{RPD}$ | Pad pull-down (when selected) at $V_{IN}$ = 3.3V. | 68 | – | 330 | µA |
| $I_{CCADC}$ | Analog supply current, analog circuits in powered up state. | – | – | 25 | mA |
| $I_{BATT}$[3] | Battery supply current. | – | – | 150 | nA |
| $R_{IN\_TERM}$[4] | Thevenin equivalent resistance of programmable input termination to $V_{CCO}$/2 (UNTUNED_SPLIT_40). | 28 | 40 | 55 | Ω |
| | Thevenin equivalent resistance of programmable input termination to $V_{CCO}$/2 (UNTUNED_SPLIT_50). | 35 | 50 | 65 | Ω |
| | Thevenin equivalent resistance of programmable input termination to $V_{CCO}$/2 (UNTUNED_SPLIT_60). | 44 | 60 | 83 | Ω |
| n | Temperature diode ideality factor. | – | 1.010 | – | – |
| r | Temperature diode series resistance. | – | 2 | – | Ω |

**Notes:**

1. Typical values are specified at nominal voltage, 25°C.
2. This measurement represents the die capacitance at the pad, not including the package.
3. Maximum value specified for worst case process at 25°C.
4. Termination resistance to a $V_{CCO}$/2 level.

# DC Input and Output Levels

Values for $V_{IL}$ and $V_{IH}$ are recommended input voltages. Values for $I_{OL}$ and $I_{OH}$ are guaranteed over the recommended operating conditions at the $V_{OL}$ and $V_{OH}$ test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum $V_{CCO}$ with the respective $V_{OL}$ and $V_{OH}$ voltage levels shown. Other standards are sample tested.

*Table 8:* **SelectIO DC Input and Output Levels**(1)(2)(3)

| I/O Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ | $V_{OH}$ | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|
| | V, Min | V, Max | V, Min | V, Max | V, Max | V, Min | mA, Max | mA, Min |
| HSTL_I | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | 8.00 | –8.00 |
| HSTL_I_18 | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | 8.00 | –8.00 |
| HSTL_II | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | 16.00 | –16.00 |
| HSTL_II_18 | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | 16.00 | –16.00 |
| HSUL_12 | –0.300 | $V_{REF}$ – 0.130 | $V_{REF}$ + 0.130 | $V_{CCO}$ + 0.300 | 20% $V_{CCO}$ | 80% $V_{CCO}$ | 0.10 | –0.10 |
| LVCMOS12 | –0.300 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | Note 4 | Note 4 |
| LVCMOS15 | –0.300 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 25% $V_{CCO}$ | 75% $V_{CCO}$ | Note 5 | Note 5 |
| LVCMOS18 | –0.300 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 0.450 | $V_{CCO}$ – 0.450 | Note 6 | Note 6 |
| LVCMOS25 | –0.300 | 0.7 | 1.700 | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | Note 5 | Note 5 |
| LVCMOS33 | –0.300 | 0.8 | 2.000 | 3.450 | 0.400 | $V_{CCO}$ – 0.400 | Note 5 | Note 5 |
| LVTTL | –0.300 | 0.8 | 2.000 | 3.450 | 0.400 | 2.400 | Note 6 | Note 6 |
| MOBILE_DDR | –0.300 | 20% $V_{CCO}$ | 80% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 10% $V_{CCO}$ | 90% $V_{CCO}$ | 0.10 | –0.10 |
| PCI33_3 | –0.400 | 30% $V_{CCO}$ | 50% $V_{CCO}$ | $V_{CCO}$ + 0.500 | 10% $V_{CCO}$ | 90% $V_{CCO}$ | 1.50 | –0.50 |
| SSTL135 | –0.300 | $V_{REF}$ – 0.090 | $V_{REF}$ + 0.090 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.150 | $V_{CCO}$/2 + 0.150 | 13.00 | –13.00 |
| SSTL135_R | –0.300 | $V_{REF}$ – 0.090 | $V_{REF}$ + 0.090 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.150 | $V_{CCO}$/2 + 0.150 | 8.90 | –8.90 |
| SSTL15 | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.175 | $V_{CCO}$/2 + 0.175 | 13.00 | –13.00 |
| SSTL15_R | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.175 | $V_{CCO}$/2 + 0.175 | 8.90 | –8.90 |
| SSTL18_I | –0.300 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.470 | $V_{CCO}$/2 + 0.470 | 8.00 | –8.00 |
| SSTL18_II | –0.300 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.600 | $V_{CCO}$/2 + 0.600 | 13.40 | –13.40 |

**Notes:**

1. Tested according to relevant specifications.
2. 3.3V and 2.5V standards are only supported in HR I/O banks.
3. For detailed interface specific DC voltage levels, see the *7 Series FPGAs SelectIO Resources User Guide* (UG471) [Ref 3].
4. Supported drive strengths of 4, 8, or 12 mA in HR I/O banks.
5. Supported drive strengths of 4, 8, 12, or 16 mA in HR I/O banks.
6. Supported drive strengths of 4, 8, 12, 16, or 24 mA in HR I/O banks.

*Table 9:* **Differential SelectIO DC Input and Output Levels**

| I/O Standard | $V_{ICM}$[1] | | | $V_{ID}$[2] | | | $V_{OCM}$[3] | | | $V_{OD}$[4] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | V, Min | V, Typ | V, Max | V, Min | V, Typ | V, Max | V, Min | V, Typ | V, Max | V, Min | V, Typ | V, Max |
| BLVDS_25 | 0.300 | 1.200 | 1.425 | 0.100 | – | – | – | 1.250 | – | Note 5 | | |
| MINI_LVDS_25 | 0.300 | 1.200 | $V_{CCAUX}$ | 0.200 | 0.400 | 0.600 | 1.000 | 1.200 | 1.400 | 0.300 | 0.450 | 0.600 |
| PPDS_25 | 0.200 | 0.900 | $V_{CCAUX}$ | 0.100 | 0.250 | 0.400 | 0.500 | 0.950 | 1.400 | 0.100 | 0.250 | 0.400 |
| RSDS_25 | 0.300 | 0.900 | 1.500 | 0.100 | 0.350 | 0.600 | 1.000 | 1.200 | 1.400 | 0.100 | 0.350 | 0.600 |
| TMDS_33 | 2.700 | 2.965 | 3.230 | 0.150 | 0.675 | 1.200 | $V_{CCO}$ – 0.405 | $V_{CCO}$ – 0.300 | $V_{CCO}$ – 0.190 | 0.400 | 0.600 | 0.800 |

**Notes:**

1. $V_{ICM}$ is the input common mode voltage.
2. $V_{ID}$ is the input differential voltage (Q – $\overline{Q}$).
3. $V_{OCM}$ is the output common mode voltage.
4. $V_{OD}$ is the output differential voltage (Q – $\overline{Q}$).
5. $V_{OD}$ for BLVDS will vary significantly depending on topology and loading.

*Table 10:* **Complementary Differential SelectIO DC Input and Output Levels**

| I/O Standard | $V_{ICM}$[1] | | | $V_{ID}$[2] | | $V_{OL}$[3] | $V_{OH}$[4] | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|---|
| | V, Min | V, Typ | V, Max | V, Min | V, Max | V, Max | V, Min | mA, Max | mA, Min |
| DIFF_HSTL_I | 0.300 | 0.750 | 1.125 | 0.100 | – | 0.400 | $V_{CCO}$ – 0.400 | 8.00 | –8.00 |
| DIFF_HSTL_I_18 | 0.300 | 0.900 | 1.425 | 0.100 | – | 0.400 | $V_{CCO}$ – 0.400 | 8.00 | –8.00 |
| DIFF_HSTL_II | 0.300 | 0.750 | 1.125 | 0.100 | – | 0.400 | $V_{CCO}$ – 0.400 | 16.00 | –16.00 |
| DIFF_HSTL_II_18 | 0.300 | 0.900 | 1.425 | 0.100 | – | 0.400 | $V_{CCO}$ – 0.400 | 16.00 | –16.00 |
| DIFF_HSUL_12 | 0.300 | 0.600 | 0.850 | 0.100 | – | 20% $V_{CCO}$ | 80% $V_{CCO}$ | 0.100 | –0.100 |
| DIFF_MOBILE_DDR | 0.300 | 0.900 | 1.425 | 0.100 | – | 10% $V_{CCO}$ | 90% $V_{CCO}$ | 0.100 | –0.100 |
| DIFF_SSTL135 | 0.300 | 0.675 | 1.000 | 0.100 | – | ($V_{CCO}$/2) – 0.150 | ($V_{CCO}$/2) + 0.150 | 13.0 | –13.0 |
| DIFF_SSTL135_R | 0.300 | 0.675 | 1.000 | 0.100 | – | ($V_{CCO}$/2) – 0.150 | ($V_{CCO}$/2) + 0.150 | 8.9 | –8.9 |
| DIFF_SSTL15 | 0.300 | 0.750 | 1.125 | 0.100 | – | ($V_{CCO}$/2) – 0.175 | ($V_{CCO}$/2) + 0.175 | 13.0 | –13.0 |
| DIFF_SSTL15_R | 0.300 | 0.750 | 1.125 | 0.100 | – | ($V_{CCO}$/2) – 0.175 | ($V_{CCO}$/2) + 0.175 | 8.9 | –8.9 |
| DIFF_SSTL18_I | 0.300 | 0.900 | 1.425 | 0.100 | – | ($V_{CCO}$/2) – 0.470 | ($V_{CCO}$/2) + 0.470 | 8.00 | –8.00 |
| DIFF_SSTL18_II | 0.300 | 0.900 | 1.425 | 0.100 | – | ($V_{CCO}$/2) – 0.600 | ($V_{CCO}$/2) + 0.600 | 13.4 | –13.4 |

**Notes:**

1. $V_{ICM}$ is the input common mode voltage.
2. $V_{ID}$ is the input differential voltage (Q – $\overline{Q}$).
3. $V_{OL}$ is the single-ended low-output voltage.
4. $V_{OH}$ is the single-ended high-output voltage.

# LVDS DC Specifications (LVDS_25)

*Table 11:* **LVDS_25 DC Specifications**[1]

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCO}$ | Supply voltage. | | 2.375 | 2.500 | 2.625 | V |
| $V_{OH}$ | Output High voltage for Q and $\overline{Q}$. | $R_T$ = 100Ω across Q and $\overline{Q}$ signals. | – | – | 1.675 | V |
| $V_{OL}$ | Output Low voltage for Q and $\overline{Q}$. | $R_T$ = 100Ω across Q and $\overline{Q}$ signals. | 0.700 | – | – | V |
| $V_{ODIFF}$ | Differential output voltage:<br>(Q – $\overline{Q}$), Q = High<br>($\overline{Q}$ – Q), $\overline{Q}$ = High | $R_T$ = 100Ω across Q and $\overline{Q}$ signals. | 247 | 350 | 600 | mV |
| $V_{OCM}$ | Output common-mode voltage. | $R_T$ = 100Ω across Q and $\overline{Q}$ signals. | 1.000 | 1.250 | 1.425 | V |
| $V_{IDIFF}$ | Differential input voltage:<br>(Q – $\overline{Q}$), Q = High<br>($\overline{Q}$ – Q), $\overline{Q}$ = High | | 100 | 350 | 600 | mV |
| $V_{ICM}$ | Input common-mode voltage. | | 0.300 | 1.200 | 1.500 | V |

**Notes:**

1. Differential inputs for LVDS_25 can be placed in banks with $V_{CCO}$ levels that are different from the required level for outputs. Consult the *7 Series FPGAs SelectIO Resources User Guide* (UG471) [Ref 3] for more information.

*Table 17:* **IOB High Range (HR) Switching Characteristics *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | $T_{IOOP}$ | | | $T_{IOTP}$ | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | $V_{CCINT}$ Operating Voltage and Speed Grade | | | | | | | | | |
| | 1.0V | | 0.95V | 1.0V | | 0.95V | 1.0V | | 0.95V | |
| | -2 | -1 | -1L | -2 | -1 | -1L | -2 | -1 | -1L | |
| LVCMOS15_F8 | 0.86 | 0.93 | 0.93 | 1.72 | 1.98 | 1.98 | 1.75 | 1.99 | 1.99 | ns |
| LVCMOS15_F12 | 0.86 | 0.93 | 0.93 | 1.47 | 1.73 | 1.73 | 1.50 | 1.74 | 1.74 | ns |
| LVCMOS15_F16 | 0.86 | 0.93 | 0.93 | 1.46 | 1.71 | 1.71 | 1.49 | 1.73 | 1.73 | ns |
| LVCMOS12_S4 | 0.95 | 1.02 | 1.02 | 2.69 | 2.95 | 2.95 | 2.72 | 2.96 | 2.96 | ns |
| LVCMOS12_S8 | 0.95 | 1.02 | 1.02 | 2.21 | 2.46 | 2.46 | 2.24 | 2.48 | 2.48 | ns |
| LVCMOS12_S12 | 0.95 | 1.02 | 1.02 | 1.91 | 2.17 | 2.17 | 1.94 | 2.18 | 2.18 | ns |
| LVCMOS12_F4 | 0.95 | 1.02 | 1.02 | 2.10 | 2.35 | 2.35 | 2.13 | 2.37 | 2.37 | ns |
| LVCMOS12_F8 | 0.95 | 1.02 | 1.02 | 1.66 | 1.92 | 1.92 | 1.69 | 1.93 | 1.93 | ns |
| LVCMOS12_F12 | 0.95 | 1.02 | 1.02 | 1.51 | 1.76 | 1.76 | 1.54 | 1.77 | 1.77 | ns |
| SSTL135_S | 0.75 | 0.82 | 0.82 | 1.47 | 1.73 | 1.73 | 1.50 | 1.74 | 1.74 | ns |
| SSTL15_S | 0.68 | 0.75 | 0.75 | 1.43 | 1.68 | 1.68 | 1.46 | 1.69 | 1.69 | ns |
| SSTL18_I_S | 0.75 | 0.82 | 0.82 | 1.79 | 2.04 | 2.04 | 1.82 | 2.06 | 2.06 | ns |
| SSTL18_II_S | 0.75 | 0.82 | 0.82 | 1.43 | 1.68 | 1.68 | 1.46 | 1.70 | 1.70 | ns |
| DIFF_SSTL135_S | 0.76 | 0.83 | 0.83 | 1.47 | 1.73 | 1.73 | 1.50 | 1.74 | 1.74 | ns |
| DIFF_SSTL15_S | 0.76 | 0.83 | 0.83 | 1.43 | 1.68 | 1.68 | 1.46 | 1.69 | 1.69 | ns |
| DIFF_SSTL18_I_S | 0.79 | 0.86 | 0.86 | 1.80 | 2.06 | 2.06 | 1.83 | 2.07 | 2.07 | ns |
| DIFF_SSTL18_II_S | 0.79 | 0.86 | 0.86 | 1.51 | 1.76 | 1.76 | 1.54 | 1.77 | 1.77 | ns |
| SSTL135_F | 0.75 | 0.82 | 0.82 | 1.24 | 1.49 | 1.49 | 1.27 | 1.51 | 1.51 | ns |
| SSTL15_F | 0.68 | 0.75 | 0.75 | 1.19 | 1.45 | 1.45 | 1.22 | 1.46 | 1.46 | ns |
| SSTL18_I_F | 0.75 | 0.82 | 0.82 | 1.24 | 1.49 | 1.49 | 1.27 | 1.51 | 1.51 | ns |
| SSTL18_II_F | 0.75 | 0.82 | 0.82 | 1.24 | 1.49 | 1.49 | 1.27 | 1.51 | 1.51 | ns |
| DIFF_SSTL135_F | 0.76 | 0.83 | 0.83 | 1.24 | 1.49 | 1.49 | 1.27 | 1.51 | 1.51 | ns |
| DIFF_SSTL15_F | 0.76 | 0.83 | 0.83 | 1.19 | 1.45 | 1.45 | 1.22 | 1.46 | 1.46 | ns |
| DIFF_SSTL18_I_F | 0.79 | 0.86 | 0.86 | 1.35 | 1.60 | 1.60 | 1.38 | 1.62 | 1.62 | ns |
| DIFF_SSTL18_II_F | 0.79 | 0.86 | 0.86 | 1.33 | 1.59 | 1.59 | 1.36 | 1.60 | 1.60 | ns |

Table 18 specifies the values of $T_{IOTPHZ}$ and $T_{IOIBUFDISABLE}$. $T_{IOTPHZ}$ is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). $T_{IOIBUFDISABLE}$ is described as the IOB delay from IBUFDISABLE to O output. In HR I/O banks, the internal IN_TERM termination turn-off time is always faster than $T_{IOTPHZ}$ when the INTERMDISABLE pin is used.

*Table 18:* **IOB 3-state Output Switching Characteristics**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| $T_{IOTPHZ}$ | T input to pad high-impedance. | 2.19 | 2.37 | 2.37 | ns |
| $T_{IOIBUFDISABLE}$ | IBUF turn-on time from IBUFDISABLE to O output. | 2.30 | 2.60 | 2.60 | ns |

# Input Serializer/Deserializer Switching Characteristics

*Table 23:* **ISERDES Switching Characteristics**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| **Setup/Hold for Control Lines** | | | | | |
| $T_{ISCCK\_BITSLIP}$/ $T_{ISCKC\_BITSLIP}$ | BITSLIP pin setup/hold with respect to CLKDIV. | 0.02/0.15 | 0.02/0.17 | 0.02/0.17 | ns |
| $T_{ISCCK\_CE}$/ $T_{ISCKC\_CE}$ | CE pin setup/hold with respect to CLK (for CE1). | 0.50/–0.01 | 0.72/–0.01 | 0.72/–0.01 | ns |
| $T_{ISCCK\_CE2}$/ $T_{ISCKC\_CE2}$ | CE pin setup/hold with respect to CLKDIV (for CE2). | –0.10/0.36 | –0.10/0.40 | –0.10/0.40 | ns |
| **Setup/Hold for Data Lines** | | | | | |
| $T_{ISDCK\_D}$/ $T_{ISCKD\_D}$ | D pin setup/hold with respect to CLK. | –0.02/0.14 | –0.02/0.17 | –0.02/0.17 | ns |
| $T_{ISDCK\_DDLY}$/ $T_{ISCKD\_DDLY}$ | DDLY pin setup/hold with respect to CLK (using IDELAY).(1) | –0.02/0.14 | –0.02/0.17 | –0.02/0.17 | ns |
| $T_{ISDCK\_D\_DDR}$/ $T_{ISCKD\_D\_DDR}$ | D pin setup/hold with respect to CLK at DDR mode. | –0.02/0.14 | –0.02/0.17 | –0.02/0.17 | ns |
| $T_{ISDCK\_DDLY\_DDR}$/ $T_{ISCKD\_DDLY\_DDR}$ | D pin setup/hold with respect to CLK at DDR mode (using IDELAY).(1) | 0.14/0.14 | 0.17/0.17 | 0.17/0.17 | ns |
| **Sequential Delays** | | | | | |
| $T_{ISCKO\_Q}$ | CLKDIV to out at Q pin. | 0.54 | 0.66 | 0.66 | ns |
| **Propagation Delays** | | | | | |
| $T_{ISDO\_DO}$ | D input to DO output pin. | 0.11 | 0.13 | 0.13 | ns |

**Notes:**

1. Recorded at 0 tap value.

# Output Serializer/Deserializer Switching Characteristics

*Table 24:* **OSERDES Switching Characteristics**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| **Setup/Hold** | | | | | |
| $T_{OSDCK\_D}$/ $T_{OSCKD\_D}$ | D input setup/hold with respect to CLKDIV. | 0.45/0.03 | 0.63/0.03 | 0.63/0.03 | ns |
| $T_{OSDCK\_T}$/ $T_{OSCKD\_T}$ | T input setup/hold with respect to CLK. | 0.73/–0.13 | 0.88/–0.13 | 0.88/–0.13 | ns |
| $T_{OSDCK\_T2}$/ $T_{OSCKD\_T2}$ | T input setup/hold with respect to CLKDIV. | 0.34/–0.13 | 0.39/–0.13 | 0.39/–0.13 | ns |
| $T_{OSCCK\_OCE}$/ $T_{OSCKC\_OCE}$ | OCE input setup/hold with respect to CLK. | 0.34/0.58 | 0.51/0.58 | 0.51/0.58 | ns |
| $T_{OSCCK\_S}$ | SR (reset) input setup with respect to CLKDIV. | 0.52 | 0.85 | 0.85 | ns |
| $T_{OSCCK\_TCE}$/ $T_{OSCKC\_TCE}$ | TCE input setup/hold with respect to CLK. | 0.34/0.01 | 0.51/0.01 | 0.51/0.01 | ns |
| **Sequential Delays** | | | | | |
| $T_{OSCKO\_OQ}$ | Clock to out from CLK to OQ. | 0.42 | 0.48 | 0.48 | ns |
| $T_{OSCKO\_TQ}$ | Clock to out from CLK to TQ. | 0.49 | 0.56 | 0.56 | ns |
| **Combinatorial** | | | | | |
| $T_{OSDO\_TTQ}$ | T input to TQ out. | 0.92 | 1.11 | 1.11 | ns |

*Table 26:* **IO_FIFO Switching Characteristics**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| **IO_FIFO Clock to Out Delays** | | | | | |
| $T_{OFFCKO\_DO}$ | RDCLK to Q outputs. | 0.60 | 0.68 | 0.68 | ns |
| $T_{CKO\_FLAGS}$ | Clock to IO_FIFO flags. | 0.61 | 0.77 | 0.77 | ns |
| **Setup/Hold** | | | | | |
| $T_{CCK\_D}/T_{CKC\_D}$ | D inputs to WRCLK. | 0.51/0.02 | 0.58/0.02 | 0.58/0.02 | ns |
| $T_{IFFCCK\_WREN}$/ $T_{IFFCKC\_WREN}$ | WREN to WRCLK. | 0.47/–0.01 | 0.53/–0.01 | 0.53/–0.01 | ns |
| $T_{OFFCCK\_RDEN}$/ $T_{OFFCKC\_RDEN}$ | RDEN to RDCLK. | 0.58/0.02 | 0.66/0.02 | 0.66/0.02 | ns |
| **Minimum Pulse Width** | | | | | |
| $T_{PWH\_IO\_FIFO}$ | RESET, RDCLK, WRCLK. | 2.15 | 2.15 | 2.15 | ns |
| $T_{PWL\_IO\_FIFO}$ | RESET, RDCLK, WRCLK. | 2.15 | 2.15 | 2.15 | ns |
| Maximum Frequency | | | | | |
| $F_{MAX}$ | RDCLK and WRCLK. | 200.00 | 200.00 | 200.00 | MHz |

# CLB Distributed RAM Switching Characteristics (SLICEM Only)

*Table 28:* **CLB Distributed RAM Switching Characteristics**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| **Sequential Delays** | | | | | |
| $T_{SHCKO}$ | Clock to A – B outputs. | 1.09 | 1.32 | 1.32 | ns, Max |
| $T_{SHCKO\_1}$ | Clock to AMUX – BMUX outputs. | 1.53 | 1.86 | 1.86 | ns, Max |
| **Setup and Hold Times Before/After Clock CLK** | | | | | |
| $T_{DS\_LRAM}/T_{DH\_LRAM}$ | A – D inputs to CLK. | 0.60/0.30 | 0.72/0.35 | 0.72/0.35 | ns, Min |
| $T_{AS\_LRAM}/T_{AH\_LRAM}$ | Address An inputs to clock. | 0.30/0.60 | 0.37/0.70 | 0.37/0.70 | ns, Min |
| | Address An inputs through MUXs and/or carry logic to clock. | 0.77/0.21 | 0.94/0.26 | 0.94/0.26 | ns, Min |
| $T_{WS\_LRAM}/T_{WH\_LRAM}$ | WE input to clock. | 0.43/0.12 | 0.53/0.17 | 0.53/0.17 | ns, Min |
| $T_{CECK\_LRAM}/T_{CKCE\_LRAM}$ | CE input to CLK. | 0.44/0.11 | 0.53/0.17 | 0.53/0.17 | ns, Min |
| **Clock CLK** | | | | | |
| $T_{MPW\_LRAM}$ | Minimum pulse width. | 1.13 | 1.25 | 1.25 | ns, Min |
| $T_{MCP}$ | Minimum clock period. | 2.26 | 2.50 | 2.50 | ns, Min |

**Notes:**

1. $T_{SHCKO}$ also represents the CLK to XMUX output. Refer to the timing report for the CLK to XMUX path.

# CLB Shift Register Switching Characteristics (SLICEM Only)

*Table 29:* **CLB Shift Register Switching Characteristics**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| **Sequential Delays** | | | | | |
| $T_{REG}$ | Clock to A – D outputs. | 1.33 | 1.61 | 1.61 | ns, Max |
| $T_{REG\_MUX}$ | Clock to AMUX – DMUX output. | 1.77 | 2.15 | 2.15 | ns, Max |
| $T_{REG\_M31}$ | Clock to DMUX output via M31 output. | 1.23 | 1.46 | 1.46 | ns, Max |
| **Setup and Hold Times Before/After Clock CLK** | | | | | |
| $T_{WS\_SHFREG}/ T_{WH\_SHFREG}$ | WE input. | 0.41/0.12 | 0.51/0.17 | 0.51/0.17 | ns, Min |
| $T_{CECK\_SHFREG}/ T_{CKCE\_SHFREG}$ | CE input to CLK. | 0.42/0.11 | 0.52/0.17 | 0.52/0.17 | ns, Min |
| $T_{DS\_SHFREG}/ T_{DH\_SHFREG}$ | A – D inputs to CLK. | 0.37/0.37 | 0.44/0.43 | 0.44/0.43 | ns, Min |
| **Clock CLK** | | | | | |
| $T_{MPW\_SHFREG}$ | Minimum pulse width. | 0.86 | 0.98 | 0.98 | ns, Min |

*Table 31:* **DSP48E1 Switching Characteristics *(Cont'd)***

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| $T_{DSPDCK\_CEM\_MREG}$/ $T_{DSPCKD\_CEM\_MREG}$ | CEM input to M register CLK. | 0.21/ 0.20 | 0.27/ 0.23 | 0.27/ 0.23 | ns |
| $T_{DSPDCK\_CEP\_PREG}$/ $T_{DSPCKD\_CEP\_PREG}$ | CEP input to P register CLK. | 0.43/ 0.01 | 0.53/ 0.01 | 0.53/ 0.01 | ns |
| **Setup and Hold Times of the RST Pins** | | | | | |
| $T_{DSPDCK\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$/ $T_{DSPCKD\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$ | {RSTA, RSTB} input to {A, B} register CLK. | 0.46/ 0.13 | 0.55/ 0.15 | 0.55/ 0.15 | ns |
| $T_{DSPDCK\_RSTC\_CREG}$/ $T_{DSPCKD\_RSTC\_CREG}$ | RSTC input to C register CLK. | 0.08/ 0.11 | 0.09/ 0.12 | 0.09/ 0.12 | ns |
| $T_{DSPDCK\_RSTD\_DREG}$/ $T_{DSPCKD\_RSTD\_DREG}$ | RSTD input to D register CLK | 0.50/ 0.08 | 0.59/ 0.09 | 0.59/ 0.09 | ns |
| $T_{DSPDCK\_RSTM\_MREG}$/ $T_{DSPCKD\_RSTM\_MREG}$ | RSTM input to M register CLK | 0.23/ 0.24 | 0.27/ 0.28 | 0.27/ 0.28 | ns |
| $T_{DSPDCK\_RSTP\_PREG}$/ $T_{DSPCKD\_RSTP\_PREG}$ | RSTP input to P register CLK | 0.30/ 0.01 | 0.35/ 0.01 | 0.35/ 0.01 | ns |
| **Combinatorial Delays from Input Pins to Output Pins** | | | | | |
| $T_{DSPDO\_A\_CARRYOUT\_MULT}$ | A input to CARRYOUT output using multiplier. | 4.35 | 5.18 | 5.18 | ns |
| $T_{DSPDO\_D\_P\_MULT}$ | D input to P output using multiplier. | 4.26 | 5.07 | 5.07 | ns |
| $T_{DSPDO\_B\_P}$ | B input to P output not using multiplier. | 1.75 | 2.08 | 2.08 | ns |
| $T_{DSPDO\_C\_P}$ | C input to P output. | 1.53 | 1.82 | 1.82 | ns |
| **Combinatorial Delays from Input Pins to Cascading Output Pins** | | | | | |
| $T_{DSPDO\_\{A; B\}\_\{ACOUT; BCOUT\}}$ | {A, B} input to {ACOUT, BCOUT} output. | 0.63 | 0.74 | 0.74 | ns |
| $T_{DSPDO\_\{A, B\}\_CARRYCASCOUT\_MULT}$ | {A, B} input to CARRYCASCOUT output using multiplier. | 4.65 | 5.54 | 5.54 | ns |
| $T_{DSPDO\_D\_CARRYCASCOUT\_MULT}$ | D input to CARRYCASCOUT output using multiplier. | 4.54 | 5.40 | 5.40 | ns |
| $T_{DSPDO\_\{A, B\}\_CARRYCASCOUT}$ | {A, B} input to CARRYCASCOUT output not using multiplier. | 2.03 | 2.41 | 2.41 | ns |
| $T_{DSPDO\_C\_CARRYCASCOUT}$ | C input to CARRYCASCOUT output. | 1.81 | 2.15 | 2.15 | ns |
| **Combinatorial Delays from Cascading Input Pins to All Output Pins** | | | | | |
| $T_{DSPDO\_ACIN\_P\_MULT}$ | ACIN input to P output using multiplier. | 4.19 | 5.00 | 5.00 | ns |
| $T_{DSPDO\_ACIN\_P}$ | ACIN input to P output not using multiplier. | 1.57 | 1.88 | 1.88 | ns |
| $T_{DSPDO\_ACIN\_ACOUT}$ | ACIN input to ACOUT output. | 0.44 | 0.53 | 0.53 | ns |
| $T_{DSPDO\_ACIN\_CARRYCASCOUT\_MULT}$ | ACIN input to CARRYCASCOUT output using multiplier. | 4.47 | 5.33 | 5.33 | ns |
| $T_{DSPDO\_ACIN\_CARRYCASCOUT}$ | ACIN input to CARRYCASCOUT output not using multiplier. | 1.85 | 2.21 | 2.21 | ns |
| $T_{DSPDO\_PCIN\_P}$ | PCIN input to P output. | 1.28 | 1.52 | 1.52 | ns |

*Table 31:* **DSP48E1 Switching Characteristics *(Cont'd)***

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| $T_{DSPDO\_PCIN\_CARRYCASCOUT}$ | PCIN input to CARRYCASCOUT output. | 1.56 | 1.85 | 1.85 | ns |
| **Clock to Outs from Output Register Clock to Output Pins** | | | | | |
| $T_{DSPCKO\_P\_PREG}$ | CLK PREG to P output. | 0.37 | 0.44 | 0.44 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_PREG}$ | CLK PREG to CARRYCASCOUT output. | 0.59 | 0.69 | 0.69 | ns |
| **Clock to Outs from Pipeline Register Clock to Output Pins** | | | | | |
| $T_{DSPCKO\_P\_MREG}$ | CLK MREG to P output. | 1.93 | 2.31 | 2.31 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_MREG}$ | CLK MREG to CARRYCASCOUT output. | 2.21 | 2.64 | 2.64 | ns |
| $T_{DSPCKO\_P\_ADREG\_MULT}$ | CLK ADREG to P output using multiplier. | 3.10 | 3.69 | 3.69 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_ADREG\_MULT}$ | CLK ADREG to CARRYCASCOUT output using multiplier. | 3.38 | 4.02 | 4.02 | ns |
| **Clock to Outs from Input Register Clock to Output Pins** | | | | | |
| $T_{DSPCKO\_P\_AREG\_MULT}$ | CLK AREG to P output using multiplier. | 4.51 | 5.37 | 5.37 | ns |
| $T_{DSPCKO\_P\_BREG}$ | CLK BREG to P output not using multiplier. | 1.87 | 2.22 | 2.22 | ns |
| $T_{DSPCKO\_P\_CREG}$ | CLK CREG to P output not using multiplier. | 1.93 | 2.30 | 2.30 | ns |
| $T_{DSPCKO\_P\_DREG\_MULT}$ | CLK DREG to P output using multiplier. | 4.48 | 5.32 | 5.32 | ns |
| **Clock to Outs from Input Register Clock to Cascading Output Pins** | | | | | |
| $T_{DSPCKO\_\{ACOUT;\ BCOUT\}\_\{AREG;\ BREG\}}$ | CLK (ACOUT, BCOUT) to {A,B} register output. | 0.73 | 0.87 | 0.87 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_\{AREG,\ BREG\}\_MULT}$ | CLK (AREG, BREG) to CARRYCASCOUT output using multiplier. | 4.79 | 5.70 | 5.70 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_\ BREG}$ | CLK BREG to CARRYCASCOUT output not using multiplier. | 2.15 | 2.55 | 2.55 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_\ DREG\_MULT}$ | CLK DREG to CARRYCASCOUT output using multiplier. | 4.76 | 5.65 | 5.65 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_\ CREG}$ | CLK CREG to CARRYCASCOUT output. | 2.21 | 2.63 | 2.63 | ns |
| **Maximum Frequency** | | | | | |
| $F_{MAX}$ | With all registers used. | 550.66 | 464.25 | 464.25 | MHz |
| $F_{MAX\_PATDET}$ | With pattern detector. | 465.77 | 392.93 | 392.93 | MHz |
| $F_{MAX\_MULT\_NOMREG}$ | Two register multiply without MREG. | 305.62 | 257.47 | 257.47 | MHz |
| $F_{MAX\_MULT\_NOMREG\_PATDET}$ | Two register multiply without MREG with pattern detect. | 277.62 | 233.92 | 233.92 | MHz |
| $F_{MAX\_PREADD\_MULT\_NOADREG}$ | Without ADREG. | 346.26 | 290.44 | 290.44 | MHz |
| $F_{MAX\_PREADD\_MULT\_NOADREG\_PATDET}$ | Without ADREG with pattern detect. | 346.26 | 290.44 | 290.44 | MHz |
| $F_{MAX\_NOPIPELINEREG}$ | Without pipeline registers (MREG, ADREG). | 227.01 | 190.69 | 190.69 | MHz |
| $F_{MAX\_NOPIPELINEREG\_PATDET}$ | Without pipeline registers (MREG, ADREG) with pattern detect. | 211.15 | 177.43 | 177.43 | MHz |

# Clock Buffers and Networks

*Table 32:* **Global Clock Switching Characteristics (Including BUFGCTRL)**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| $T_{BCCCK\_CE}/T_{BCCKC\_CE}$(1) | CE pins setup/hold. | 0.13/0.40 | 0.16/0.41 | 0.16/0.41 | ns |
| $T_{BCCCK\_S}/T_{BCCKC\_S}$(1) | S pins setup/hold. | 0.13/0.40 | 0.16/0.41 | 0.16/0.41 | ns |
| $T_{BCCKO\_O}$(2) | BUFGCTRL delay from I0/I1 to O. | 0.09 | 0.10 | 0.10 | ns |
| **Maximum Frequency** | | | | | |
| $F_{MAX\_BUFG}$ | Global clock tree (BUFG). | 628.00 | 464.00 | 464.00 | MHz |

**Notes:**

1. $T_{BCCCK\_CE}$ and $T_{BCCKC\_CE}$ must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. $T_{BGCKO\_O}$ (BUFG delay from I0 to O) values are the same as $T_{BCCKO\_O}$ values.

*Table 33:* **Input/Output Clock Switching Characteristics (BUFIO)**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| $T_{BIOCKO\_O}$ | Clock to out delay from I to O. | 1.26 | 1.54 | 1.54 | ns |
| **Maximum Frequency** | | | | | |
| $F_{MAX\_BUFIO}$ | I/O clock tree (BUFIO). | 680.00 | 600.00 | 600.00 | MHz |

*Table 34:* **Regional Clock Buffer Switching Characteristics (BUFR)**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| $T_{BRCKO\_O}$ | Clock to out delay from I to O. | 0.76 | 0.99 | 0.99 | ns |
| $T_{BRCKO\_O\_BYP}$ | Clock to out delay from I to O with Divide Bypass attribute set. | 0.39 | 0.52 | 0.52 | ns |
| $T_{BRDO\_O}$ | Propagation delay from CLR to O. | 0.85 | 1.09 | 1.09 | ns |
| **Maximum Frequency** | | | | | |
| $F_{MAX\_BUFR}$(1) | Regional clock tree (BUFR). | 375.00 | 315.00 | 315.00 | MHz |

**Notes:**

1. The maximum input frequency to the BUFR is the BUFIO $F_{MAX}$ frequency.

*Table 40:* **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Far Clock Region)[1]**

| Symbol | Description | Device | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | 1.0V | | 0.95V | |
| | | | -2 | -1 | -1L | |
| **SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM/PLL.** | | | | | | |
| $T_{ICKOFFAR}$ | Clock-capable clock input and OUTFF at pins/banks farthest from the BUFGs *without* MMCM/PLL (far clock region).[2] | XC7S6 | 5.55 | 6.50 | 6.50 | ns |
| | | XC7S15 | 5.55 | 6.50 | 6.50 | ns |
| | | XC7S25 | 5.55 | 6.44 | 6.44 | ns |
| | | XC7S50 | 5.71 | 6.62 | 6.62 | ns |
| | | XC7S75 | 6.01 | 7.02 | 7.02 | ns |
| | | XC7S100 | 6.01 | 7.02 | 7.02 | ns |
| | | XA7S6 | 5.55 | 6.50 | N/A | ns |
| | | XA7S15 | 5.55 | 6.50 | N/A | ns |
| | | XA7S25 | 5.55 | 6.44 | N/A | ns |
| | | XA7S50 | 5.71 | 6.62 | N/A | ns |
| | | XA7S75 | 6.01 | 7.02 | N/A | ns |
| | | XA7S100 | 6.01 | 7.02 | N/A | ns |

**Notes:**

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Refer to the *Die Level Bank Numbering Overview* section of the *7 Series FPGA Packaging and Pinout Specification* (UG475) [Ref 4].

*Table 41:* **Clock-Capable Clock Input to Output Delay With MMCM(1)**

| Symbol | Description | Device | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | 1.0V | | 0.95V | |
| | | | -2 | -1 | -1L | |
| **SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *with* MMCM.** | | | | | | |
| $T_{ICKOFMMCMCC}$ | Clock-capable clock input and OUTFF *with* MMCM.(2) | XC7S6 | 1.03 | 1.03 | 1.03 | ns |
| | | XC7S15 | 1.03 | 1.03 | 1.03 | ns |
| | | XC7S25 | 1.00 | 1.00 | 1.00 | ns |
| | | XC7S50 | 1.00 | 1.00 | 1.00 | ns |
| | | XC7S75 | 1.00 | 1.00 | 1.00 | ns |
| | | XC7S100 | 1.00 | 1.00 | 1.00 | ns |
| | | XA7S6 | 1.03 | 1.03 | N/A | ns |
| | | XA7S15 | 1.03 | 1.03 | N/A | ns |
| | | XA7S25 | 1.00 | 1.00 | N/A | ns |
| | | XA7S50 | 1.00 | 1.00 | N/A | ns |
| | | XA7S75 | 1.00 | 1.00 | N/A | ns |
| | | XA7S100 | 1.00 | 1.00 | N/A | ns |

**Notes:**

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

*Table 42:* **Clock-Capable Clock Input to Output Delay With PLL(1)**

| Symbol | Description | Device | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | 1.0V | | 0.95V | |
| | | | -2 | -1 | -1L | |
| **SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *with* PLL.** | | | | | | |
| $T_{ICKOFPLLCC}$ | Clock-capable clock input and OUTFF *with* PLL.(2) | XC7S6 | 0.85 | 0.85 | 0.85 | ns |
| | | XC7S15 | 0.85 | 0.85 | 0.85 | ns |
| | | XC7S25 | 0.83 | 0.83 | 0.83 | ns |
| | | XC7S50 | 0.83 | 0.83 | 0.83 | ns |
| | | XC7S75 | 0.83 | 0.83 | 0.83 | ns |
| | | XC7S100 | 0.83 | 0.83 | 0.83 | ns |
| | | XA7S6 | 0.85 | 0.85 | N/A | ns |
| | | XA7S15 | 0.85 | 0.85 | N/A | ns |
| | | XA7S25 | 0.83 | 0.83 | N/A | ns |
| | | XA7S50 | 0.83 | 0.83 | N/A | ns |
| | | XA7S75 | 0.83 | 0.83 | N/A | ns |
| | | XA7S100 | 0.83 | 0.83 | N/A | ns |

**Notes:**

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is already included in the timing calculation.

*Table 43:* **Pin-to-Pin, Clock-to-Out using BUFIO**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| **SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with BUFIO.** | | | | | |
| $T_{ICKOFCS}$ | Clock to out of I/O clock. | 5.61 | 6.64 | 6.64 | ns |

# Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

*Table 44:* **Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks**

| Symbol | Description | Device | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | 1.0V | | 0.95V | |
| | | | -2 | -1 | -1L | |
| **Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1)** | | | | | | |
| $T_{PSFD}$/ $T_{PHFD}$ | Full delay (legacy delay or default delay) global clock input and IFF(2) without MMCM/PLL with ZHOLD_DELAY on HR I/O banks. | XC7S6 | 2.76/–0.40 | 3.17/–0.40 | 3.17/–0.40 | ns |
| | | XC7S15 | 2.76/–0.40 | 3.17/–0.40 | 3.17/–0.40 | ns |
| | | XC7S25 | 2.67/–0.37 | 3.12/–0.37 | 3.12/–0.37 | ns |
| | | XC7S50 | 2.66/–0.28 | 3.11/–0.28 | 3.11/–0.28 | ns |
| | | XC7S75 | 2.91/–0.33 | 3.36/–0.33 | 3.36/–0.33 | ns |
| | | XC7S100 | 2.91/–0.33 | 3.36/–0.33 | 3.36/–0.33 | ns |
| | | XA7S6 | 2.76/–0.40 | 3.17/–0.40 | N/A | ns |
| | | XA7S15 | 2.76/–0.40 | 3.17/–0.40 | N/A | ns |
| | | XA7S25 | 2.67/–0.37 | 3.12/–0.37 | N/A | ns |
| | | XA7S50 | 2.66/–0.28 | 3.11/–0.28 | N/A | ns |
| | | XA7S75 | 2.91/–0.33 | 3.36/–0.33 | N/A | ns |
| | | XA7S100 | 2.91/–0.33 | 3.36/–0.33 | N/A | ns |

**Notes:**

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch.

*Table 48:* **Sample Window**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| $T_{SAMP}$ | Sampling error at receiver pins.(1) | 0.64 | 0.70 | 0.70 | ns |
| $T_{SAMP\_BUFIO}$ | Sampling error at receiver pins using BUFIO.(2) | 0.40 | 0.46 | 0.46 | ns |

**Notes:**

1. This parameter indicates the total sampling error of the Spartan-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 MMCM jitter
   - MMCM accuracy (phase offset)
   - MMCM phase shift resolution

   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of the Spartan-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

# XADC Specifications

The *7 Series FPGAs Overview* (DS180) [Ref 1] and *XA Spartan-7 Automotive FPGA Data Sheet: Overview* (DS171) [Ref 2] list the devices that contain a 7 series XADC dual 12-Bit 1 MSPS analog-to-digital converter.

*Table 50:* **XADC Specifications**

| Parameter | Symbol | Comments/Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCADC}$ = 1.8V ± 5%, $V_{REFP}$ = 1.25V, $V_{REFN}$ = 0V, ADCCLK = 26 MHz, –55°C ≤ $T_j$ ≤ 125°C. Typical values at $T_j$ = +40°C. | | | | | | |
| **ADC Accuracy**(1) | | | | | | |
| Resolution | | | 12 | – | – | Bits |
| Integral nonlinearity(2) | INL | –40°C ≤ $T_j$ ≤ 100°C | – | – | ±2 | LSBs |
| | | –55°C ≤ $T_j$ < –40°C; 100°C < $T_j$ ≤ 125°C | – | – | ±3 | LSBs |
| Differential nonlinearity | DNL | No missing codes, guaranteed monotonic. | – | – | ±1 | LSBs |
| Offset error | Unipolar | –40°C ≤ $T_j$ ≤ 100°C | – | – | ±8 | LSBs |
| | | –55°C ≤ $T_j$ < –40°C; 100°C < $T_j$ ≤ 125°C | – | – | ±12 | LSBs |
| | Bipolar | –55°C ≤ $T_j$ ≤ 125°C | – | – | ±4 | LSBs |
| Gain error | | | – | – | ±0.5 | % |
| Offset matching | | | – | – | 4 | LSBs |
| Gain matching | | | – | – | 0.3 | % |
| Sample rate | | | – | – | 1 | MS/s |
| Signal to noise ratio(2) | SNR | $F_{SAMPLE}$ = 500 KS/s, $F_{IN}$ = 20 kHz | 60 | – | – | dB |
| RMS code noise | | External 1.25V reference. | – | – | 2 | LSBs |
| | | On-chip reference. | – | 3 | – | LSBs |
| Total harmonic distortion(2) | THD | $F_{SAMPLE}$ = 500 KS/s, $F_{IN}$ = 20 kHz | 70 | – | – | dB |
| **Analog Inputs**(3) | | | | | | |
| ADC input ranges | | Unipolar operation. | 0 | – | 1 | V |
| | | Bipolar operation. | –0.5 | – | +0.5 | V |
| | | Unipolar common mode range (FS input). | 0 | – | +0.5 | V |
| | | Bipolar common mode range (FS input). | +0.5 | – | +0.6 | V |
| Maximum external channel input ranges | | Adjacent analog channels set within these ranges should not corrupt measurements on adjacent channels. | –0.1 | – | $V_{CCADC}$ | V |
| Full-resolution bandwidth | FRBW | Auxiliary channel full resolution bandwidth. | 250 | – | – | kHz |
| **On-chip Sensors** | | | | | | |
| Temperature sensor error | | –40°C ≤ $T_j$ ≤ 100°C | – | – | ±4 | °C |
| | | –55°C ≤ $T_j$ < –40°C; 100°C < $T_j$ ≤ 125°C | – | – | ±6 | °C |
| Supply sensor error | | –40°C ≤ $T_j$ ≤ 100°C | – | – | ±1 | % |
| | | –55°C ≤ $T_j$ < –40°C; 100°C < $T_j$ ≤ 125°C | – | – | ±2 | % |

*Table 50:* **XADC Specifications *(Cont'd)***

| Parameter | Symbol | Comments/Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Conversion Rate(4)** | | | | | | |
| Conversion time: continuous | $t_{CONV}$ | Number of ADCCLK cycles. | 26 | – | 32 | Cycles |
| Conversion time: event | $t_{CONV}$ | Number of CLK cycles. | – | – | 21 | Cycles |
| DRP clock frequency | DCLK | DRP clock frequency. | 8 | – | 250 | MHz |
| ADC clock frequency | ADCCLK | Derived from DCLK. | 1 | – | 26 | MHz |
| DCLK duty cycle | | | 40 | – | 60 | % |
| **XADC Reference(5)** | | | | | | |
| External reference | $V_{REFP}$ | Externally supplied reference voltage. | 1.20 | 1.25 | 1.30 | V |
| On-chip reference | | Ground $V_{REFP}$ pin to AGND, $-40°C \le T_j \le 100°C$ | 1.2375 | 1.25 | 1.2625 | V |
| | | Ground VREFP pin to AGND, $-55°C \le T_j < -40°C$; $100°C < T_j \le 125°C$ | 1.225 | 1.25 | 1.275 | V |

**Notes:**

1. Offset and gain errors are removed by enabling the XADC automatic gain calibration feature. The values are specified for when this feature is enabled.
2. Only specified for bitstream option XADCEnhancedLinearity = ON.
3. For a detailed description, see the *ADC* chapter in the *7 Series FPGAs and Zynq-7000 AP SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480) [Ref 9].
4. For a detailed description, see the *Timing* chapter in the *7 Series FPGAs and Zynq-7000 AP SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480) [Ref 9].
5. Any variation in the reference voltage from the nominal $V_{REFP}$ = 1.25V and $V_{REFN}$ = 0V will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted.