# AMD Xilinx - XC7S6-2CPGA196I Datasheet

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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 6000 |
| Total RAM Bits | 184320 |
| Number of I/O | 100 |
| Number of Gates | - |
| Voltage - Supply | 0.95V ~ 1.05V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 196-TFBGA, CSBGA |
| Supplier Device Package | 196-CSPBGA (8x8) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc7s6-2cpga196i |

*Table 2:* **Recommended Operating Conditions**(1)(2)

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **FPGA Logic** | | | | | |
| $V_{CCINT}$(3) | For -2 and -1 (1.0V) devices: internal supply voltage. | 0.95 | 1.00 | 1.05 | V |
| | For -1L (0.95V) devices: internal supply voltage. | 0.92 | 0.95 | 0.98 | V |
| $V_{CCAUX}$ | Auxiliary supply voltage. | 1.71 | 1.80 | 1.89 | V |
| $V_{CCBRAM}$(3) | For -2 and -1 (1.0V) devices: block RAM supply voltage. | 0.95 | 1.00 | 1.05 | V |
| | For -1L (0.95V) devices: block RAM supply voltage. | 0.92 | 0.95 | 0.98 | V |
| $V_{CCO}$(4)(5) | Supply voltage for HR I/O banks. | 1.14 | – | 3.465 | V |
| $V_{IN}$(6) | I/O input voltage. | –0.20 | – | $V_{CCO}$ + 0.20 | V |
| | I/O input voltage (when $V_{CCO}$ = 3.3V) for $V_{REF}$ and differential I/O standards except TMDS_33.(7) | –0.20 | – | 2.625 | V |
| $I_{IN}$(8) | Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode. | – | – | 10 | mA |
| $V_{CCBATT}$(9) | Battery voltage. | 1.0 | – | 1.89 | V |
| **XADC** | | | | | |
| $V_{CCADC}$ | XADC supply relative to GNDADC. | 1.71 | 1.80 | 1.89 | V |
| $V_{REFP}$ | Externally supplied reference voltage. | 1.20 | 1.25 | 1.30 | V |
| **Temperature** | | | | | |
| $T_j$ | Junction temperature operating range for commercial (C) temperature devices. | 0 | – | 85 | °C |
| | Junction temperature operating range for industrial (I) temperature devices. | –40 | – | 100 | °C |
| | Junction temperature operating range for expanded (Q) temperature devices. | –40 | – | 125 | °C |

**Notes:**

1. All voltages are relative to ground.
2. For the design of the power distribution system consult the *7 Series FPGAs PCB Design Guide* (UG483) [Ref 5].
3. If $V_{CCINT}$ and $V_{CCBRAM}$ are operating at the same voltage, $V_{CCINT}$ and $V_{CCBRAM}$ should be connected to the same supply.
4. Configuration data is retained even if $V_{CCO}$ drops to 0V.
5. Includes $V_{CCO}$ of 1.2V, 1.35V, 1.5V, 1.8V, 2.5V, and 3.3V at ±5%.
6. The lower absolute voltage specification always applies.
7. See Table 9 for TMDS_33 specifications.
8. A total of 200 mA per bank should not be exceeded.
9. $V_{CCBATT}$ is required only when using bitstream encryption. If battery is not used, connect $V_{CCBATT}$ to either ground or $V_{CCAUX}$.

*Table 4:* **$V_{IN}$ Maximum Allowed AC Voltage Overshoot and Undershoot for HR I/O Banks(1)(2)**

| AC Voltage Overshoot | % of UI at –40°C to 125°C | AC Voltage Undershoot | % of UI at –40°C to 125°C |
|---|---|---|---|
| $V_{CCO}$ + 0.55 | 100 | –0.40 | 100 |
| | | –0.45 | 61.7 |
| | | –0.50 | 25.8 |
| | | –0.55 | 11.0 |
| $V_{CCO}$ + 0.60 | 46.6 | –0.60 | 4.77 |
| $V_{CCO}$ + 0.65 | 21.2 | –0.65 | 2.10 |
| $V_{CCO}$ + 0.70 | 9.75 | –0.70 | 0.94 |
| $V_{CCO}$ + 0.75 | 4.55 | –0.75 | 0.43 |
| $V_{CCO}$ + 0.80 | 2.15 | –0.80 | 0.20 |
| $V_{CCO}$ + 0.85 | 1.02 | –0.85 | 0.09 |
| $V_{CCO}$ + 0.90 | 0.49 | –0.90 | 0.04 |
| $V_{CCO}$ + 0.95 | 0.24 | –0.95 | 0.02 |

**Notes:**

1. A total of 200 mA per bank should not be exceeded.
2. The peak voltage of the overshoot or undershoot, and the duration above $V_{CCO}$ + 0.20V or below GND – 0.20V, must not exceed the values in this table.

*Table 5:* **Typical Quiescent Supply Current(1)(2)(3)**

| Symbol | Description | Device | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | | | 0.95V | |
| | | | -2C | -2I | -1C | -1I | -1Q | -1LI | |
| $I_{CCINTQ}$ | Quiescent $V_{CCINT}$ supply current. | XC7S6 | 36 | 36 | 36 | 36 | 36 | 32 | mA |
| | | XC7S15 | 36 | 36 | 36 | 36 | 36 | 32 | mA |
| | | XC7S25 | 48 | 48 | 48 | 48 | 48 | 43 | mA |
| | | XC7S50 | 95 | 95 | 95 | 95 | 95 | 59 | mA |
| | | XC7S75 | 148 | 148 | 148 | 148 | 148 | 134 | mA |
| | | XC7S100 | 148 | 148 | 148 | 148 | 148 | 134 | mA |
| | | XA7S6 | N/A | 36 | N/A | 36 | 36 | N/A | mA |
| | | XA7S15 | N/A | 36 | N/A | 36 | 36 | N/A | mA |
| | | XA7S25 | N/A | 48 | N/A | 48 | 48 | N/A | mA |
| | | XA7S50 | N/A | 95 | N/A | 95 | 95 | N/A | mA |
| | | XA7S75 | N/A | 148 | N/A | 148 | 148 | N/A | mA |
| | | XA7S100 | N/A | 148 | N/A | 148 | 148 | N/A | mA |

*Table 5:* **Typical Quiescent Supply Current(1)(2)(3)** ***(Cont'd)***

| **Symbol** | **Description** | **Device** | **Speed Grade** | | | | | | **Units** |
|---|---|---|---|---|---|---|---|---|---|
| | | | **1.0V** | | | | | **0.95V** | |
| | | | **-2C** | **-2I** | **-1C** | **-1I** | **-1Q** | **-1LI** | |
| $I_{CCOQ}$ | Quiescent $V_{CCO}$ supply current. | XC7S6 | 1 | 1 | 1 | 1 | 1 | 1 | mA |
| | | XC7S15 | 1 | 1 | 1 | 1 | 1 | 1 | mA |
| | | XC7S25 | 1 | 1 | 1 | 1 | 1 | 1 | mA |
| | | XC7S50 | 1 | 1 | 1 | 1 | 1 | 1 | mA |
| | | XC7S75 | 4 | 4 | 4 | 4 | 4 | 4 | mA |
| | | XC7S100 | 4 | 4 | 4 | 4 | 4 | 4 | mA |
| | | XA7S6 | N/A | 1 | N/A | 1 | 1 | N/A | mA |
| | | XA7S15 | N/A | 1 | N/A | 1 | 1 | N/A | mA |
| | | XA7S25 | N/A | 1 | N/A | 1 | 1 | N/A | mA |
| | | XA7S50 | N/A | 1 | N/A | 1 | 1 | N/A | mA |
| | | XA7S75 | N/A | 4 | N/A | 4 | 4 | N/A | mA |
| | | XA7S100 | N/A | 4 | N/A | 4 | 4 | N/A | mA |
| $I_{CCAUXQ}$ | Quiescent $V_{CCAUX}$ supply current. | XC7S6 | 10 | 10 | 10 | 10 | 10 | 10 | mA |
| | | XC7S15 | 10 | 10 | 10 | 10 | 10 | 10 | mA |
| | | XC7S25 | 13 | 13 | 13 | 13 | 13 | 13 | mA |
| | | XC7S50 | 22 | 22 | 22 | 22 | 22 | 20 | mA |
| | | XC7S75 | 43 | 43 | 43 | 43 | 43 | 43 | mA |
| | | XC7S100 | 43 | 43 | 43 | 43 | 43 | 43 | mA |
| | | XA7S6 | N/A | 10 | N/A | 10 | 10 | N/A | mA |
| | | XA7S15 | N/A | 10 | N/A | 10 | 10 | N/A | mA |
| | | XA7S25 | N/A | 13 | N/A | 13 | 13 | N/A | mA |
| | | XA7S50 | N/A | 22 | N/A | 22 | 22 | N/A | mA |
| | | XA7S75 | N/A | 43 | N/A | 43 | 43 | N/A | mA |
| | | XA7S100 | N/A | 43 | N/A | 43 | 43 | N/A | mA |

Table 6 shows the minimum current, in addition to $I_{CCQ}$ maximum, that is required by Spartan-7 devices for proper power-on and configuration. If the current minimums shown in Table 6 are met, the device powers on after all four supplies have passed through their power-on reset threshold voltages. The FPGA must not be configured until after $V_{CCINT}$ is applied. Once initialized and configured, use the *Xilinx Power Estimator* spreadsheet tool [Ref 6] to estimate current drain on these supplies.

*Table 6:* **Power-On Current**

| Device | $I_{CCINTMIN}$ | $I_{CCAUXMIN}$ | $I_{CCOMIN}$ | $I_{CCBRAMMIN}$ | Units |
|---|---|---|---|---|---|
| XC7S6 | $I_{CCINTQ}$ + 120 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 40 mA per bank | $I_{CCBRAMQ}$ + 60 | mA |
| XC7S15 | $I_{CCINTQ}$ + 120 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 40 mA per bank | $I_{CCBRAMQ}$ + 60 | mA |
| XC7S25 | $I_{CCINTQ}$ + 120 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 40 mA per bank | $I_{CCBRAMQ}$ + 60 | mA |
| XC7S50 | $I_{CCINTQ}$ + 120 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 40 mA per bank | $I_{CCBRAMQ}$ + 60 | mA |
| XC7S75 | $I_{CCINTQ}$ + 300 | $I_{CCAUXQ}$ + 140 | $I_{CCOQ}$ + 40 mA per bank | $I_{CCBRAMQ}$ + 60 | mA |
| XC7S100 | $I_{CCINTQ}$ + 300 | $I_{CCAUXQ}$ + 140 | $I_{CCOQ}$ + 40 mA per bank | $I_{CCBRAMQ}$ + 60 | mA |
| XA7S6 | $I_{CCINTQ}$ + 120 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 40 mA per bank | $I_{CCBRAMQ}$ + 60 | mA |
| XA7S15 | $I_{CCINTQ}$ + 120 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 40 mA per bank | $I_{CCBRAMQ}$ + 60 | mA |
| XA7S25 | $I_{CCINTQ}$ + 120 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 40 mA per bank | $I_{CCBRAMQ}$ + 60 | mA |
| XA7S50 | $I_{CCINTQ}$ + 120 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 40 mA per bank | $I_{CCBRAMQ}$ + 60 | mA |
| XA7S75 | $I_{CCINTQ}$ + 300 | $I_{CCAUXQ}$ + 140 | $I_{CCOQ}$ + 40 mA per bank | $I_{CCBRAMQ}$ + 60 | mA |
| XA7S100 | $I_{CCINTQ}$ + 300 | $I_{CCAUXQ}$ + 140 | $I_{CCOQ}$ + 40 mA per bank | $I_{CCBRAMQ}$ + 60 | mA |

*Table 7:* **Power Supply Ramp Time**

| Symbol | Description | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| $T_{VCCINT}$ | Ramp time from GND to 90% of $V_{CCINT}$. | | 0.2 | 50 | ms |
| $T_{VCCO}$ | Ramp time from GND to 90% of $V_{CCO}$. | | 0.2 | 50 | ms |
| $T_{VCCAUX}$ | Ramp time from GND to 90% of $V_{CCAUX}$. | | 0.2 | 50 | ms |
| $T_{VCCBRAM}$ | Ramp time from GND to 90% of $V_{CCBRAM}$. | | 0.2 | 50 | ms |
| $T_{VCCO2VCCAUX}$ | Allowed time per power cycle for $V_{CCO} - V_{CCAUX} > 2.625V$. | $T_J = 125°C$(1) | – | 300 | ms |
| | | $T_J = 100°C$(1) | – | 500 | ms |
| | | $T_J = 85°C$(1) | – | 800 | ms |

**Notes:**

1. Based on 240,000 power cycles with a nominal $V_{CCO}$ of 3.3V or 36,500 power cycles with a worst case $V_{CCO}$ of 3.465V.

### *Table 9:* Differential SelectIO DC Input and Output Levels

| I/O Standard | $V_{ICM}$[1] | | | $V_{ID}$[2] | | | $V_{OCM}$[3] | | | $V_{OD}$[4] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | V, Min | V, Typ | V, Max | V, Min | V, Typ | V, Max | V, Min | V, Typ | V, Max | V, Min | V, Typ | V, Max |
| BLVDS_25 | 0.300 | 1.200 | 1.425 | 0.100 | – | – | – | 1.250 | – | Note 5 | | |
| MINI_LVDS_25 | 0.300 | 1.200 | $V_{CCAUX}$ | 0.200 | 0.400 | 0.600 | 1.000 | 1.200 | 1.400 | 0.300 | 0.450 | 0.600 |
| PPDS_25 | 0.200 | 0.900 | $V_{CCAUX}$ | 0.100 | 0.250 | 0.400 | 0.500 | 0.950 | 1.400 | 0.100 | 0.250 | 0.400 |
| RSDS_25 | 0.300 | 0.900 | 1.500 | 0.100 | 0.350 | 0.600 | 1.000 | 1.200 | 1.400 | 0.100 | 0.350 | 0.600 |
| TMDS_33 | 2.700 | 2.965 | 3.230 | 0.150 | 0.675 | 1.200 | $V_{CCO}$ – 0.405 | $V_{CCO}$ – 0.300 | $V_{CCO}$ – 0.190 | 0.400 | 0.600 | 0.800 |

**Notes:**

1. $V_{ICM}$ is the input common mode voltage.
2. $V_{ID}$ is the input differential voltage ($Q - \overline{Q}$).
3. $V_{OCM}$ is the output common mode voltage.
4. $V_{OD}$ is the output differential voltage ($Q - \overline{Q}$).
5. $V_{OD}$ for BLVDS will vary significantly depending on topology and loading.

### *Table 10:* Complementary Differential SelectIO DC Input and Output Levels

| I/O Standard | $V_{ICM}$[1] | | | $V_{ID}$[2] | | $V_{OL}$[3] | $V_{OH}$[4] | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|---|
| | V, Min | V, Typ | V, Max | V, Min | V, Max | V, Max | V, Min | mA, Max | mA, Min |
| DIFF_HSTL_I | 0.300 | 0.750 | 1.125 | 0.100 | – | 0.400 | $V_{CCO}$ – 0.400 | 8.00 | –8.00 |
| DIFF_HSTL_I_18 | 0.300 | 0.900 | 1.425 | 0.100 | – | 0.400 | $V_{CCO}$ – 0.400 | 8.00 | –8.00 |
| DIFF_HSTL_II | 0.300 | 0.750 | 1.125 | 0.100 | – | 0.400 | $V_{CCO}$ – 0.400 | 16.00 | –16.00 |
| DIFF_HSTL_II_18 | 0.300 | 0.900 | 1.425 | 0.100 | – | 0.400 | $V_{CCO}$ – 0.400 | 16.00 | –16.00 |
| DIFF_HSUL_12 | 0.300 | 0.600 | 0.850 | 0.100 | – | 20% $V_{CCO}$ | 80% $V_{CCO}$ | 0.100 | –0.100 |
| DIFF_MOBILE_DDR | 0.300 | 0.900 | 1.425 | 0.100 | – | 10% $V_{CCO}$ | 90% $V_{CCO}$ | 0.100 | –0.100 |
| DIFF_SSTL135 | 0.300 | 0.675 | 1.000 | 0.100 | – | ($V_{CCO}$/2) – 0.150 | ($V_{CCO}$/2) + 0.150 | 13.0 | –13.0 |
| DIFF_SSTL135_R | 0.300 | 0.675 | 1.000 | 0.100 | – | ($V_{CCO}$/2) – 0.150 | ($V_{CCO}$/2) + 0.150 | 8.9 | –8.9 |
| DIFF_SSTL15 | 0.300 | 0.750 | 1.125 | 0.100 | – | ($V_{CCO}$/2) – 0.175 | ($V_{CCO}$/2) + 0.175 | 13.0 | –13.0 |
| DIFF_SSTL15_R | 0.300 | 0.750 | 1.125 | 0.100 | – | ($V_{CCO}$/2) – 0.175 | ($V_{CCO}$/2) + 0.175 | 8.9 | –8.9 |
| DIFF_SSTL18_I | 0.300 | 0.900 | 1.425 | 0.100 | – | ($V_{CCO}$/2) – 0.470 | ($V_{CCO}$/2) + 0.470 | 8.00 | –8.00 |
| DIFF_SSTL18_II | 0.300 | 0.900 | 1.425 | 0.100 | – | ($V_{CCO}$/2) – 0.600 | ($V_{CCO}$/2) + 0.600 | 13.4 | –13.4 |

**Notes:**

1. $V_{ICM}$ is the input common mode voltage.
2. $V_{ID}$ is the input differential voltage ($Q - \overline{Q}$).
3. $V_{OL}$ is the single-ended low-output voltage.
4. $V_{OH}$ is the single-ended high-output voltage.

# AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications from the Vivado® Design Suite as outlined in Table 12.

*Table 12:* **Speed Specification Version By Device**

| 2018.2.1 | Device |
|---|---|
| 1.23 | XC7S6, XC7S15, XC7S25, XC7S50, XC7S75, XC7S100 |
| 1.16 | XA7S6, XA7S15, XA7S25, XA7S50, XA7S75, XA7S100 |

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows.

### Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

### Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

### Production Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

# Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Spartan-7 FPGAs.

*Table 17:* **IOB High Range (HR) Switching Characteristics *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | $T_{IOOP}$ | | | $T_{IOTP}$ | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | $V_{CCINT}$ Operating Voltage and Speed Grade | | | | | | | | | |
| | 1.0V | | 0.95V | 1.0V | | 0.95V | 1.0V | | 0.95V | |
| | -2 | -1 | -1L | -2 | -1 | -1L | -2 | -1 | -1L | |
| LVCMOS15_F8 | 0.86 | 0.93 | 0.93 | 1.72 | 1.98 | 1.98 | 1.75 | 1.99 | 1.99 | ns |
| LVCMOS15_F12 | 0.86 | 0.93 | 0.93 | 1.47 | 1.73 | 1.73 | 1.50 | 1.74 | 1.74 | ns |
| LVCMOS15_F16 | 0.86 | 0.93 | 0.93 | 1.46 | 1.71 | 1.71 | 1.49 | 1.73 | 1.73 | ns |
| LVCMOS12_S4 | 0.95 | 1.02 | 1.02 | 2.69 | 2.95 | 2.95 | 2.72 | 2.96 | 2.96 | ns |
| LVCMOS12_S8 | 0.95 | 1.02 | 1.02 | 2.21 | 2.46 | 2.46 | 2.24 | 2.48 | 2.48 | ns |
| LVCMOS12_S12 | 0.95 | 1.02 | 1.02 | 1.91 | 2.17 | 2.17 | 1.94 | 2.18 | 2.18 | ns |
| LVCMOS12_F4 | 0.95 | 1.02 | 1.02 | 2.10 | 2.35 | 2.35 | 2.13 | 2.37 | 2.37 | ns |
| LVCMOS12_F8 | 0.95 | 1.02 | 1.02 | 1.66 | 1.92 | 1.92 | 1.69 | 1.93 | 1.93 | ns |
| LVCMOS12_F12 | 0.95 | 1.02 | 1.02 | 1.51 | 1.76 | 1.76 | 1.54 | 1.77 | 1.77 | ns |
| SSTL135_S | 0.75 | 0.82 | 0.82 | 1.47 | 1.73 | 1.73 | 1.50 | 1.74 | 1.74 | ns |
| SSTL15_S | 0.68 | 0.75 | 0.75 | 1.43 | 1.68 | 1.68 | 1.46 | 1.69 | 1.69 | ns |
| SSTL18_I_S | 0.75 | 0.82 | 0.82 | 1.79 | 2.04 | 2.04 | 1.82 | 2.06 | 2.06 | ns |
| SSTL18_II_S | 0.75 | 0.82 | 0.82 | 1.43 | 1.68 | 1.68 | 1.46 | 1.70 | 1.70 | ns |
| DIFF_SSTL135_S | 0.76 | 0.83 | 0.83 | 1.47 | 1.73 | 1.73 | 1.50 | 1.74 | 1.74 | ns |
| DIFF_SSTL15_S | 0.76 | 0.83 | 0.83 | 1.43 | 1.68 | 1.68 | 1.46 | 1.69 | 1.69 | ns |
| DIFF_SSTL18_I_S | 0.79 | 0.86 | 0.86 | 1.80 | 2.06 | 2.06 | 1.83 | 2.07 | 2.07 | ns |
| DIFF_SSTL18_II_S | 0.79 | 0.86 | 0.86 | 1.51 | 1.76 | 1.76 | 1.54 | 1.77 | 1.77 | ns |
| SSTL135_F | 0.75 | 0.82 | 0.82 | 1.24 | 1.49 | 1.49 | 1.27 | 1.51 | 1.51 | ns |
| SSTL15_F | 0.68 | 0.75 | 0.75 | 1.19 | 1.45 | 1.45 | 1.22 | 1.46 | 1.46 | ns |
| SSTL18_I_F | 0.75 | 0.82 | 0.82 | 1.24 | 1.49 | 1.49 | 1.27 | 1.51 | 1.51 | ns |
| SSTL18_II_F | 0.75 | 0.82 | 0.82 | 1.24 | 1.49 | 1.49 | 1.27 | 1.51 | 1.51 | ns |
| DIFF_SSTL135_F | 0.76 | 0.83 | 0.83 | 1.24 | 1.49 | 1.49 | 1.27 | 1.51 | 1.51 | ns |
| DIFF_SSTL15_F | 0.76 | 0.83 | 0.83 | 1.19 | 1.45 | 1.45 | 1.22 | 1.46 | 1.46 | ns |
| DIFF_SSTL18_I_F | 0.79 | 0.86 | 0.86 | 1.35 | 1.60 | 1.60 | 1.38 | 1.62 | 1.62 | ns |
| DIFF_SSTL18_II_F | 0.79 | 0.86 | 0.86 | 1.33 | 1.59 | 1.59 | 1.36 | 1.60 | 1.60 | ns |

Table 18 specifies the values of $T_{IOTPHZ}$ and $T_{IOIBUFDISABLE}$. $T_{IOTPHZ}$ is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). $T_{IOIBUFDISABLE}$ is described as the IOB delay from IBUFDISABLE to O output. In HR I/O banks, the internal IN_TERM termination turn-off time is always faster than $T_{IOTPHZ}$ when the INTERMDISABLE pin is used.

*Table 22:* **OLOGIC Switching Characteristics**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| **Setup/Hold** | | | | | |
| $T_{ODCK}/T_{OCKD}$ | D1/D2 pins setup/hold with respect to CLK. | 0.71/–0.11 | 0.84/–0.11 | 0.84/–0.11 | ns |
| $T_{OOCECK}/T_{OCKOCE}$ | OCE pin setup/hold with respect to CLK. | 0.34/0.58 | 0.51/0.58 | 0.51/0.58 | ns |
| $T_{OSRCK}/T_{OCKSR}$ | SR pin setup/hold with respect to CLK. | 0.44/0.21 | 0.80/0.21 | 0.80/0.21 | ns |
| $T_{OTCK}/T_{OCKT}$ | T1/T2 pins setup/hold with respect to CLK. | 0.73/–0.14 | 0.89/–0.14 | 0.89/–0.14 | ns |
| $T_{OTCECK}/T_{OCKTCE}$ | TCE pin setup/hold with respect to CLK. | 0.34/0.01 | 0.51/0.01 | 0.51/0.01 | ns |
| **Combinatorial** | | | | | |
| $T_{ODQ}$ | D1 to OQ out or T1 to TQ out. | 0.96 | 1.16 | 1.16 | ns |
| **Sequential Delays** | | | | | |
| $T_{OCKQ}$ | CLK to OQ/TQ out. | 0.49 | 0.56 | 0.56 | ns |
| $T_{RQ\_OLOGIC}$ | SR pin to OQ/TQ out. | 0.80 | 0.95 | 0.95 | ns |
| $T_{GSRQ\_OLOGIC}$ | Global set/reset to Q outputs. | 7.60 | 10.51 | 10.51 | ns |
| **Set/Reset** | | | | | |
| $T_{RPW\_OLOGIC}$ | Minimum pulse width, SR inputs. | 0.74 | 0.74 | 0.74 | ns, Min |

## Output Serializer/Deserializer Switching Characteristics

*Table 24:* **OSERDES Switching Characteristics**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| **Setup/Hold** | | | | | |
| $T_{OSDCK\_D}$/<br>$T_{OSCKD\_D}$ | D input setup/hold with respect to CLKDIV. | 0.45/0.03 | 0.63/0.03 | 0.63/0.03 | ns |
| $T_{OSDCK\_T}$/<br>$T_{OSCKD\_T}$ | T input setup/hold with respect to CLK. | 0.73/–0.13 | 0.88/–0.13 | 0.88/–0.13 | ns |
| $T_{OSDCK\_T2}$/<br>$T_{OSCKD\_T2}$ | T input setup/hold with respect to CLKDIV. | 0.34/–0.13 | 0.39/–0.13 | 0.39/–0.13 | ns |
| $T_{OSCCK\_OCE}$/<br>$T_{OSCKC\_OCE}$ | OCE input setup/hold with respect to CLK. | 0.34/0.58 | 0.51/0.58 | 0.51/0.58 | ns |
| $T_{OSCCK\_S}$ | SR (reset) input setup with respect to CLKDIV. | 0.52 | 0.85 | 0.85 | ns |
| $T_{OSCCK\_TCE}$/<br>$T_{OSCKC\_TCE}$ | TCE input setup/hold with respect to CLK. | 0.34/0.01 | 0.51/0.01 | 0.51/0.01 | ns |
| **Sequential Delays** | | | | | |
| $T_{OSCKO\_OQ}$ | Clock to out from CLK to OQ. | 0.42 | 0.48 | 0.48 | ns |
| $T_{OSCKO\_TQ}$ | Clock to out from CLK to TQ. | 0.49 | 0.56 | 0.56 | ns |
| **Combinatorial** | | | | | |
| $T_{OSDO\_TTQ}$ | T input to TQ out. | 0.92 | 1.11 | 1.11 | ns |

*Table 26:* **IO_FIFO Switching Characteristics**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| **IO_FIFO Clock to Out Delays** | | | | | |
| $T_{OFFCKO\_DO}$ | RDCLK to Q outputs. | 0.60 | 0.68 | 0.68 | ns |
| $T_{CKO\_FLAGS}$ | Clock to IO_FIFO flags. | 0.61 | 0.77 | 0.77 | ns |
| **Setup/Hold** | | | | | |
| $T_{CCK\_D}/T_{CKC\_D}$ | D inputs to WRCLK. | 0.51/0.02 | 0.58/0.02 | 0.58/0.02 | ns |
| $T_{IFFCCK\_WREN}/$ $T_{IFFCKC\_WREN}$ | WREN to WRCLK. | 0.47/–0.01 | 0.53/–0.01 | 0.53/–0.01 | ns |
| $T_{OFFCCK\_RDEN}/$ $T_{OFFCKC\_RDEN}$ | RDEN to RDCLK. | 0.58/0.02 | 0.66/0.02 | 0.66/0.02 | ns |
| **Minimum Pulse Width** | | | | | |
| $T_{PWH\_IO\_FIFO}$ | RESET, RDCLK, WRCLK. | 2.15 | 2.15 | 2.15 | ns |
| $T_{PWL\_IO\_FIFO}$ | RESET, RDCLK, WRCLK. | 2.15 | 2.15 | 2.15 | ns |
| Maximum Frequency | | | | | |
| $F_{MAX}$ | RDCLK and WRCLK. | 200.00 | 200.00 | 200.00 | MHz |

# CLB Distributed RAM Switching Characteristics (SLICEM Only)

*Table 28:* **CLB Distributed RAM Switching Characteristics**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| **Sequential Delays** | | | | | |
| $T_{SHCKO}$ | Clock to A – B outputs. | 1.09 | 1.32 | 1.32 | ns, Max |
| $T_{SHCKO\_1}$ | Clock to AMUX – BMUX outputs. | 1.53 | 1.86 | 1.86 | ns, Max |
| **Setup and Hold Times Before/After Clock CLK** | | | | | |
| $T_{DS\_LRAM}/T_{DH\_LRAM}$ | A – D inputs to CLK. | 0.60/0.30 | 0.72/0.35 | 0.72/0.35 | ns, Min |
| $T_{AS\_LRAM}/T_{AH\_LRAM}$ | Address An inputs to clock. | 0.30/0.60 | 0.37/0.70 | 0.37/0.70 | ns, Min |
| | Address An inputs through MUXs and/or carry logic to clock. | 0.77/0.21 | 0.94/0.26 | 0.94/0.26 | ns, Min |
| $T_{WS\_LRAM}/T_{WH\_LRAM}$ | WE input to clock. | 0.43/0.12 | 0.53/0.17 | 0.53/0.17 | ns, Min |
| $T_{CECK\_LRAM}/T_{CKCE\_LRAM}$ | CE input to CLK. | 0.44/0.11 | 0.53/0.17 | 0.53/0.17 | ns, Min |
| **Clock CLK** | | | | | |
| $T_{MPW\_LRAM}$ | Minimum pulse width. | 1.13 | 1.25 | 1.25 | ns, Min |
| $T_{MCP}$ | Minimum clock period. | 2.26 | 2.50 | 2.50 | ns, Min |

**Notes:**

1. $T_{SHCKO}$ also represents the CLK to XMUX output. Refer to the timing report for the CLK to XMUX path.

# CLB Shift Register Switching Characteristics (SLICEM Only)

*Table 29:* **CLB Shift Register Switching Characteristics**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| **Sequential Delays** | | | | | |
| $T_{REG}$ | Clock to A – D outputs. | 1.33 | 1.61 | 1.61 | ns, Max |
| $T_{REG\_MUX}$ | Clock to AMUX – DMUX output. | 1.77 | 2.15 | 2.15 | ns, Max |
| $T_{REG\_M31}$ | Clock to DMUX output via M31 output. | 1.23 | 1.46 | 1.46 | ns, Max |
| **Setup and Hold Times Before/After Clock CLK** | | | | | |
| $T_{WS\_SHFREG}$/ $T_{WH\_SHFREG}$ | WE input. | 0.41/0.12 | 0.51/0.17 | 0.51/0.17 | ns, Min |
| $T_{CECK\_SHFREG}$/ $T_{CKCE\_SHFREG}$ | CE input to CLK. | 0.42/0.11 | 0.52/0.17 | 0.52/0.17 | ns, Min |
| $T_{DS\_SHFREG}$/ $T_{DH\_SHFREG}$ | A – D inputs to CLK. | 0.37/0.37 | 0.44/0.43 | 0.44/0.43 | ns, Min |
| **Clock CLK** | | | | | |
| $T_{MPW\_SHFREG}$ | Minimum pulse width. | 0.86 | 0.98 | 0.98 | ns, Min |

*Table 30:* **Block RAM and FIFO Switching Characteristics *(Cont'd)***

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| $F_{MAX\_CAS\_RF\_DELAYED\_WRITE}$ | When in cascade RF mode and there is a possibility of address overlap between port A and port B. | 362.19 | 297.35 | 297.35 | MHz |
| $F_{MAX\_FIFO}$ | FIFO in all modes without ECC. | 460.83 | 388.20 | 388.20 | MHz |
| $F_{MAX\_ECC}$ | Block RAM and FIFO in ECC configuration. | 365.10 | 297.53 | 297.53 | MHz |

**Notes:**

1. $T_{RCKO\_DOR}$ includes $T_{RCKO\_DOW}$, $T_{RCKO\_DOPR}$, and $T_{RCKO\_DOPW}$ as well as the B port equivalent timing parameters.
2. These parameters also apply to synchronous FIFO with DO_REG = 0.
3. $T_{RCKO\_DO}$ includes $T_{RCKO\_DOP}$ as well as the B port equivalent timing parameters.
4. These parameters also apply to multi-rate (asynchronous) and synchronous FIFO with DO_REG = 1.
5. $T_{RCKO\_FLAGS}$ includes the following parameters: $T_{RCKO\_AEMPTY}$, $T_{RCKO\_AFULL}$, $T_{RCKO\_EMPTY}$, $T_{RCKO\_FULL}$, $T_{RCKO\_RDERR}$, $T_{RCKO\_WRERR}$.
6. $T_{RCKO\_POINTERS}$ includes both $T_{RCKO\_RDCOUNT}$ and $T_{RCKO\_WRCOUNT}$.
7. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
8. These parameters include both A and B inputs as well as the parity inputs of A and B.
9. $T_{RCO\_FLAGS}$ includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
10. RDEN and WREN must be held Low prior to and during reset. The FIFO reset must be asserted for at least five positive clock edges of the slowest clock (WRCLK or RDCLK).

# DSP48E1 Switching Characteristics

*Table 31:* **DSP48E1 Switching Characteristics**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| **Setup and Hold Times of Data/Control Pins to the Input Register Clock** | | | | | |
| $T_{DSPDCK\_A\_AREG}$/ $T_{DSPCKD\_A\_AREG}$ | A input to A register CLK. | 0.30/ 0.13 | 0.37/ 0.14 | 0.37/ 0.14 | ns |
| $T_{DSPDCK\_B\_BREG}$/ $T_{DSPCKD\_B\_BREG}$ | B input to B register CLK. | 0.38/ 0.16 | 0.45/ 0.18 | 0.45/ 0.18 | ns |
| $T_{DSPDCK\_C\_CREG}$/ $T_{DSPCKD\_C\_CREG}$ | C input to C register CLK. | 0.20/ 0.19 | 0.24/ 0.21 | 0.24/ 0.21 | ns |
| $T_{DSPDCK\_D\_DREG}$/ $T_{DSPCKD\_D\_DREG}$ | D input to D register CLK. | 0.32/ 0.27 | 0.42/ 0.27 | 0.42/ 0.27 | ns |
| $T_{DSPDCK\_ACIN\_AREG}$/ $T_{DSPCKD\_ACIN\_AREG}$ | ACIN input to A register CLK. | 0.27/ 0.13 | 0.32/ 0.14 | 0.32/ 0.14 | ns |
| $T_{DSPDCK\_BCIN\_BREG}$/ $T_{DSPCKD\_BCIN\_BREG}$ | BCIN input to B register CLK. | 0.29/ 0.16 | 0.36/ 0.18 | 0.36/ 0.18 | ns |
| **Setup and Hold Times of Data Pins to the Pipeline Register Clock** | | | | | |
| $T_{DSPDCK\_\{A, B\}\_MREG\_MULT}$/ $T_{DSPCKD\_\{A, B\}\_MREG\_MULT}$ | {A, B} input to M register CLK using multiplier. | 2.76/ –0.01 | 3.29/ –0.01 | 3.29/ –0.01 | ns |
| $T_{DSPDCK\_\{A, D\}\_ADREG}$/ $T_{DSPCKD\_\{A, D\}\_ADREG}$ | {A, D} input to AD register CLK. | 1.48/ –0.02 | 1.76/ –0.02 | 1.76/ –0.02 | ns |
| **Setup and Hold Times of Data/Control Pins to the Output Register Clock** | | | | | |
| $T_{DSPDCK\_\{A, B\}\_PREG\_MULT}$/ $T_{DSPCKD\_\{A, B\}\ \_PREG\_MULT}$ | {A, B} input to P register CLK using multiplier. | 4.60/ –0.28 | 5.48/ –0.28 | 5.48/ –0.28 | ns |
| $T_{DSPDCK\_D\_PREG\_MULT}$/ $T_{DSPCKD\_D\_PREG\_MULT}$ | D input to P register CLK using multiplier. | 4.50/ –0.73 | 5.35/ –0.73 | 5.35/ –0.73 | ns |
| $T_{DSPDCK\_\{A, B\}\ \_PREG}$/ $T_{DSPCKD\_\{A, B\}\ \_PREG}$ | A or B input to P register CLK not using multiplier. | 1.98/ –0.28 | 2.35/ –0.28 | 2.35/ –0.28 | ns |
| $T_{DSPDCK\_C\_PREG}$/ $T_{DSPCKD\_C\_PREG}$ | C input to P register CLK not using multiplier. | 1.76/ –0.26 | 2.10/ –0.26 | 2.10/ –0.26 | ns |
| $T_{DSPDCK\_PCIN\_PREG}$/ $T_{DSPCKD\_PCIN\_PREG}$ | PCIN input to P register CLK. | 1.51/ –0.15 | 1.80/ –0.15 | 1.80/ –0.15 | ns |
| **Setup and Hold Times of the CE Pins** | | | | | |
| $T_{DSPDCK\_\{CEA;CEB\}\_\{AREG;BREG\}}$/ $T_{DSPCKD\_\{CEA;CEB\}\_\{AREG;BREG\}}$ | {CEA; CEB} input to {A; B} register CLK. | 0.42/ 0.08 | 0.52/ 0.11 | 0.52/ 0.11 | ns |
| $T_{DSPDCK\_CEC\_CREG}$/ $T_{DSPCKD\_CEC\_CREG}$ | CEC input to C register CLK. | 0.34/ 0.11 | 0.42/ 0.13 | 0.42/ 0.13 | ns |
| $T_{DSPDCK\_CED\_DREG}$/ $T_{DSPCKD\_CED\_DREG}$ | CED input to D register CLK. | 0.43/ –0.03 | 0.52/ –0.03 | 0.52/ –0.03 | ns |

*Table 31:* **DSP48E1 Switching Characteristics *(Cont'd)***

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| $T_{DSPDO\_PCIN\_CARRYCASCOUT}$ | PCIN input to CARRYCASCOUT output. | 1.56 | 1.85 | 1.85 | ns |
| **Clock to Outs from Output Register Clock to Output Pins** | | | | | |
| $T_{DSPCKO\_P\_PREG}$ | CLK PREG to P output. | 0.37 | 0.44 | 0.44 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_PREG}$ | CLK PREG to CARRYCASCOUT output. | 0.59 | 0.69 | 0.69 | ns |
| **Clock to Outs from Pipeline Register Clock to Output Pins** | | | | | |
| $T_{DSPCKO\_P\_MREG}$ | CLK MREG to P output. | 1.93 | 2.31 | 2.31 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_MREG}$ | CLK MREG to CARRYCASCOUT output. | 2.21 | 2.64 | 2.64 | ns |
| $T_{DSPCKO\_P\_ADREG\_MULT}$ | CLK ADREG to P output using multiplier. | 3.10 | 3.69 | 3.69 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_ADREG\_MULT}$ | CLK ADREG to CARRYCASCOUT output using multiplier. | 3.38 | 4.02 | 4.02 | ns |
| **Clock to Outs from Input Register Clock to Output Pins** | | | | | |
| $T_{DSPCKO\_P\_AREG\_MULT}$ | CLK AREG to P output using multiplier. | 4.51 | 5.37 | 5.37 | ns |
| $T_{DSPCKO\_P\_BREG}$ | CLK BREG to P output not using multiplier. | 1.87 | 2.22 | 2.22 | ns |
| $T_{DSPCKO\_P\_CREG}$ | CLK CREG to P output not using multiplier. | 1.93 | 2.30 | 2.30 | ns |
| $T_{DSPCKO\_P\_DREG\_MULT}$ | CLK DREG to P output using multiplier. | 4.48 | 5.32 | 5.32 | ns |
| **Clock to Outs from Input Register Clock to Cascading Output Pins** | | | | | |
| $T_{DSPCKO\_\{ACOUT;\ BCOUT\}\_\{AREG;\ BREG\}}$ | CLK (ACOUT, BCOUT) to {A,B} register output. | 0.73 | 0.87 | 0.87 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_\{AREG,\ BREG\}\_MULT}$ | CLK (AREG, BREG) to CARRYCASCOUT output using multiplier. | 4.79 | 5.70 | 5.70 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_\ BREG}$ | CLK BREG to CARRYCASCOUT output not using multiplier. | 2.15 | 2.55 | 2.55 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_\ DREG\_MULT}$ | CLK DREG to CARRYCASCOUT output using multiplier. | 4.76 | 5.65 | 5.65 | ns |
| $T_{DSPCKO\_CARRYCASCOUT\_\ CREG}$ | CLK CREG to CARRYCASCOUT output. | 2.21 | 2.63 | 2.63 | ns |
| **Maximum Frequency** | | | | | |
| $F_{MAX}$ | With all registers used. | 550.66 | 464.25 | 464.25 | MHz |
| $F_{MAX\_PATDET}$ | With pattern detector. | 465.77 | 392.93 | 392.93 | MHz |
| $F_{MAX\_MULT\_NOMREG}$ | Two register multiply without MREG. | 305.62 | 257.47 | 257.47 | MHz |
| $F_{MAX\_MULT\_NOMREG\_PATDET}$ | Two register multiply without MREG with pattern detect. | 277.62 | 233.92 | 233.92 | MHz |
| $F_{MAX\_PREADD\_MULT\_NOADREG}$ | Without ADREG. | 346.26 | 290.44 | 290.44 | MHz |
| $F_{MAX\_PREADD\_MULT\_NOADREG\_PATDET}$ | Without ADREG with pattern detect. | 346.26 | 290.44 | 290.44 | MHz |
| $F_{MAX\_NOPIPELINEREG}$ | Without pipeline registers (MREG, ADREG). | 227.01 | 190.69 | 190.69 | MHz |
| $F_{MAX\_NOPIPELINEREG\_PATDET}$ | Without pipeline registers (MREG, ADREG) with pattern detect. | 211.15 | 177.43 | 177.43 | MHz |

*Table 38:* **PLL Specification**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| PLL_$F_{BANDWIDTH}$ | Low PLL bandwidth at typical. | 1.00 | 1.00 | 1.00 | MHz |
| | High PLL bandwidth at typical.(1) | 4.00 | 4.00 | 4.00 | MHz |
| PLL_$T_{STATPHAOFFSET}$ | Static phase offset of the PLL outputs.(2) | 0.12 | 0.12 | 0.12 | ns |
| PLL_$T_{OUTJITTER}$ | PLL output jitter. | Note 3 | | | |
| PLL_$T_{OUTDUTY}$ | PLL output clock duty-cycle precision.(4) | 0.20 | 0.20 | 0.20 | ns |
| PLL_$T_{LOCKMAX}$ | PLL maximum lock time. | 100.00 | 100.00 | 100.00 | µs |
| PLL_$F_{OUTMAX}$ | PLL maximum output frequency. | 800.00 | 800.00 | 800.00 | MHz |
| PLL_$F_{OUTMIN}$ | PLL minimum output frequency.(5) | 6.25 | 6.25 | 6.25 | MHz |
| PLL_$T_{EXTFDVAR}$ | External clock feedback variation. | < 20% of clock input period or 1 ns Max | | | |
| PLL_$RST_{MINPULSE}$ | Minimum reset pulse width. | 5.00 | 5.00 | 5.00 | ns |
| PLL_$F_{PFDMAX}$ | Maximum frequency at the phase frequency detector. | 500.00 | 450.00 | 450.00 | MHz |
| PLL_$F_{PFDMIN}$ | Minimum frequency at the phase frequency detector. | 19.00 | 19.00 | 19.00 | MHz |
| PLL_$T_{FBDELAY}$ | Maximum delay in the feedback path. | 3 ns Max or one CLKIN cycle | | | |
| **Dynamic Reconfiguration Port (DRP) for PLL Before and After DCLK** | | | | | |
| $T_{PLLDCK\_DADDR}$/ $T_{PLLCKD\_DADDR}$ | Setup and hold of D address. | 1.40/0.15 | 1.63/0.15 | 1.63/0.15 | ns, Min |
| $T_{PLLDCK\_DI}$/ $T_{PLLCKD\_DI}$ | Setup and hold of D input. | 1.40/0.15 | 1.63/0.15 | 1.63/0.15 | ns, Min |
| $T_{PLLDCK\_DEN}$/ $T_{PLLCKD\_DEN}$ | Setup and hold of D enable. | 1.97/0.00 | 2.29/0.00 | 2.29/0.00 | ns, Min |
| $T_{PLLDCK\_DWE}$/ $T_{PLLCKD\_DWE}$ | Setup and hold of D write enable. | 1.40/0.15 | 1.63/0.15 | 1.63/0.15 | ns, Min |
| $T_{PLLCKO\_DRDY}$ | CLK to out of DRDY. | 0.72 | 0.99 | 0.99 | ns, Max |
| $F_{DCK}$ | DCLK frequency. | 200.00 | 200.00 | 200.00 | MHz, Max |

**Notes:**

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the *Clocking Wizard* [Ref 8].
4. Includes global clock buffer.
5. Calculated as FVCO/128 assuming output duty cycle is 50%.

## Device Pin-to-Pin Output Parameter Guidelines

*Table 39:* **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)[(1)]**

| Symbol | Description | Device | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | 1.0V | | 0.95V | |
| | | | -2 | -1 | -1L | |
| **SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM/PLL.** | | | | | | |
| $T_{ICKOF}$ | Clock-capable clock input and OUTFF at pins/banks closest to the BUFGs *without* MMCM/PLL (near clock region).[(2)] | XC7S6 | 5.55 | 6.50 | 6.50 | ns |
| | | XC7S15 | 5.55 | 6.50 | 6.50 | ns |
| | | XC7S25 | 5.55 | 6.44 | 6.44 | ns |
| | | XC7S50 | 5.71 | 6.62 | 6.62 | ns |
| | | XC7S75 | 5.73 | 6.71 | 6.71 | ns |
| | | XC7S100 | 5.73 | 6.71 | 6.71 | ns |
| | | XA7S6 | 5.55 | 6.50 | N/A | ns |
| | | XA7S15 | 5.55 | 6.50 | N/A | ns |
| | | XA7S25 | 5.55 | 6.44 | N/A | ns |
| | | XA7S50 | 5.71 | 6.62 | N/A | ns |
| | | XA7S75 | 5.73 | 6.71 | N/A | ns |
| | | XA7S100 | 5.73 | 6.71 | N/A | ns |

**Notes:**

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Refer to the *Die Level Bank Numbering Overview* section of the *7 Series FPGA Packaging and Pinout Specification* (UG475) [Ref 4].

*Table 41:* **Clock-Capable Clock Input to Output Delay With MMCM**[(1)]

| Symbol | Description | Device | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | 1.0V | | 0.95V | |
| | | | -2 | -1 | -1L | |
| **SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *with* MMCM.** | | | | | | |
| $T_{ICKOFMMCMCC}$ | Clock-capable clock input and OUTFF *with* MMCM.[(2)] | XC7S6 | 1.03 | 1.03 | 1.03 | ns |
| | | XC7S15 | 1.03 | 1.03 | 1.03 | ns |
| | | XC7S25 | 1.00 | 1.00 | 1.00 | ns |
| | | XC7S50 | 1.00 | 1.00 | 1.00 | ns |
| | | XC7S75 | 1.00 | 1.00 | 1.00 | ns |
| | | XC7S100 | 1.00 | 1.00 | 1.00 | ns |
| | | XA7S6 | 1.03 | 1.03 | N/A | ns |
| | | XA7S15 | 1.03 | 1.03 | N/A | ns |
| | | XA7S25 | 1.00 | 1.00 | N/A | ns |
| | | XA7S50 | 1.00 | 1.00 | N/A | ns |
| | | XA7S75 | 1.00 | 1.00 | N/A | ns |
| | | XA7S100 | 1.00 | 1.00 | N/A | ns |

**Notes:**

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

# XADC Specifications

The *7 Series FPGAs Overview* (DS180) [Ref 1] and *XA Spartan-7 Automotive FPGA Data Sheet: Overview* (DS171) [Ref 2] list the devices that contain a 7 series XADC dual 12-Bit 1 MSPS analog-to-digital converter.

*Table 50:* **XADC Specifications**

| Parameter | Symbol | Comments/Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCADC}$ = 1.8V ± 5%, $V_{REFP}$ = 1.25V, $V_{REFN}$ = 0V, ADCCLK = 26 MHz, $-55°C \le T_j \le 125°C$. Typical values at $T_j$ = +40°C. | | | | | | |
| **ADC Accuracy**(1) | | | | | | |
| Resolution | | | 12 | – | – | Bits |
| Integral nonlinearity(2) | INL | $-40°C \le T_j \le 100°C$ | – | – | ±2 | LSBs |
| | | $-55°C \le T_j < -40°C$; $100°C < T_j \le 125°C$ | – | – | ±3 | LSBs |
| Differential nonlinearity | DNL | No missing codes, guaranteed monotonic. | – | – | ±1 | LSBs |
| Offset error | Unipolar | $-40°C \le T_j \le 100°C$ | – | – | ±8 | LSBs |
| | | $-55°C \le T_j < -40°C$; $100°C < T_j \le 125°C$ | – | – | ±12 | LSBs |
| | Bipolar | $-55°C \le T_j \le 125°C$ | – | – | ±4 | LSBs |
| Gain error | | | – | – | ±0.5 | % |
| Offset matching | | | – | – | 4 | LSBs |
| Gain matching | | | – | – | 0.3 | % |
| Sample rate | | | – | – | 1 | MS/s |
| Signal to noise ratio(2) | SNR | $F_{SAMPLE}$ = 500 KS/s, $F_{IN}$ = 20 kHz | 60 | – | – | dB |
| RMS code noise | | External 1.25V reference. | – | – | 2 | LSBs |
| | | On-chip reference. | – | 3 | – | LSBs |
| Total harmonic distortion(2) | THD | $F_{SAMPLE}$ = 500 KS/s, $F_{IN}$ = 20 kHz | 70 | – | – | dB |
| **Analog Inputs**(3) | | | | | | |
| ADC input ranges | | Unipolar operation. | 0 | – | 1 | V |
| | | Bipolar operation. | –0.5 | – | +0.5 | V |
| | | Unipolar common mode range (FS input). | 0 | – | +0.5 | V |
| | | Bipolar common mode range (FS input). | +0.5 | – | +0.6 | V |
| Maximum external channel input ranges | | Adjacent analog channels set within these ranges should not corrupt measurements on adjacent channels. | –0.1 | – | $V_{CCADC}$ | V |
| Full-resolution bandwidth | FRBW | Auxiliary channel full resolution bandwidth. | 250 | – | – | kHz |
| **On-chip Sensors** | | | | | | |
| Temperature sensor error | | $-40°C \le T_j \le 100°C$ | – | – | ±4 | °C |
| | | $-55°C \le T_j < -40°C$; $100°C < T_j \le 125°C$ | – | – | ±6 | °C |
| Supply sensor error | | $-40°C \le T_j \le 100°C$ | – | – | ±1 | % |
| | | $-55°C \le T_j < -40°C$; $100°C < T_j \le 125°C$ | – | – | ±2 | % |

*Table 50:* **XADC Specifications *(Cont'd)***

| Parameter | Symbol | Comments/Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Conversion Rate(4)** | | | | | | |
| Conversion time: continuous | $t_{CONV}$ | Number of ADCCLK cycles. | 26 | – | 32 | Cycles |
| Conversion time: event | $t_{CONV}$ | Number of CLK cycles. | – | – | 21 | Cycles |
| DRP clock frequency | DCLK | DRP clock frequency. | 8 | – | 250 | MHz |
| ADC clock frequency | ADCCLK | Derived from DCLK. | 1 | – | 26 | MHz |
| DCLK duty cycle | | | 40 | – | 60 | % |
| **XADC Reference(5)** | | | | | | |
| External reference | $V_{REFP}$ | Externally supplied reference voltage. | 1.20 | 1.25 | 1.30 | V |
| On-chip reference | | Ground $V_{REFP}$ pin to AGND, $-40°C \le T_j \le 100°C$ | 1.2375 | 1.25 | 1.2625 | V |
| | | Ground VREFP pin to AGND, $-55°C \le T_j < -40°C$; $100°C < T_j \le 125°C$ | 1.225 | 1.25 | 1.275 | V |

**Notes:**

1. Offset and gain errors are removed by enabling the XADC automatic gain calibration feature. The values are specified for when this feature is enabled.
2. Only specified for bitstream option XADCEnhancedLinearity = ON.
3. For a detailed description, see the *ADC* chapter in the *7 Series FPGAs and Zynq-7000 AP SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480) [Ref 9].
4. For a detailed description, see the *Timing* chapter in the *7 Series FPGAs and Zynq-7000 AP SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480) [Ref 9].
5. Any variation in the reference voltage from the nominal $V_{REFP}$ = 1.25V and $V_{REFN}$ = 0V will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted.

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