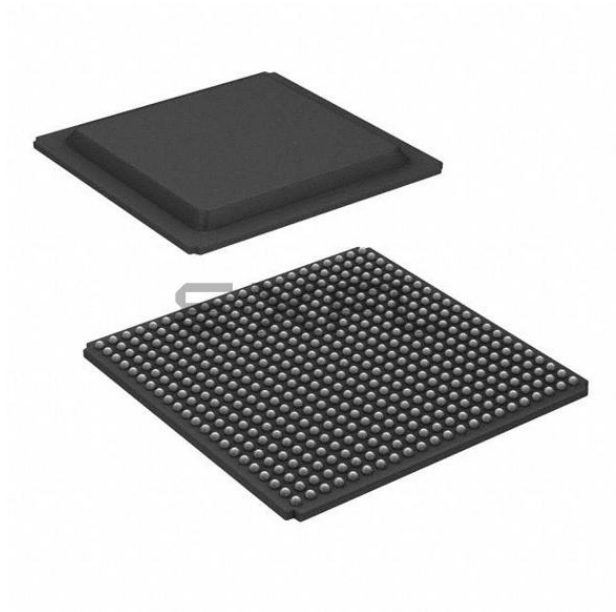
AMD Xilinx - XC7S75-1FGGA484I Datasheet



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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	6000
Number of Logic Elements/Cells	76800
Total RAM Bits	4331520
Number of I/O	338
Number of Gates	-
Voltage - Supply	0.95V ~ 1.05V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7s75-1fgga484i

Table 3: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Min	Typ[1]	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost).	0.75	–	–	V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost).	1.5	–	–	V
I_{REF}	V_{REF} leakage current per pin.	–	–	15	µA
I_L	Input or output leakage current per pin (sample-tested).	–	–	15	µA
C_{IN}[2]	Die input capacitance at the pad.	–	–	8	pF
I_{RPU}	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 3.3V.	90	–	330	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 2.5V.	68	–	250	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 1.8V.	34	–	220	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 1.5V.	23	–	150	µA
	Pad pull-up (when selected) at V_{IN} = 0V, V_{CCO} = 1.2V.	12	–	120	µA
I_{RPD}	Pad pull-down (when selected) at V_{IN} = 3.3V.	68	–	330	µA
I_{CCADC}	Analog supply current, analog circuits in powered up state.	–	–	25	mA
I_{BATT}[3]	Battery supply current.	–	–	150	nA
R_{IN_TERM}[4]	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 (UNTUNED_SPLIT_40).	28	40	55	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 (UNTUNED_SPLIT_50).	35	50	65	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 (UNTUNED_SPLIT_60).	44	60	83	Ω
n	Temperature diode ideality factor.	–	1.010	–	–
r	Temperature diode series resistance.	–	2	–	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. This measurement represents the die capacitance at the pad, not including the package.
3. Maximum value specified for worst case process at 25°C.
4. Termination resistance to a V_{CCO}/2 level.

Table 5: **Typical Quiescent Supply Current[(1)(2)(3)] *(Cont'd)***

Symbol	Description	Device	Speed Grade						Units
			1.0V					0.95V	
			-2C	-2I	-1C	-1I	-1Q	-1LI	
I_{CCOQ}	Quiescent V_{CCO} supply current.	XC7S6	1	1	1	1	1	1	mA
		XC7S15	1	1	1	1	1	1	mA
		XC7S25	1	1	1	1	1	1	mA
		XC7S50	1	1	1	1	1	1	mA
		XC7S75	4	4	4	4	4	4	mA
		XC7S100	4	4	4	4	4	4	mA
		XA7S6	N/A	1	N/A	1	1	N/A	mA
		XA7S15	N/A	1	N/A	1	1	N/A	mA
		XA7S25	N/A	1	N/A	1	1	N/A	mA
		XA7S50	N/A	1	N/A	1	1	N/A	mA
		XA7S75	N/A	4	N/A	4	4	N/A	mA
		XA7S100	N/A	4	N/A	4	4	N/A	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current.	XC7S6	10	10	10	10	10	10	mA
		XC7S15	10	10	10	10	10	10	mA
		XC7S25	13	13	13	13	13	13	mA
		XC7S50	22	22	22	22	22	20	mA
		XC7S75	43	43	43	43	43	43	mA
		XC7S100	43	43	43	43	43	43	mA
		XA7S6	N/A	10	N/A	10	10	N/A	mA
		XA7S15	N/A	10	N/A	10	10	N/A	mA
		XA7S25	N/A	13	N/A	13	13	N/A	mA
		XA7S50	N/A	22	N/A	22	22	N/A	mA
		XA7S75	N/A	43	N/A	43	43	N/A	mA
		XA7S100	N/A	43	N/A	43	43	N/A	mA

Table 5: **Typical Quiescent Supply Current[(1)(2)(3)] *(Cont'd)***

Symbol	Description	Device	Speed Grade						Units
			1.0V					0.95V	
			-2C	-2I	-1C	-1I	-1Q	-1LI	
$I_{CCBRAMQ}$	Quiescent V_{CCBRAM} supply current.	XC7S6	1	1	1	1	1	1	mA
		XC7S15	1	1	1	1	1	1	mA
		XC7S25	1	1	1	1	1	1	mA
		XC7S50	2	2	2	2	2	1	mA
		XC7S75	9	9	9	9	9	8	mA
		XC7S100	9	9	9	9	9	8	mA
		XA7S6	N/A	1	N/A	1	1	N/A	mA
		XA7S15	N/A	1	N/A	1	1	N/A	mA
		XA7S25	N/A	1	N/A	1	1	N/A	mA
		XA7S50	N/A	2	N/A	2	2	N/A	mA
		XA7S75	N/A	9	N/A	9	9	N/A	mA
		XA7S100	N/A	9	N/A	9	9	N/A	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperature (T_j) with single-ended SelectIO™ resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the *Xilinx Power Estimator* spreadsheet tool [Ref 6] to estimate static power consumption for conditions other than those specified.

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCBRAM} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If V_{CCAUX} and V_{CCO} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously.

For V_{CCO} voltages of 3.3V in HR I/O banks and configuration bank 0 the following conditions apply.

- The voltage difference between V_{CCO} and V_{CCAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

There is no recommended sequence for supplies not discussed in this section.

Table 14: **Spartan-7 Device Production Software and Speed Specification Release**

Device	V_{CCINT} Operating Voltage, Speed Grade, and Temperature Range					
	1.0V					0.95V
	-2C	-2I	-1C	-1I	-1Q	-1LI
XC7S6	Vivado tools 2018.2 v1.22				Vivado tools 2018.2.1 v1.23	Vivado tools 2018.2 v1.22
XC7S15	Vivado tools 2018.2 v1.22				Vivado tools 2018.2.1 v1.23	Vivado tools 2018.2 v1.22
XC7S25	Vivado tools 2017.4 v1.20				Vivado tools 2018.1 v1.21	Vivado tools 2017.4 v1.20
XC7S50	Vivado tools 2017.2 v1.17				Vivado tools 2017.3 v1.19	Vivado tools 2017.2 v1.17
XC7S75	Vivado tools 2018.1 v1.21				Vivado tools 2018.2.1 v1.23	Vivado tools 2018.1 v1.21
XC7S100	Vivado tools 2018.1 v1.21				Vivado tools 2018.2.1 v1.23	Vivado tools 2018.1 v1.21
XA7S6	N/A	Vivado tools 2018.2.1 v1.16	N/A	Vivado tools 2018.2.1 v1.16		N/A
XA7S15	N/A	Vivado tools 2018.2.1 v1.16	N/A	Vivado tools 2018.2.1 v1.16		N/A
XA7S25	N/A	Vivado tools 2018.1 v1.15	N/A	Vivado tools 2018.1 v1.15		N/A
XA7S50	N/A	Vivado tools 2017.3 v1.12	N/A	Vivado tools 2017.3 v1.12		N/A
XA7S75	N/A	Vivado tools 2018.2.1 v1.16	N/A	Vivado tools 2018.2.1 v1.16		N/A
XA7S100	N/A	Vivado tools 2018.2.1 v1.16	N/A	Vivado tools 2018.2.1 v1.16		N/A

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Spartan-7 FPGAs. These values are subject to the same guidelines as the AC Switching Characteristics, page 12.

Table 15: **Networking Applications Interface Performances**

Description	V_{CCINT} Operating Voltage, Speed Grade, and Temperature Range			Units
	1.0V		0.95V	
	-2C/-2I	-1C/-1I/-1Q	-1LI	
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	680	600	600	Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14)	1250	950	950	Mb/s
SDR LVDS receiver(1)	680	600	600	Mb/s

Table 17: **IOB High Range (HR) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}			T_{IOOP}			T_{IOTP}			Units
	V_{CCINT} Operating Voltage and Speed Grade									
	1.0V		0.95V	1.0V		0.95V	1.0V		0.95V	
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
HSTL_II_18_F	0.75	0.81	0.81	1.24	1.49	1.49	1.27	1.51	1.51	ns
DIFF_HSTL_I_F	0.76	0.83	0.83	1.30	1.56	1.56	1.33	1.57	1.57	ns
DIFF_HSTL_II_F	0.76	0.83	0.83	1.33	1.59	1.59	1.36	1.60	1.60	ns
DIFF_HSTL_I_18_F	0.79	0.86	0.86	1.33	1.59	1.59	1.36	1.60	1.60	ns
DIFF_HSTL_II_18_F	0.78	0.85	0.85	1.33	1.59	1.59	1.36	1.60	1.60	ns
LVCMOS33_S4	1.34	1.41	1.41	3.93	4.18	4.18	3.96	4.20	4.20	ns
LVCMOS33_S8	1.34	1.41	1.41	3.65	3.90	3.90	3.68	3.91	3.91	ns
LVCMOS33_S12	1.34	1.41	1.41	3.21	3.46	3.46	3.24	3.48	3.48	ns
LVCMOS33_S16	1.34	1.41	1.41	3.52	3.77	3.77	3.55	3.79	3.79	ns
LVCMOS33_F4	1.34	1.41	1.41	3.38	3.64	3.64	3.41	3.65	3.65	ns
LVCMOS33_F8	1.34	1.41	1.41	2.87	3.12	3.12	2.90	3.13	3.13	ns
LVCMOS33_F12	1.34	1.41	1.41	2.68	2.93	2.93	2.71	2.95	2.95	ns
LVCMOS33_F16	1.34	1.41	1.41	2.68	2.93	2.93	2.71	2.95	2.95	ns
LVCMOS25_S4	1.20	1.27	1.27	3.26	3.51	3.51	3.29	3.52	3.52	ns
LVCMOS25_S8	1.20	1.27	1.27	3.01	3.26	3.26	3.04	3.27	3.27	ns
LVCMOS25_S12	1.20	1.27	1.27	2.60	2.85	2.85	2.63	2.87	2.87	ns
LVCMOS25_S16	1.20	1.27	1.27	2.94	3.20	3.20	2.97	3.21	3.21	ns
LVCMOS25_F4	1.20	1.27	1.27	2.87	3.12	3.12	2.90	3.13	3.13	ns
LVCMOS25_F8	1.20	1.27	1.27	2.30	2.56	2.56	2.33	2.57	2.57	ns
LVCMOS25_F12	1.20	1.27	1.27	2.29	2.54	2.54	2.32	2.55	2.55	ns
LVCMOS25_F16	1.20	1.27	1.27	2.13	2.39	2.39	2.16	2.40	2.40	ns
LVCMOS18_S4	0.83	0.89	0.89	1.74	1.99	1.99	1.77	2.01	2.01	ns
LVCMOS18_S8	0.83	0.89	0.89	2.30	2.56	2.56	2.33	2.57	2.57	ns
LVCMOS18_S12	0.83	0.89	0.89	2.30	2.56	2.56	2.33	2.57	2.57	ns
LVCMOS18_S16	0.83	0.89	0.89	1.65	1.90	1.90	1.68	1.91	1.91	ns
LVCMOS18_S24	0.83	0.89	0.89	1.72	1.98	1.98	1.75	1.99	1.99	ns
LVCMOS18_F4	0.83	0.89	0.89	1.57	1.82	1.82	1.60	1.84	1.84	ns
LVCMOS18_F8	0.83	0.89	0.89	1.80	2.06	2.06	1.83	2.07	2.07	ns
LVCMOS18_F12	0.83	0.89	0.89	1.80	2.06	2.06	1.83	2.07	2.07	ns
LVCMOS18_F16	0.83	0.89	0.89	1.52	1.77	1.77	1.55	1.79	1.79	ns
LVCMOS18_F24	0.83	0.89	0.89	1.46	1.71	1.71	1.49	1.73	1.73	ns
LVCMOS15_S4	0.86	0.93	0.93	2.18	2.43	2.43	2.21	2.45	2.45	ns
LVCMOS15_S8	0.86	0.93	0.93	2.21	2.46	2.46	2.24	2.48	2.48	ns
LVCMOS15_S12	0.86	0.93	0.93	1.71	1.96	1.96	1.74	1.98	1.98	ns
LVCMOS15_S16	0.86	0.93	0.93	1.71	1.96	1.96	1.74	1.98	1.98	ns
LVCMOS15_F4	0.86	0.93	0.93	1.97	2.23	2.23	2.00	2.24	2.24	ns

Table 20: **Output Delay Measurement Methodology**

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
LVCMOS, 1.2V	LVCMOS12	1M	0	0.6	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 3.3V	LVCMOS33	1M	0	1.65	0
LVTTL, 3.3V	LVTTL	1M	0	1.65	0
PCI33, 3.3V	PCI33_3	25	10	1.65	0
HSTL (high-speed transceiver logic), Class I, 1.2V	HSTL_I_12	50	0	V_{REF}	0.6
HSTL, Class I, 1.5V	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II, 1.5V	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	50	0	V_{REF}	0.6
SSTL12, 1.2V	SSTL12	50	0	V_{REF}	0.6
SSTL135/SSTL135_R, 1.35V	SSTL135, SSTL135_R	50	0	V_{REF}	0.675
SSTL15/SSTL15_R, 1.5V	SSTL15, SSTL15_R	50	0	V_{REF}	0.75
SSTL (stub-series terminated logic), Class I & Class II, 1.8V	SSTL18_I, SSTL18_II	50	0	V_{REF}	0.9
DIFF_MOBILE_DDR, 1.8V	DIFF_MOBILE_DDR	50	0	V_{REF}	0.9
DIFF_HSTL, Class I, 1.2V	DIFF_HSTL_I_12	50	0	V_{REF}	0.6
DIFF_HSTL, Class I & II, 1.5V	DIFF_HSTL_I, DIFF_HSTL_II	50	0	V_{REF}	0.75
DIFF_HSTL, Class I & II, 1.8V	DIFF_HSTL_I_18, DIFF_HSTL_II_18	50	0	V_{REF}	0.9
DIFF_HSUL_12, 1.2V	DIFF_HSUL_12	50	0	V_{REF}	0.6
DIFF_SSTL135/DIFF_SSTL135_R, 1.35V	DIFF_SSTL135, DIFF_SSTL135_R	50	0	V_{REF}	0.675
DIFF_SSTL15/DIFF_SSTL15_R, 1.5V	DIFF_SSTL15, DIFF_SSTL15_R	50	0	V_{REF}	0.75
DIFF_SSTL18, Class I & II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	50	0	V_{REF}	0.9
LVDS, 2.5V	LVDS_25	100	0	0[2]	0
BLVDS (Bus LVDS), 2.5V	BLVDS_25	100	0	0[2]	0
Mini LVDS, 2.5V	MINI_LVDS_25	100	0	0[2]	0
PPDS_25	PPDS_25	100	0	0[2]	0
RSDS_25	RSDS_25	100	0	0[2]	0
TMDS_33	TMDS_33	50	0	0[2]	3.3

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Input/Output Logic Switching Characteristics

Table 21: **ILOGIC Switching Characteristics**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Setup/Hold					
T_{ICE1CK}/T_{ICKCE1}	CE1 pin setup/hold with respect to CLK.	0.54/0.02	0.76/0.02	0.76/0.02	ns
T_{ISRCK}/T_{ICKSR}	SR pin setup/hold with respect to CLK.	0.70/0.01	1.13/0.01	1.13/0.01	ns
T_{IDOCK}/T_{IOCKD}	D pin setup/hold with respect to CLK without delay.	0.01/0.29	0.01/0.33	0.01/0.33	ns
T_{IDOCKD}/T_{IOCKDD}	DDLY pin setup/hold with respect to CLK (using IDELAY).	0.02/0.29	0.02/0.33	0.02/0.33	ns
Combinatorial					
T_{IDI}	D pin to O pin propagation delay, no delay.	0.11	0.13	0.13	ns
T_{IDID}	DDLY pin to O pin propagation delay (using IDELAY).	0.12	0.14	0.14	ns
Sequential Delays					
T_{IDLO}	D pin to Q1 pin using flip-flop as a latch without delay.	0.44	0.51	0.51	ns
T_{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY).	0.44	0.51	0.51	ns
T_{ICKQ}	CLK to Q outputs.	0.57	0.66	0.66	ns
T_{RQ_ILOGIC}	SR pin to OQ/TQ out.	1.08	1.32	1.32	ns
T_{GSRQ_ILOGIC}	Global set/reset to Q outputs.	7.60	10.51	10.51	ns
Set/Reset					
T_{RPW_ILOGIC}	Minimum pulse width, SR inputs.	0.72	0.72	0.72	ns, Min

Input Serializer/Deserializer Switching Characteristics

Table 23: **ISERDES Switching Characteristics**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Setup/Hold for Control Lines					
$T_{ISCCK\_BITSLIP}$/ $T_{ISCKC\_BITSLIP}$	BITSLIP pin setup/hold with respect to CLKDIV.	0.02/0.15	0.02/0.17	0.02/0.17	ns
T_{ISCCK_CE}/ T_{ISCKC_CE}	CE pin setup/hold with respect to CLK (for CE1).	0.50/–0.01	0.72/–0.01	0.72/–0.01	ns
T_{ISCCK_CE2}/ T_{ISCKC_CE2}	CE pin setup/hold with respect to CLKDIV (for CE2).	–0.10/0.36	–0.10/0.40	–0.10/0.40	ns
Setup/Hold for Data Lines					
T_{ISDCK_D}/ T_{ISCKD_D}	D pin setup/hold with respect to CLK.	–0.02/0.14	–0.02/0.17	–0.02/0.17	ns
T_{ISDCK_DDLY}/ T_{ISCKD_DDLY}	DDLY pin setup/hold with respect to CLK (using IDELAY).(1)	–0.02/0.14	–0.02/0.17	–0.02/0.17	ns
$T_{ISDCK\_D\_DDR}$/ $T_{ISCKD\_D\_DDR}$	D pin setup/hold with respect to CLK at DDR mode.	–0.02/0.14	–0.02/0.17	–0.02/0.17	ns
$T_{ISDCK\_DDLY\_DDR}$/ $T_{ISCKD\_DDLY\_DDR}$	D pin setup/hold with respect to CLK at DDR mode (using IDELAY).(1)	0.14/0.14	0.17/0.17	0.17/0.17	ns
Sequential Delays					
T_{ISCKO_Q}	CLKDIV to out at Q pin.	0.54	0.66	0.66	ns
Propagation Delays					
T_{ISDO_DO}	D input to DO output pin.	0.11	0.13	0.13	ns

Notes:

1. Recorded at 0 tap value.

Table 26: **IO_FIFO Switching Characteristics**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
IO_FIFO Clock to Out Delays					
T_{OFFCKO_DO}	RDCLK to Q outputs.	0.60	0.68	0.68	ns
T_{CKO_FLAGS}	Clock to IO_FIFO flags.	0.61	0.77	0.77	ns
Setup/Hold					
T_{CCK_D}/T_{CKC_D}	D inputs to WRCLK.	0.51/0.02	0.58/0.02	0.58/0.02	ns
T_{IFFCCK_WREN}/ T_{IFFCKC_WREN}	WREN to WRCLK.	0.47/–0.01	0.53/–0.01	0.53/–0.01	ns
T_{OFFCCK_RDEN}/ T_{OFFCKC_RDEN}	RDEN to RDCLK.	0.58/0.02	0.66/0.02	0.66/0.02	ns
Minimum Pulse Width					
$T_{PWH\_IO\_FIFO}$	RESET, RDCLK, WRCLK.	2.15	2.15	2.15	ns
$T_{PWL\_IO\_FIFO}$	RESET, RDCLK, WRCLK.	2.15	2.15	2.15	ns
Maximum Frequency					
F_{MAX}	RDCLK and WRCLK.	200.00	200.00	200.00	MHz

Table 30: **Block RAM and FIFO Switching Characteristics *(Cont'd)***

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
$T_{RDCK\_DI\_ECC\_FIFO}$/ $T_{RCKD\_DI\_ECC\_FIFO}$	DIN inputs with FIFO ECC in standard mode.(8)	1.15/0.59	1.32/0.64	1.32/0.64	ns, Min
$T_{RCCK\_INJECTBITERR}$/ $T_{RCKC\_INJECTBITERR}$	Inject single/double bit error in ECC mode.	0.64/0.37	0.74/0.40	0.74/0.40	ns, Min
T_{RCCK_EN}/T_{RCKC_EN}	Block RAM enable (EN) input.	0.39/0.21	0.45/0.23	0.45/0.23	ns, Min
T_{RCCK_REGCE}/ T_{RCKC_REGCE}	CE input of output register.	0.29/0.15	0.36/0.16	0.36/0.16	ns, Min
T_{RCCK_RSTREG}/ T_{RCKC_RSTREG}	Synchronous RSTREG input.	0.32/0.07	0.35/0.07	0.35/0.07	ns, Min
T_{RCCK_RSTRAM}/ T_{RCKC_RSTRAM}	Synchronous RSTRAM input.	0.34/0.43	0.36/0.46	0.36/0.46	ns, Min
T_{RCCK_WEA}/T_{RCKC_WEA}	Write enable (WE) input (block RAM only).	0.48/0.19	0.54/0.20	0.54/0.20	ns, Min
T_{RCCK_WREN}/ T_{RCKC_WREN}	WREN FIFO inputs.	0.46/0.35	0.47/0.43	0.47/0.43	ns, Min
T_{RCCK_RDEN}/ T_{RCKC_RDEN}	RDEN FIFO inputs.	0.43/0.35	0.43/0.43	0.43/0.43	ns, Min
Reset Delays					
T_{RCO_FLAGS}	Reset RST to FIFO flags/pointers.(9)	0.98	1.10	1.10	ns, Max
T_{RREC_RST}/T_{RREM_RST}	FIFO reset recovery and removal timing.(10)	2.07/–0.81	2.37/–0.81	2.37/–0.81	ns, Max
Maximum Frequency					
$F_{MAX\_BRAM\_WF\_NC}$	Block RAM (write first and no change modes) when not in SDP RF mode.	460.83	388.20	388.20	MHz
$F_{MAX\_BRAM\_RF\_PERFORMANCE}$	Block RAM (read first, performance mode) when in SDP RF mode but no address overlap between port A and port B.	460.83	388.20	388.20	MHz
$F_{MAX\_BRAM\_RF\_DELAYED\_WRITE}$	Block RAM (read first, delayed write mode) when in SDP RF mode and there is possibility of overlap between port A and port B addresses.	404.53	339.67	339.67	MHz
$F_{MAX\_CAS\_WF\_NC}$	Block RAM cascade (write first, no change mode) when cascade but not in RF mode.	418.59	345.78	345.78	MHz
$F_{MAX\_CAS\_RF\_PERFORMANCE}$	Block RAM cascade (read first, performance mode) when in cascade with RF mode and no possibility of address overlap/one port is disabled.	418.59	345.78	345.78	MHz

Table 31: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
$T_{DSPDCK\_CEM\_MREG}$/ $T_{DSPCKD\_CEM\_MREG}$	CEM input to M register CLK.	0.21/ 0.20	0.27/ 0.23	0.27/ 0.23	ns
$T_{DSPDCK\_CEP\_PREG}$/ $T_{DSPCKD\_CEP\_PREG}$	CEP input to P register CLK.	0.43/ 0.01	0.53/ 0.01	0.53/ 0.01	ns
Setup and Hold Times of the RST Pins					
$T_{DSPDCK\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$/ $T_{DSPCKD\_\{RSTA; RSTB\}\_\{AREG; BREG\}}$	{RSTA, RSTB} input to {A, B} register CLK.	0.46/ 0.13	0.55/ 0.15	0.55/ 0.15	ns
$T_{DSPDCK\_RSTC\_CREG}$/ $T_{DSPCKD\_RSTC\_CREG}$	RSTC input to C register CLK.	0.08/ 0.11	0.09/ 0.12	0.09/ 0.12	ns
$T_{DSPDCK\_RSTD\_DREG}$/ $T_{DSPCKD\_RSTD\_DREG}$	RSTD input to D register CLK	0.50/ 0.08	0.59/ 0.09	0.59/ 0.09	ns
$T_{DSPDCK\_RSTM\_MREG}$/ $T_{DSPCKD\_RSTM\_MREG}$	RSTM input to M register CLK	0.23/ 0.24	0.27/ 0.28	0.27/ 0.28	ns
$T_{DSPDCK\_RSTP\_PREG}$/ $T_{DSPCKD\_RSTP\_PREG}$	RSTP input to P register CLK	0.30/ 0.01	0.35/ 0.01	0.35/ 0.01	ns
Combinatorial Delays from Input Pins to Output Pins					
$T_{DSPDO\_A\_CARRYOUT\_MULT}$	A input to CARRYOUT output using multiplier.	4.35	5.18	5.18	ns
$T_{DSPDO\_D\_P\_MULT}$	D input to P output using multiplier.	4.26	5.07	5.07	ns
$T_{DSPDO\_B\_P}$	B input to P output not using multiplier.	1.75	2.08	2.08	ns
$T_{DSPDO\_C\_P}$	C input to P output.	1.53	1.82	1.82	ns
Combinatorial Delays from Input Pins to Cascading Output Pins					
$T_{DSPDO\_\{A; B\}\_\{ACOUT; BCOUT\}}$	{A, B} input to {ACOUT, BCOUT} output.	0.63	0.74	0.74	ns
$T_{DSPDO\_\{A, B\}\_CARRYCASCOUT\_MULT}$	{A, B} input to CARRYCASCOUT output using multiplier.	4.65	5.54	5.54	ns
$T_{DSPDO\_D\_CARRYCASCOUT\_MULT}$	D input to CARRYCASCOUT output using multiplier.	4.54	5.40	5.40	ns
$T_{DSPDO\_\{A, B\}\_CARRYCASCOUT}$	{A, B} input to CARRYCASCOUT output not using multiplier.	2.03	2.41	2.41	ns
$T_{DSPDO\_C\_CARRYCASCOUT}$	C input to CARRYCASCOUT output.	1.81	2.15	2.15	ns
Combinatorial Delays from Cascading Input Pins to All Output Pins					
$T_{DSPDO\_ACIN\_P\_MULT}$	ACIN input to P output using multiplier.	4.19	5.00	5.00	ns
$T_{DSPDO\_ACIN\_P}$	ACIN input to P output not using multiplier.	1.57	1.88	1.88	ns
$T_{DSPDO\_ACIN\_ACOUT}$	ACIN input to ACOUT output.	0.44	0.53	0.53	ns
$T_{DSPDO\_ACIN\_CARRYCASCOUT\_MULT}$	ACIN input to CARRYCASCOUT output using multiplier.	4.47	5.33	5.33	ns
$T_{DSPDO\_ACIN\_CARRYCASCOUT}$	ACIN input to CARRYCASCOUT output not using multiplier.	1.85	2.21	2.21	ns
$T_{DSPDO\_PCIN\_P}$	PCIN input to P output.	1.28	1.52	1.52	ns

MMCM Switching Characteristics

Table 37: **MMCM Specification**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
MMCM_F_{INMAX}	Maximum input clock frequency.	800.00	800.00	800.00	MHz
MMCM_F_{INMIN}	Minimum input clock frequency.	10.00	10.00	10.00	MHz
MMCM_$F_{INJITTER}$	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max			
MMCM_F_{INDUTY}	Allowable input duty cycle: 10—49 MHz.	25	25	25	%
	Allowable input duty cycle: 50—199 MHz.	30	30	30	%
	Allowable input duty cycle: 200—399 MHz.	35	35	35	%
	Allowable input duty cycle: 400—499 MHz.	40	40	40	%
	Allowable input duty cycle: > 500 MHz.	45	45	45	%
MMCM_F_{MIN_PSCLK}	Minimum dynamic phase-shift clock frequency.	0.01	0.01	0.01	MHz
MMCM_F_{MAX_PSCLK}	Maximum dynamic phase-shift clock frequency.	500.00	450.00	450.00	MHz
MMCM_F_{VCOMIN}	Minimum MMCM VCO frequency.	600.00	600.00	600.00	MHz
MMCM_F_{VCOMAX}	Maximum MMCM VCO frequency.	1440.00	1200.00	1200.00	MHz
MMCM_$F_{BANDWIDTH}$	Low MMCM bandwidth at typical.(1)	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical.(1)	4.00	4.00	4.00	MHz
MMCM_$T_{STATPHAOFFSET}$	Static phase offset of the MMCM outputs.(2)	0.12	0.12	0.12	ns
MMCM_$T_{OUTJITTER}$	MMCM output jitter.	Note 3			
MMCM_$T_{OUTDUTY}$	MMCM output clock duty-cycle precision.(4)	0.20	0.20	0.20	ns
MMCM_$T_{LOCKMAX}$	MMCM maximum lock time.	100.00	100.00	100.00	µs
MMCM_F_{OUTMAX}	MMCM maximum output frequency.	800.00	800.00	800.00	MHz
MMCM_F_{OUTMIN}	MMCM minimum output frequency.(5)(6)	4.69	4.69	4.69	MHz
MMCM_$T_{EXTFDVAR}$	External clock feedback variation.	< 20% of clock input period or 1 ns Max			
MMCM_$RST_{MINPULSE}$	Minimum reset pulse width.	5.00	5.00	5.00	ns
MMCM_F_{PFDMAX}	Maximum frequency at the phase frequency detector.	500.00	450.00	450.00	MHz
MMCM_F_{PFDMIN}	Minimum frequency at the phase frequency detector.	10.00	10.00	10.00	MHz
MMCM_$T_{FBDELAY}$	Maximum delay in the feedback path.	3 ns Max or one CLKIN cycle			
MMCM Switching Characteristics Setup and Hold					
$T_{MMCMDCK\_PSEN}$/ $T_{MMCMCKD\_PSEN}$	Setup and hold of phase-shift enable.	1.04/0.00	1.04/0.00	1.04/0.00	ns

Table 37: **MMCM Specification *(Cont'd)***

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
$T_{MMCMDCK\_PSINCDEC}$/ $T_{MMCMCKD\_PSINCDEC}$	Setup and hold of phase-shift increment/decrement.	1.04/0.00	1.04/0.00	1.04/0.00	ns
$T_{MMCMCKO\_PSDONE}$	Phase shift clock-to-out of PSDONE.	0.68	0.81	0.81	ns
Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK					
$T_{MMCMDCK\_DADDR}$/ $T_{MMCMCKD\_DADDR}$	DADDR setup/hold.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
$T_{MMCMDCK\_DI}$/ $T_{MMCMCKD\_DI}$	DI setup/hold.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
$T_{MMCMDCK\_DEN}$/ $T_{MMCMCKD\_DEN}$	DEN setup/hold.	1.97/0.00	2.29/0.00	2.29/0.00	ns, Min
$T_{MMCMDCK\_DWE}$/ $T_{MMCMCKD\_DWE}$	DWE setup/hold.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
$T_{MMCMCKO\_DRDY}$	CLK to out of DRDY.	0.72	0.99	0.99	ns, Max
F_{DCK}	DCLK frequency.	200.00	200.00	200.00	MHz, Max

Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the *Clocking Wizard* [Ref 8].
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.
6. When CLKOUT4_CASCADE = TRUE, MMCM_F_{OUTMIN} is 0.036 MHz.

PLL Switching Characteristics

Table 38: **PLL Specification**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
PLL_F_{INMAX}	Maximum input clock frequency.	800.00	800.00	800.00	MHz
PLL_F_{INMIN}	Minimum input clock frequency.	19.00	19.00	19.00	MHz
PLL_$F_{INJITTER}$	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max			
PLL_F_{INDUTY}	Allowable input duty cycle: 19—49 MHz.	25	25	25	%
	Allowable input duty cycle: 50—199 MHz.	30	30	30	%
	Allowable input duty cycle: 200—399 MHz.	35	35	35	%
	Allowable input duty cycle: 400—499 MHz.	40	40	40	%
	Allowable input duty cycle: >500 MHz.	45	45	45	%
PLL_F_{VCOMIN}	Minimum PLL VCO frequency.	800.00	800.00	800.00	MHz
PLL_F_{VCOMAX}	Maximum PLL VCO frequency.	1866.00	1600.00	1600.00	MHz

Table 40: **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Far Clock Region)[1]**

Symbol	Description	Device	V_{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM/PLL.						
$T_{ICKOFFAR}$	Clock-capable clock input and OUTFF at pins/banks farthest from the BUFGs *without* MMCM/PLL (far clock region).[2]	XC7S6	5.55	6.50	6.50	ns
		XC7S15	5.55	6.50	6.50	ns
		XC7S25	5.55	6.44	6.44	ns
		XC7S50	5.71	6.62	6.62	ns
		XC7S75	6.01	7.02	7.02	ns
		XC7S100	6.01	7.02	7.02	ns
		XA7S6	5.55	6.50	N/A	ns
		XA7S15	5.55	6.50	N/A	ns
		XA7S25	5.55	6.44	N/A	ns
		XA7S50	5.71	6.62	N/A	ns
		XA7S75	6.01	7.02	N/A	ns
		XA7S100	6.01	7.02	N/A	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Refer to the *Die Level Bank Numbering Overview* section of the *7 Series FPGA Packaging and Pinout Specification* (UG475) [Ref 4].

Table 41: **Clock-Capable Clock Input to Output Delay With MMCM(1)**

Symbol	Description	Device	V_{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *with* MMCM.						
$T_{ICKOFMMCMCC}$	Clock-capable clock input and OUTFF *with* MMCM.(2)	XC7S6	1.03	1.03	1.03	ns
		XC7S15	1.03	1.03	1.03	ns
		XC7S25	1.00	1.00	1.00	ns
		XC7S50	1.00	1.00	1.00	ns
		XC7S75	1.00	1.00	1.00	ns
		XC7S100	1.00	1.00	1.00	ns
		XA7S6	1.03	1.03	N/A	ns
		XA7S15	1.03	1.03	N/A	ns
		XA7S25	1.00	1.00	N/A	ns
		XA7S50	1.00	1.00	N/A	ns
		XA7S75	1.00	1.00	N/A	ns
		XA7S100	1.00	1.00	N/A	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

Table 44: **Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks**

Symbol	Description	Device	V_{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1)						
T_{PSFD}/ T_{PHFD}	Full delay (legacy delay or default delay) global clock input and IFF(2) without MMCM/PLL with ZHOLD_DELAY on HR I/O banks.	XC7S6	2.76/–0.40	3.17/–0.40	3.17/–0.40	ns
		XC7S15	2.76/–0.40	3.17/–0.40	3.17/–0.40	ns
		XC7S25	2.67/–0.37	3.12/–0.37	3.12/–0.37	ns
		XC7S50	2.66/–0.28	3.11/–0.28	3.11/–0.28	ns
		XC7S75	2.91/–0.33	3.36/–0.33	3.36/–0.33	ns
		XC7S100	2.91/–0.33	3.36/–0.33	3.36/–0.33	ns
		XA7S6	2.76/–0.40	3.17/–0.40	N/A	ns
		XA7S15	2.76/–0.40	3.17/–0.40	N/A	ns
		XA7S25	2.67/–0.37	3.12/–0.37	N/A	ns
		XA7S50	2.66/–0.28	3.11/–0.28	N/A	ns
		XA7S75	2.91/–0.33	3.36/–0.33	N/A	ns
		XA7S100	2.91/–0.33	3.36/–0.33	N/A	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch.

Table 46: **Clock-Capable Clock Input Setup and Hold With PLL**

Symbol	Description	Device	V_{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard.(1)(2)						
$T_{PSPLLCC}$/ $T_{PHPLLCC}$	No delay clock-capable clock input and IFF(3) with PLL.	XC7S6	3.07/–0.17	3.69/–0.17	3.69/–0.17	ns
		XC7S15	3.07/–0.17	3.69/–0.17	3.69/–0.17	ns
		XC7S25	3.04/–0.19	3.64/–0.19	3.64/–0.19	ns
		XC7S50	3.15/–0.19	3.77/–0.19	3.77/–0.19	ns
		XC7S75	3.15/–0.19	3.78/–0.19	3.78/–0.19	ns
		XC7S100	3.15/–0.19	3.78/–0.19	3.78/–0.19	ns
		XA7S6	3.07/–0.17	3.69/–0.17	N/A	ns
		XA7S15	3.07/–0.17	3.69/–0.17	N/A	ns
		XA7S25	3.04/–0.19	3.64/–0.19	N/A	ns
		XA7S50	3.15/–0.19	3.77/–0.19	N/A	ns
		XA7S75	3.15/–0.19	3.78/–0.19	N/A	ns
		XA7S100	3.15/–0.19	3.78/–0.19	N/A	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. Use IBIS to determine any duty-cycle distortion incurred using various standards.
3. IFF = Input flip-flop or latch.

Table 47: **Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Input Setup and Hold Time Relative to a Forwarded Clock Input Pin Using BUFIO for SSTL15 Standard.					
T_{PSCS}/T_{PHCS}	Setup and hold of I/O clock.	–0.38/1.46	–0.38/1.73	–0.38/1.76	ns

Table 48: **Sample Window**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
T_{SAMP}	Sampling error at receiver pins.(1)	0.64	0.70	0.70	ns
T_{SAMP_BUFIO}	Sampling error at receiver pins using BUFIO.(2)	0.40	0.46	0.46	ns

Notes:

1. This parameter indicates the total sampling error of the Spartan-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 MMCM jitter
   - MMCM accuracy (phase offset)
   - MMCM phase shift resolution

   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of the Spartan-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Additional Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for Spartan-7 FPGA clock transmitter and receiver data-valid windows.

Table 49: **Package Skew**[1]

Symbol	Description	Device	Package	Value	Units
$T_{PKGSKEW}$	Package skew.[2]	XC7S6	CPGA196	44	ps
			CSGA225	83	ps
			FTGB196	65	ps
		XC7S15	CPGA196	44	ps
			CSGA225	83	ps
			FTGB196	65	ps
		XC7S25	CSGA225	93	ps
			CSGA324	62	ps
			FTGB196	83	ps
		XC7S50	CSGA324	80	ps
			FGGA484	110	ps
			FTGB196	103	ps
		XC7S75	FGGA484	117	ps
			FGGA676	110	ps
		XC7S100	FGGA484	117	ps
			FGGA676	110	ps
		XA7S6	CPGA196	44	ps
			CSGA225	83	ps
			FTGB196	65	ps
		XA7S15	CPGA196	44	ps
			CSGA225	83	ps
			FTGB196	65	ps
		XA7S25	CSGA225	93	ps
			CSGA324	62	ps
			FTGB196	83	ps
		XA7S50	CSGA324	80	ps
			FGGA484	110	ps
			FTGB196	103	ps
		XA7S75	FGGA484	117	ps
			FGGA676	110	ps
		XC7S100	FGGA484	117	ps
			FGGA676	110	ps

Notes:

1. Package delay information is available for these device/package combinations. This information can be used to deskew the package.
2. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.

Configuration Switching Characteristics

Table 51: **Configuration Switching Characteristics**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Power-up Timing Characteristics					
T_{PL} (1)	Program latency.	5.00	5.00	5.00	ms, Max
T_{POR} (2)	Power-on reset (50 ms ramp rate time).	10/50	10/50	10/50	ms, Min/Max
	Power-on reset (1 ms ramp rate time).	10/35	10/35	10/35	ms, Min/Max
$T_{PROGRAM}$	Program pulse width.	250.00	250.00	250.00	ns, Min
CCLK Output (Master Mode)					
T_{ICCK}	Master CCLK output delay.	150.00	150.00	150.00	ns, Min
T_{MCCKL}	Master CCLK clock Low time duty cycle.	40/60	40/60	40/60	%, Min/Max
T_{MCCKH}	Master CCLK clock High time duty cycle.	40/60	40/60	40/60	%, Min/Max
F_{MCCK}	Master CCLK frequency.	100.00	100.00	100.00	MHz, Max
	Master CCLK frequency for AES encrypted x16. (2)	50.00	50.00	50.00	MHz, Max
F_{MCCK_START}	Master CCLK frequency at start of configuration.	3.00	3.00	3.00	MHz, Typ
$F_{MCCKTOL}$	Frequency tolerance, master mode with respect to nominal CCLK.	±50	±50	±50	%, Max
CCLK Input (Slave Modes)					
T_{SCCKL}	Slave CCLK clock minimum Low time.	2.50	2.50	2.50	ns, Min
T_{SCCKH}	Slave CCLK clock minimum High time.	2.50	2.50	2.50	ns, Min
F_{SCCK}	Slave CCLK frequency.	100.00	100.00	100.00	MHz, Max
EMCCLK Input (Master Mode)					
T_{EMCCKL}	External master CCLK Low time.	2.50	2.50	2.50	ns, Min
T_{EMCCKH}	External master CCLK High time.	2.50	2.50	2.50	ns, Min
F_{EMCCK}	External master CCLK frequency.	100.00	100.00	100.00	MHz, Max
Internal Configuration Access Port					
F_{ICAPCK}	Internal configuration access port (ICAPE2) clock frequency.	100.00	100.00	100.00	MHz, Max
Master/Slave Serial Mode Programming Switching					
T_{DCCK}/ T_{CCKD}	D_{IN} setup/hold.	4.00/0.00	4.00/0.00	4.00/0.00	ns, Min
T_{CCO}	D_{OUT} clock to out.	8.00	8.00	8.00	ns, Max
SelectMAP Mode Programming Switching					
T_{SMDCCK}/ T_{SMCCKD}	D[31:00] setup/hold.	4.00/0.00	4.00/0.00	4.00/0.00	ns, Min