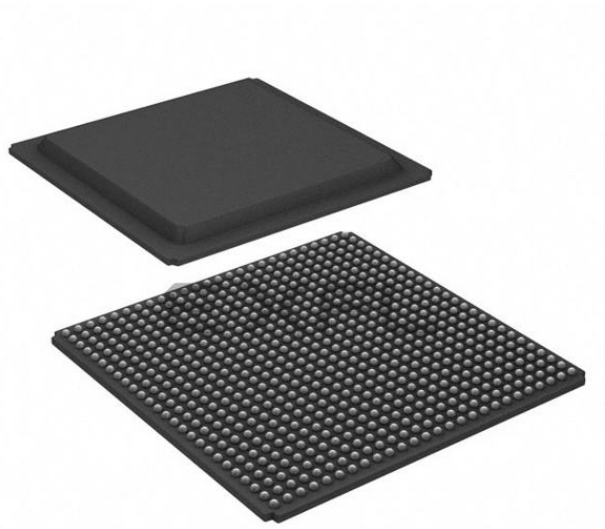
AMD Xilinx - XC7S75-1FGGA676C Datasheet



Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	6000
Number of Logic Elements/Cells	76800
Total RAM Bits	4331520
Number of I/O	400
Number of Gates	-
Voltage - Supply	0.95V ~ 1.05V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7s75-1fgga676c

Table 1: **Absolute Maximum Ratings(1) *(Cont'd)***

Symbol	Description	Min	Max	Units
V_{IN}(2)(3)(4)	I/O input voltage.	–0.4	V_{CCO} + 0.55	V
	I/O input voltage (when V_{CCO} = 3.3V) for V_{REF} and differential I/O standards except TMDS_33.(5)	–0.4	2.625	V
V_{CCBATT}	Key memory battery backup supply.	–0.5	2.0	V
XADC				
V_{CCADC}	XADC supply relative to GNDADC.	–0.5	2.0	V
V_{REFP}	XADC reference input relative to GNDADC.	–0.5	2.0	V
Temperature				
T_{STG}	Storage temperature (ambient).	–65	150	°C
T_{SOL}	Maximum soldering temperature for Pb/Sn component bodies.(6)	–	+220	°C
	Maximum soldering temperature for Pb-free component bodies.(6)	–	+260	°C
T_j	Maximum junction temperature.(6)	–	+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. The lower absolute voltage specification always applies.
3. For I/O operation, refer to the *7 Series FPGAs SelectIO Resources User Guide* (UG471) [Ref 3].
4. The maximum limit applies to DC signals. For maximum undershoot and overshoot AC specifications, see Table 4.
5. See Table 9 for TMDS_33 specifications.
6. For soldering guidelines and thermal considerations, see the *7 Series FPGA Packaging and Pinout Specification* (UG475) [Ref 4].

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 8: **SelectIO DC Input and Output Levels**(1)(2)(3)

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
HSTL_I	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8.00	–8.00
HSTL_I_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8.00	–8.00
HSTL_II	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	16.00	–16.00
HSTL_II_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	16.00	–16.00
HSUL_12	–0.300	V_{REF} – 0.130	V_{REF} + 0.130	V_{CCO} + 0.300	20% V_{CCO}	80% V_{CCO}	0.10	–0.10
LVCMOS12	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 4	Note 4
LVCMOS15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	25% V_{CCO}	75% V_{CCO}	Note 5	Note 5
LVCMOS18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 6	Note 6
LVCMOS25	–0.300	0.7	1.700	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 5	Note 5
LVCMOS33	–0.300	0.8	2.000	3.450	0.400	V_{CCO} – 0.400	Note 5	Note 5
LVTTL	–0.300	0.8	2.000	3.450	0.400	2.400	Note 6	Note 6
MOBILE_DDR	–0.300	20% V_{CCO}	80% V_{CCO}	V_{CCO} + 0.300	10% V_{CCO}	90% V_{CCO}	0.10	–0.10
PCI33_3	–0.400	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.500	10% V_{CCO}	90% V_{CCO}	1.50	–0.50
SSTL135	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	13.00	–13.00
SSTL135_R	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	8.90	–8.90
SSTL15	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.175	V_{CCO}/2 + 0.175	13.00	–13.00
SSTL15_R	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.175	V_{CCO}/2 + 0.175	8.90	–8.90
SSTL18_I	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 – 0.470	V_{CCO}/2 + 0.470	8.00	–8.00
SSTL18_II	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 – 0.600	V_{CCO}/2 + 0.600	13.40	–13.40

Notes:

1. Tested according to relevant specifications.
2. 3.3V and 2.5V standards are only supported in HR I/O banks.
3. For detailed interface specific DC voltage levels, see the *7 Series FPGAs SelectIO Resources User Guide* (UG471) [Ref 3].
4. Supported drive strengths of 4, 8, or 12 mA in HR I/O banks.
5. Supported drive strengths of 4, 8, 12, or 16 mA in HR I/O banks.
6. Supported drive strengths of 4, 8, 12, 16, or 24 mA in HR I/O banks.

Table 9: **Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM}[1]			V_{ID}[2]			V_{OCM}[3]			V_{OD}[4]		
	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max
BLVDS_25	0.300	1.200	1.425	0.100	–	–	–	1.250	–	Note 5		
MINI_LVDS_25	0.300	1.200	V_{CCAUX}	0.200	0.400	0.600	1.000	1.200	1.400	0.300	0.450	0.600
PPDS_25	0.200	0.900	V_{CCAUX}	0.100	0.250	0.400	0.500	0.950	1.400	0.100	0.250	0.400
RSDS_25	0.300	0.900	1.500	0.100	0.350	0.600	1.000	1.200	1.400	0.100	0.350	0.600
TMDS_33	2.700	2.965	3.230	0.150	0.675	1.200	V_{CCO} – 0.405	V_{CCO} – 0.300	V_{CCO} – 0.190	0.400	0.600	0.800

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q – $\overline{Q}$).
3. V_{OCM} is the output common mode voltage.
4. V_{OD} is the output differential voltage (Q – $\overline{Q}$).
5. V_{OD} for BLVDS will vary significantly depending on topology and loading.

Table 10: **Complementary Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM}[1]			V_{ID}[2]		V_{OL}[3]	V_{OH}[4]	I_{OL}	I_{OH}
	V, Min	V, Typ	V, Max	V, Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
DIFF_HSTL_I	0.300	0.750	1.125	0.100	–	0.400	V_{CCO} – 0.400	8.00	–8.00
DIFF_HSTL_I_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO} – 0.400	8.00	–8.00
DIFF_HSTL_II	0.300	0.750	1.125	0.100	–	0.400	V_{CCO} – 0.400	16.00	–16.00
DIFF_HSTL_II_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO} – 0.400	16.00	–16.00
DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% V_{CCO}	80% V_{CCO}	0.100	–0.100
DIFF_MOBILE_DDR	0.300	0.900	1.425	0.100	–	10% V_{CCO}	90% V_{CCO}	0.100	–0.100
DIFF_SSTL135	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	13.0	–13.0
DIFF_SSTL135_R	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	8.9	–8.9
DIFF_SSTL15	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	13.0	–13.0
DIFF_SSTL15_R	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	8.9	–8.9
DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.470	(V_{CCO}/2) + 0.470	8.00	–8.00
DIFF_SSTL18_II	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.600	(V_{CCO}/2) + 0.600	13.4	–13.4

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q – $\overline{Q}$).
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications from the Vivado® Design Suite as outlined in Table 12.

Table 12: **Speed Specification Version By Device**

2018.2.1	Device
1.23	XC7S6, XC7S15, XC7S25, XC7S50, XC7S75, XC7S100
1.16	XA7S6, XA7S15, XA7S25, XA7S50, XA7S75, XA7S100

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows.

Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Spartan-7 FPGAs.

Table 17: **IOB High Range (HR) Switching Characteristics**

I/O Standard	T_{IOPI}			T_{IOOP}			T_{IOTP}			Units
	V_{CCINT} Operating Voltage and Speed Grade									
	1.0V		0.95V	1.0V		0.95V	1.0V		0.95V	
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
LVTTL_S4	1.34	1.41	1.41	3.93	4.18	4.18	3.96	4.20	4.20	ns
LVTTL_S8	1.34	1.41	1.41	3.66	3.92	3.92	3.69	3.93	3.93	ns
LVTTL_S12	1.34	1.41	1.41	3.65	3.90	3.90	3.68	3.91	3.91	ns
LVTTL_S16	1.34	1.41	1.41	3.19	3.45	3.45	3.22	3.46	3.46	ns
LVTTL_S24	1.34	1.41	1.41	3.41	3.67	3.67	3.44	3.68	3.68	ns
LVTTL_F4	1.34	1.41	1.41	3.38	3.64	3.64	3.41	3.65	3.65	ns
LVTTL_F8	1.34	1.41	1.41	2.87	3.12	3.12	2.90	3.13	3.13	ns
LVTTL_F12	1.34	1.41	1.41	2.85	3.10	3.10	2.88	3.12	3.12	ns
LVTTL_F16	1.34	1.41	1.41	2.68	2.93	2.93	2.71	2.95	2.95	ns
LVTTL_F24	1.34	1.41	1.41	2.65	2.90	2.90	2.68	2.91	2.91	ns
LVDS_25	0.81	0.88	0.88	1.41	1.67	1.67	1.44	1.68	1.68	ns
MINI_LVDS_25	0.81	0.88	0.88	1.40	1.65	1.65	1.43	1.66	1.66	ns
BLVDS_25	0.81	0.88	0.88	1.96	2.21	2.21	1.99	2.23	2.23	ns
RSDS_25 (point to point)	0.81	0.88	0.88	1.40	1.65	1.65	1.43	1.66	1.66	ns
PPDS_25	0.81	0.88	0.88	1.41	1.67	1.67	1.44	1.68	1.68	ns
TMDS_33	0.81	0.88	0.88	1.54	1.79	1.79	1.57	1.80	1.80	ns
PCI33_3	1.32	1.39	1.39	3.22	3.48	3.48	3.25	3.49	3.49	ns
HSUL_12_S	0.75	0.82	0.82	1.93	2.18	2.18	1.96	2.20	2.20	ns
HSUL_12_F	0.75	0.82	0.82	1.41	1.67	1.67	1.44	1.68	1.68	ns
DIFF_HSUL_12_S	0.76	0.83	0.83	1.93	2.18	2.18	1.96	2.20	2.20	ns
DIFF_HSUL_12_F	0.76	0.83	0.83	1.41	1.67	1.67	1.44	1.68	1.68	ns
MOBILE_DDR_S	0.84	0.91	0.91	1.80	2.06	2.06	1.83	2.07	2.07	ns
MOBILE_DDR_F	0.84	0.91	0.91	1.51	1.76	1.76	1.54	1.77	1.77	ns
DIFF_MOBILE_DDR_S	0.78	0.85	0.85	1.82	2.07	2.07	1.85	2.09	2.09	ns
DIFF_MOBILE_DDR_F	0.78	0.85	0.85	1.57	1.82	1.82	1.60	1.84	1.84	ns
HSTL_I_S	0.75	0.82	0.82	1.74	1.99	1.99	1.77	2.01	2.01	ns
HSTL_II_S	0.73	0.80	0.80	1.54	1.79	1.79	1.57	1.80	1.80	ns
HSTL_I_18_S	0.75	0.82	0.82	1.41	1.67	1.67	1.44	1.68	1.68	ns
HSTL_II_18_S	0.75	0.81	0.81	1.54	1.79	1.79	1.57	1.80	1.80	ns
DIFF_HSTL_I_S	0.76	0.83	0.83	1.71	1.96	1.96	1.74	1.98	1.98	ns
DIFF_HSTL_II_S	0.76	0.83	0.83	1.63	1.88	1.88	1.66	1.90	1.90	ns
DIFF_HSTL_I_18_S	0.79	0.86	0.86	1.51	1.76	1.76	1.54	1.77	1.77	ns
DIFF_HSTL_II_18_S	0.78	0.85	0.85	1.58	1.84	1.84	1.61	1.85	1.85	ns
HSTL_I_F	0.75	0.82	0.82	1.22	1.48	1.48	1.25	1.49	1.49	ns
HSTL_II_F	0.73	0.80	0.80	1.24	1.49	1.49	1.27	1.51	1.51	ns
HSTL_I_18_F	0.75	0.82	0.82	1.26	1.51	1.51	1.29	1.52	1.52	ns

Table 17: **IOB High Range (HR) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}			T_{IOOP}			T_{IOTP}			Units
	V_{CCINT} Operating Voltage and Speed Grade									
	1.0V		0.95V	1.0V		0.95V	1.0V		0.95V	
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
HSTL_II_18_F	0.75	0.81	0.81	1.24	1.49	1.49	1.27	1.51	1.51	ns
DIFF_HSTL_I_F	0.76	0.83	0.83	1.30	1.56	1.56	1.33	1.57	1.57	ns
DIFF_HSTL_II_F	0.76	0.83	0.83	1.33	1.59	1.59	1.36	1.60	1.60	ns
DIFF_HSTL_I_18_F	0.79	0.86	0.86	1.33	1.59	1.59	1.36	1.60	1.60	ns
DIFF_HSTL_II_18_F	0.78	0.85	0.85	1.33	1.59	1.59	1.36	1.60	1.60	ns
LVCMOS33_S4	1.34	1.41	1.41	3.93	4.18	4.18	3.96	4.20	4.20	ns
LVCMOS33_S8	1.34	1.41	1.41	3.65	3.90	3.90	3.68	3.91	3.91	ns
LVCMOS33_S12	1.34	1.41	1.41	3.21	3.46	3.46	3.24	3.48	3.48	ns
LVCMOS33_S16	1.34	1.41	1.41	3.52	3.77	3.77	3.55	3.79	3.79	ns
LVCMOS33_F4	1.34	1.41	1.41	3.38	3.64	3.64	3.41	3.65	3.65	ns
LVCMOS33_F8	1.34	1.41	1.41	2.87	3.12	3.12	2.90	3.13	3.13	ns
LVCMOS33_F12	1.34	1.41	1.41	2.68	2.93	2.93	2.71	2.95	2.95	ns
LVCMOS33_F16	1.34	1.41	1.41	2.68	2.93	2.93	2.71	2.95	2.95	ns
LVCMOS25_S4	1.20	1.27	1.27	3.26	3.51	3.51	3.29	3.52	3.52	ns
LVCMOS25_S8	1.20	1.27	1.27	3.01	3.26	3.26	3.04	3.27	3.27	ns
LVCMOS25_S12	1.20	1.27	1.27	2.60	2.85	2.85	2.63	2.87	2.87	ns
LVCMOS25_S16	1.20	1.27	1.27	2.94	3.20	3.20	2.97	3.21	3.21	ns
LVCMOS25_F4	1.20	1.27	1.27	2.87	3.12	3.12	2.90	3.13	3.13	ns
LVCMOS25_F8	1.20	1.27	1.27	2.30	2.56	2.56	2.33	2.57	2.57	ns
LVCMOS25_F12	1.20	1.27	1.27	2.29	2.54	2.54	2.32	2.55	2.55	ns
LVCMOS25_F16	1.20	1.27	1.27	2.13	2.39	2.39	2.16	2.40	2.40	ns
LVCMOS18_S4	0.83	0.89	0.89	1.74	1.99	1.99	1.77	2.01	2.01	ns
LVCMOS18_S8	0.83	0.89	0.89	2.30	2.56	2.56	2.33	2.57	2.57	ns
LVCMOS18_S12	0.83	0.89	0.89	2.30	2.56	2.56	2.33	2.57	2.57	ns
LVCMOS18_S16	0.83	0.89	0.89	1.65	1.90	1.90	1.68	1.91	1.91	ns
LVCMOS18_S24	0.83	0.89	0.89	1.72	1.98	1.98	1.75	1.99	1.99	ns
LVCMOS18_F4	0.83	0.89	0.89	1.57	1.82	1.82	1.60	1.84	1.84	ns
LVCMOS18_F8	0.83	0.89	0.89	1.80	2.06	2.06	1.83	2.07	2.07	ns
LVCMOS18_F12	0.83	0.89	0.89	1.80	2.06	2.06	1.83	2.07	2.07	ns
LVCMOS18_F16	0.83	0.89	0.89	1.52	1.77	1.77	1.55	1.79	1.79	ns
LVCMOS18_F24	0.83	0.89	0.89	1.46	1.71	1.71	1.49	1.73	1.73	ns
LVCMOS15_S4	0.86	0.93	0.93	2.18	2.43	2.43	2.21	2.45	2.45	ns
LVCMOS15_S8	0.86	0.93	0.93	2.21	2.46	2.46	2.24	2.48	2.48	ns
LVCMOS15_S12	0.86	0.93	0.93	1.71	1.96	1.96	1.74	1.98	1.98	ns
LVCMOS15_S16	0.86	0.93	0.93	1.71	1.96	1.96	1.74	1.98	1.98	ns
LVCMOS15_F4	0.86	0.93	0.93	1.97	2.23	2.23	2.00	2.24	2.24	ns

Table 19: **Input Delay Measurement Methodology *(Cont'd)***

Description	I/O Standard Attribute	V_L[(1)]	V_H[(1)]	V_{MEAS}[(3)(5)]	V_{REF}[(2)(4)]
PPDS_25	PPDS_25	1.25 – 0.125	1.25 + 0.125	0[(5)]	–
RSDS_25	RSDS_25	1.25 – 0.125	1.25 + 0.125	0[(5)]	–
TMDS_33	TMDS_33	3 – 0.125	3 + 0.125	0[(5)]	–

Notes:

1. Input waveform switches between V_L and V_H.
2. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
3. Input voltage level from which measurement starts.
4. This is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 1.
5. The value given is the differential input voltage.

Table 20: **Output Delay Measurement Methodology**

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
LVCMOS, 1.2V	LVCMOS12	1M	0	0.6	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 3.3V	LVCMOS33	1M	0	1.65	0
LVTTL, 3.3V	LVTTL	1M	0	1.65	0
PCI33, 3.3V	PCI33_3	25	10	1.65	0
HSTL (high-speed transceiver logic), Class I, 1.2V	HSTL_I_12	50	0	V_{REF}	0.6
HSTL, Class I, 1.5V	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II, 1.5V	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	50	0	V_{REF}	0.6
SSTL12, 1.2V	SSTL12	50	0	V_{REF}	0.6
SSTL135/SSTL135_R, 1.35V	SSTL135, SSTL135_R	50	0	V_{REF}	0.675
SSTL15/SSTL15_R, 1.5V	SSTL15, SSTL15_R	50	0	V_{REF}	0.75
SSTL (stub-series terminated logic), Class I & Class II, 1.8V	SSTL18_I, SSTL18_II	50	0	V_{REF}	0.9
DIFF_MOBILE_DDR, 1.8V	DIFF_MOBILE_DDR	50	0	V_{REF}	0.9
DIFF_HSTL, Class I, 1.2V	DIFF_HSTL_I_12	50	0	V_{REF}	0.6
DIFF_HSTL, Class I & II, 1.5V	DIFF_HSTL_I, DIFF_HSTL_II	50	0	V_{REF}	0.75
DIFF_HSTL, Class I & II, 1.8V	DIFF_HSTL_I_18, DIFF_HSTL_II_18	50	0	V_{REF}	0.9
DIFF_HSUL_12, 1.2V	DIFF_HSUL_12	50	0	V_{REF}	0.6
DIFF_SSTL135/DIFF_SSTL135_R, 1.35V	DIFF_SSTL135, DIFF_SSTL135_R	50	0	V_{REF}	0.675
DIFF_SSTL15/DIFF_SSTL15_R, 1.5V	DIFF_SSTL15, DIFF_SSTL15_R	50	0	V_{REF}	0.75
DIFF_SSTL18, Class I & II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	50	0	V_{REF}	0.9
LVDS, 2.5V	LVDS_25	100	0	0[2]	0
BLVDS (Bus LVDS), 2.5V	BLVDS_25	100	0	0[2]	0
Mini LVDS, 2.5V	MINI_LVDS_25	100	0	0[2]	0
PPDS_25	PPDS_25	100	0	0[2]	0
RSDS_25	RSDS_25	100	0	0[2]	0
TMDS_33	TMDS_33	50	0	0[2]	3.3

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Input/Output Logic Switching Characteristics

Table 21: **ILOGIC Switching Characteristics**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Setup/Hold					
T_{ICE1CK}/T_{ICKCE1}	CE1 pin setup/hold with respect to CLK.	0.54/0.02	0.76/0.02	0.76/0.02	ns
T_{ISRCK}/T_{ICKSR}	SR pin setup/hold with respect to CLK.	0.70/0.01	1.13/0.01	1.13/0.01	ns
T_{IDOCK}/T_{IOCKD}	D pin setup/hold with respect to CLK without delay.	0.01/0.29	0.01/0.33	0.01/0.33	ns
T_{IDOCKD}/T_{IOCKDD}	DDLY pin setup/hold with respect to CLK (using IDELAY).	0.02/0.29	0.02/0.33	0.02/0.33	ns
Combinatorial					
T_{IDI}	D pin to O pin propagation delay, no delay.	0.11	0.13	0.13	ns
T_{IDID}	DDLY pin to O pin propagation delay (using IDELAY).	0.12	0.14	0.14	ns
Sequential Delays					
T_{IDLO}	D pin to Q1 pin using flip-flop as a latch without delay.	0.44	0.51	0.51	ns
T_{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY).	0.44	0.51	0.51	ns
T_{ICKQ}	CLK to Q outputs.	0.57	0.66	0.66	ns
T_{RQ_ILOGIC}	SR pin to OQ/TQ out.	1.08	1.32	1.32	ns
T_{GSRQ_ILOGIC}	Global set/reset to Q outputs.	7.60	10.51	10.51	ns
Set/Reset					
T_{RPW_ILOGIC}	Minimum pulse width, SR inputs.	0.72	0.72	0.72	ns, Min

Output Serializer/Deserializer Switching Characteristics

Table 24: **OSERDES Switching Characteristics**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Setup/Hold					
T_{OSDCK_D}/ T_{OSCKD_D}	D input setup/hold with respect to CLKDIV.	0.45/0.03	0.63/0.03	0.63/0.03	ns
T_{OSDCK_T}/ T_{OSCKD_T}	T input setup/hold with respect to CLK.	0.73/–0.13	0.88/–0.13	0.88/–0.13	ns
T_{OSDCK_T2}/ T_{OSCKD_T2}	T input setup/hold with respect to CLKDIV.	0.34/–0.13	0.39/–0.13	0.39/–0.13	ns
T_{OSCCK_OCE}/ T_{OSCKC_OCE}	OCE input setup/hold with respect to CLK.	0.34/0.58	0.51/0.58	0.51/0.58	ns
T_{OSCCK_S}	SR (reset) input setup with respect to CLKDIV.	0.52	0.85	0.85	ns
T_{OSCCK_TCE}/ T_{OSCKC_TCE}	TCE input setup/hold with respect to CLK.	0.34/0.01	0.51/0.01	0.51/0.01	ns
Sequential Delays					
T_{OSCKO_OQ}	Clock to out from CLK to OQ.	0.42	0.48	0.48	ns
T_{OSCKO_TQ}	Clock to out from CLK to TQ.	0.49	0.56	0.56	ns
Combinatorial					
T_{OSDO_TTQ}	T input to TQ out.	0.92	1.11	1.11	ns

Input/Output Delay Switching Characteristics

Table 25: **Input/Output Delay Switching Characteristics**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
IDELAYCTRL					
T_{DLYCCO_RDY}	Reset to ready for IDELAYCTRL.	3.67	3.67	3.67	µs
$F_{IDELAYCTRL\_REF}$	Attribute REFCLK frequency = 200.00.(1)	200.00	200.00	200.00	MHz
	Attribute REFCLK frequency = 300.00.(1)	300.00	300.00	300.00	MHz
	Attribute REFCLK frequency = 400.00.(1)	400.00	N/A	N/A	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	±10	MHz
$T_{IDELAYCTRL\_RPW}$	Minimum reset pulse width.	59.28	59.28	59.28	ns
IDELAY					
$T_{IDELAYRESOLUTION}$	IDELAY chain delay resolution.	1/(32 x 2 x F_{REF})			µs
$T_{IDELAYPAT\_JIT}$	Pattern dependent period jitter in delay chain for clock pattern.(2)	0	0	0	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23).(3)	±5	±5	±5	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23).(4)	±9	±9	±9	ps per tap
$T_{IDELAY\_CLK\_MAX}$	Maximum frequency of CLK input to IDELAY.	680.00	600.00	600.00	MHz
T_{IDCCK_CE} / T_{IDCKC_CE}	CE pin setup/hold with respect to C for IDELAY.	0.16/0.13	0.21/0.16	0.21/0.16	ns
T_{IDCCK_INC}/ T_{IDCKC_INC}	INC pin setup/hold with respect to C for IDELAY.	0.14/0.18	0.16/0.22	0.16/0.22	ns
T_{IDCCK_RST}/ T_{IDCKC_RST}	RST pin setup/hold with respect to C for IDELAY.	0.16/0.11	0.18/0.14	0.18/0.14	ns
$T_{IDDO\_IDATAIN}$	Propagation delay through IDELAY.	Note 5	Note 5	Note 5	ps

Notes:

1. Average tap delay at 200 MHz = 78 ps, at 300 MHz = 52 ps, and at 400 MHz = 39 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE.
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY tap setting. See the timing report for actual values.

CLB Switching Characteristics

Table 27: **CLB Switching Characteristics**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Combinatorial Delays					
T_{ILO}	An – Dn LUT address to A.	0.11	0.13	0.13	ns, Max
T_{ILO_2}	An – Dn LUT address to AMUX/CMUX.	0.30	0.36	0.36	ns, Max
T_{ILO_3}	An – Dn LUT address to BMUX_A.	0.46	0.55	0.55	ns, Max
T_{ITO}	An – Dn inputs to A – D Q outputs.	1.05	1.27	1.27	ns, Max
T_{AXA}	AX inputs to AMUX output.	0.69	0.84	0.84	ns, Max
T_{AXB}	AX inputs to BMUX output.	0.66	0.83	0.83	ns, Max
T_{AXC}	AX inputs to CMUX output.	0.68	0.82	0.82	ns, Max
T_{AXD}	AX inputs to DMUX output.	0.75	0.90	0.90	ns, Max
T_{BXB}	BX inputs to BMUX output.	0.57	0.69	0.69	ns, Max
T_{BXD}	BX inputs to DMUX output.	0.69	0.82	0.82	ns, Max
T_{CXC}	CX inputs to CMUX output.	0.48	0.58	0.58	ns, Max
T_{CXD}	CX inputs to DMUX output.	0.59	0.71	0.71	ns, Max
T_{DXD}	DX inputs to DMUX output.	0.58	0.70	0.70	ns, Max
Sequential Delays					
T_{CKO}	Clock to AQ – DQ outputs.	0.44	0.53	0.53	ns, Max
T_{SHCKO}	Clock to AMUX – DMUX outputs.	0.53	0.66	0.66	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK					
T_{AS}/T_{AH}	AN – DN input to CLK on A – D flip-flops.	0.09/0.14	0.11/0.18	0.11/0.18	ns, Min
T_{DICK}/T_{CKDI}	AX – DX input to CLK on A – D flip-flops.	0.07/0.21	0.09/0.26	0.09/0.26	ns, Min
	AX – DX input through MUXs and/or carry logic to CLK on A – D flip-flops.	0.66/0.09	0.81/0.11	0.81/0.11	ns, Min
$T_{CECK\_CLB}/T_{CKCE\_CLB}$	CE input to CLK on A – D flip-flops.	0.17/0.00	0.21/0.01	0.21/0.01	ns, Min
T_{SRCK}/T_{CKSR}	SR input to CLK on A – D flip-flops.	0.43/0.04	0.53/0.05	0.53/0.05	ns, Min
Set/Reset					
T_{SRMIN}	SR input minimum pulse width.	0.78	1.04	1.04	ns, Min
T_{RQ}	Delay from SR input to AQ – DQ flip-flops.	0.59	0.71	0.71	ns, Max
T_{CEO}	Delay from CE input to AQ – DQ flip-flops.	0.58	0.70	0.70	ns, Max
F_{TOG}	Toggle frequency (for export control).	1286	1098	1098	MHz

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 28: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Sequential Delays					
T_{SHCKO}	Clock to A – B outputs.	1.09	1.32	1.32	ns, Max
T_{SHCKO_1}	Clock to AMUX – BMUX outputs.	1.53	1.86	1.86	ns, Max
Setup and Hold Times Before/After Clock CLK					
T_{DS_LRAM}/T_{DH_LRAM}	A – D inputs to CLK.	0.60/0.30	0.72/0.35	0.72/0.35	ns, Min
T_{AS_LRAM}/T_{AH_LRAM}	Address An inputs to clock.	0.30/0.60	0.37/0.70	0.37/0.70	ns, Min
	Address An inputs through MUXs and/or carry logic to clock.	0.77/0.21	0.94/0.26	0.94/0.26	ns, Min
T_{WS_LRAM}/T_{WH_LRAM}	WE input to clock.	0.43/0.12	0.53/0.17	0.53/0.17	ns, Min
$T_{CECK\_LRAM}/T_{CKCE\_LRAM}$	CE input to CLK.	0.44/0.11	0.53/0.17	0.53/0.17	ns, Min
Clock CLK					
T_{MPW_LRAM}	Minimum pulse width.	1.13	1.25	1.25	ns, Min
T_{MCP}	Minimum clock period.	2.26	2.50	2.50	ns, Min

Notes:

1. T_{SHCKO} also represents the CLK to XMUX output. Refer to the timing report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 29: **CLB Shift Register Switching Characteristics**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Sequential Delays					
T_{REG}	Clock to A – D outputs.	1.33	1.61	1.61	ns, Max
T_{REG_MUX}	Clock to AMUX – DMUX output.	1.77	2.15	2.15	ns, Max
T_{REG_M31}	Clock to DMUX output via M31 output.	1.23	1.46	1.46	ns, Max
Setup and Hold Times Before/After Clock CLK					
$T_{WS\_SHFREG}/ T_{WH\_SHFREG}$	WE input.	0.41/0.12	0.51/0.17	0.51/0.17	ns, Min
$T_{CECK\_SHFREG}/ T_{CKCE\_SHFREG}$	CE input to CLK.	0.42/0.11	0.52/0.17	0.52/0.17	ns, Min
$T_{DS\_SHFREG}/ T_{DH\_SHFREG}$	A – D inputs to CLK.	0.37/0.37	0.44/0.43	0.44/0.43	ns, Min
Clock CLK					
T_{MPW_SHFREG}	Minimum pulse width.	0.86	0.98	0.98	ns, Min

Block RAM and FIFO Switching Characteristics

Table 30: **Block RAM and FIFO Switching Characteristics**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Block RAM and FIFO Clock-to-Out Delays					
T_{RCKO_DO} and $T_{RCKO\_DO\_REG}$	Clock CLK to DOUT output (without output register).(1)(2)	2.13	2.46	2.46	ns, Max
	Clock CLK to DOUT output (with output register).(3)(4)	0.74	0.89	0.89	ns, Max
$T_{RCKO\_DO\_ECC}$ and $T_{RCKO\_DO\_ECC\_REG}$	Clock CLK to DOUT output with ECC (without output register).(1)(2)	3.04	3.84	3.84	ns, Max
	Clock CLK to DOUT output with ECC (with output register).(3)(4)	0.81	0.94	0.94	ns, Max
$T_{RCKO\_DO\_CASCOUT}$ and $T_{RCKO\_DO\_CASCOUT\_REG}$	Clock CLK to DOUT output with cascade (without output register).(1)	2.88	3.30	3.30	ns, Max
	Clock CLK to DOUT output with cascade (with output register).(3)	1.28	1.46	1.46	ns, Max
T_{RCKO_FLAGS}	Clock CLK to FIFO flags outputs.(5)	0.87	1.05	1.05	ns, Max
$T_{RCKO\_POINTERS}$	Clock CLK to FIFO pointers outputs.(6)	1.02	1.15	1.15	ns, Max
$T_{RCKO\_PARITY\_ECC}$	Clock CLK to ECCPARITY in ECC encode only mode.	0.85	0.94	0.94	ns, Max
$T_{RCKO\_SDBIT\_ECC}$ and $T_{RCKO\_SDBIT\_ECC\_REG}$	Clock CLK to BITERR (without output register).	2.81	3.55	3.55	ns, Max
	Clock CLK to BITERR (with output register).	0.76	0.89	0.89	ns, Max
$T_{RCKO\_RDADDR\_ECC}$ and $T_{RCKO\_RDADDR\_ECC\_REG}$	Clock CLK to RDADDR output with ECC (without output register).	0.88	1.07	1.07	ns, Max
	Clock CLK to RDADDR output with ECC (with output register).	0.93	1.08	1.08	ns, Max
Setup and Hold Times Before/After Clock CLK					
T_{RCCK_ADDRA}/ T_{RCKC_ADDRA}	ADDR inputs.(7)	0.49/0.33	0.57/0.36	0.57/0.36	ns, Min
$T_{RDCK\_DI\_WF\_NC}$/ $T_{RCKD\_DI\_WF\_NC}$	Data input setup/hold time when block RAM is configured in WRITE_FIRST or NO_CHANGE mode.(8)	0.65/0.63	0.74/0.67	0.74/0.67	ns, Min
$T_{RDCK\_DI\_RF}$/ $T_{RCKD\_DI\_RF}$	Data input setup/hold time when block RAM is configured in READ_FIRST mode.(8)	0.22/0.34	0.25/0.41	0.25/0.41	ns, Min
$T_{RDCK\_DI\_ECC}$/ $T_{RCKD\_DI\_ECC}$	DIN inputs with block RAM ECC in standard mode.(8)	0.55/0.46	0.63/0.50	0.63/0.50	ns, Min
$T_{RDCK\_DI\_ECCW}$/ $T_{RCKD\_DI\_ECCW}$	DIN inputs with block RAM ECC encode only.(8)	1.02/0.46	1.17/0.50	1.17/0.50	ns, Min

MMCM Switching Characteristics

Table 37: **MMCM Specification**

Symbol	Description	V_{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
MMCM_F_{INMAX}	Maximum input clock frequency.	800.00	800.00	800.00	MHz
MMCM_F_{INMIN}	Minimum input clock frequency.	10.00	10.00	10.00	MHz
MMCM_$F_{INJITTER}$	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max			
MMCM_F_{INDUTY}	Allowable input duty cycle: 10—49 MHz.	25	25	25	%
	Allowable input duty cycle: 50—199 MHz.	30	30	30	%
	Allowable input duty cycle: 200—399 MHz.	35	35	35	%
	Allowable input duty cycle: 400—499 MHz.	40	40	40	%
	Allowable input duty cycle: > 500 MHz.	45	45	45	%
MMCM_F_{MIN_PSCLK}	Minimum dynamic phase-shift clock frequency.	0.01	0.01	0.01	MHz
MMCM_F_{MAX_PSCLK}	Maximum dynamic phase-shift clock frequency.	500.00	450.00	450.00	MHz
MMCM_F_{VCOMIN}	Minimum MMCM VCO frequency.	600.00	600.00	600.00	MHz
MMCM_F_{VCOMAX}	Maximum MMCM VCO frequency.	1440.00	1200.00	1200.00	MHz
MMCM_$F_{BANDWIDTH}$	Low MMCM bandwidth at typical.(1)	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical.(1)	4.00	4.00	4.00	MHz
MMCM_$T_{STATPHAOFFSET}$	Static phase offset of the MMCM outputs.(2)	0.12	0.12	0.12	ns
MMCM_$T_{OUTJITTER}$	MMCM output jitter.	Note 3			
MMCM_$T_{OUTDUTY}$	MMCM output clock duty-cycle precision.(4)	0.20	0.20	0.20	ns
MMCM_$T_{LOCKMAX}$	MMCM maximum lock time.	100.00	100.00	100.00	µs
MMCM_F_{OUTMAX}	MMCM maximum output frequency.	800.00	800.00	800.00	MHz
MMCM_F_{OUTMIN}	MMCM minimum output frequency.(5)(6)	4.69	4.69	4.69	MHz
MMCM_$T_{EXTFDVAR}$	External clock feedback variation.	< 20% of clock input period or 1 ns Max			
MMCM_$RST_{MINPULSE}$	Minimum reset pulse width.	5.00	5.00	5.00	ns
MMCM_F_{PFDMAX}	Maximum frequency at the phase frequency detector.	500.00	450.00	450.00	MHz
MMCM_F_{PFDMIN}	Minimum frequency at the phase frequency detector.	10.00	10.00	10.00	MHz
MMCM_$T_{FBDELAY}$	Maximum delay in the feedback path.	3 ns Max or one CLKIN cycle			
MMCM Switching Characteristics Setup and Hold					
$T_{MMCMDCK\_PSEN}$/ $T_{MMCMCKD\_PSEN}$	Setup and hold of phase-shift enable.	1.04/0.00	1.04/0.00	1.04/0.00	ns

Device Pin-to-Pin Output Parameter Guidelines

Table 39: **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)[1]**

Symbol	Description	Device	V_{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM/PLL.						
T_{ICKOF}	Clock-capable clock input and OUTFF at pins/banks closest to the BUFGs *without* MMCM/PLL (near clock region).[2]	XC7S6	5.55	6.50	6.50	ns
		XC7S15	5.55	6.50	6.50	ns
		XC7S25	5.55	6.44	6.44	ns
		XC7S50	5.71	6.62	6.62	ns
		XC7S75	5.73	6.71	6.71	ns
		XC7S100	5.73	6.71	6.71	ns
		XA7S6	5.55	6.50	N/A	ns
		XA7S15	5.55	6.50	N/A	ns
		XA7S25	5.55	6.44	N/A	ns
		XA7S50	5.71	6.62	N/A	ns
		XA7S75	5.73	6.71	N/A	ns
		XA7S100	5.73	6.71	N/A	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Refer to the *Die Level Bank Numbering Overview* section of the *7 Series FPGA Packaging and Pinout Specification* (UG475) [Ref 4].

Table 41: **Clock-Capable Clock Input to Output Delay With MMCM(1)**

Symbol	Description	Device	V_{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *with* MMCM.						
$T_{ICKOFMMCMCC}$	Clock-capable clock input and OUTFF *with* MMCM.(2)	XC7S6	1.03	1.03	1.03	ns
		XC7S15	1.03	1.03	1.03	ns
		XC7S25	1.00	1.00	1.00	ns
		XC7S50	1.00	1.00	1.00	ns
		XC7S75	1.00	1.00	1.00	ns
		XC7S100	1.00	1.00	1.00	ns
		XA7S6	1.03	1.03	N/A	ns
		XA7S15	1.03	1.03	N/A	ns
		XA7S25	1.00	1.00	N/A	ns
		XA7S50	1.00	1.00	N/A	ns
		XA7S75	1.00	1.00	N/A	ns
		XA7S100	1.00	1.00	N/A	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

Table 44: **Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks**

Symbol	Description	Device	V_{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1)						
T_{PSFD}/ T_{PHFD}	Full delay (legacy delay or default delay) global clock input and IFF(2) without MMCM/PLL with ZHOLD_DELAY on HR I/O banks.	XC7S6	2.76/–0.40	3.17/–0.40	3.17/–0.40	ns
		XC7S15	2.76/–0.40	3.17/–0.40	3.17/–0.40	ns
		XC7S25	2.67/–0.37	3.12/–0.37	3.12/–0.37	ns
		XC7S50	2.66/–0.28	3.11/–0.28	3.11/–0.28	ns
		XC7S75	2.91/–0.33	3.36/–0.33	3.36/–0.33	ns
		XC7S100	2.91/–0.33	3.36/–0.33	3.36/–0.33	ns
		XA7S6	2.76/–0.40	3.17/–0.40	N/A	ns
		XA7S15	2.76/–0.40	3.17/–0.40	N/A	ns
		XA7S25	2.67/–0.37	3.12/–0.37	N/A	ns
		XA7S50	2.66/–0.28	3.11/–0.28	N/A	ns
		XA7S75	2.91/–0.33	3.36/–0.33	N/A	ns
		XA7S100	2.91/–0.33	3.36/–0.33	N/A	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch.

Additional Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for Spartan-7 FPGA clock transmitter and receiver data-valid windows.

Table 49: **Package Skew**[1]

Symbol	Description	Device	Package	Value	Units
$T_{PKGSKEW}$	Package skew.[2]	XC7S6	CPGA196	44	ps
			CSGA225	83	ps
			FTGB196	65	ps
		XC7S15	CPGA196	44	ps
			CSGA225	83	ps
			FTGB196	65	ps
		XC7S25	CSGA225	93	ps
			CSGA324	62	ps
			FTGB196	83	ps
		XC7S50	CSGA324	80	ps
			FGGA484	110	ps
			FTGB196	103	ps
		XC7S75	FGGA484	117	ps
			FGGA676	110	ps
		XC7S100	FGGA484	117	ps
			FGGA676	110	ps
		XA7S6	CPGA196	44	ps
			CSGA225	83	ps
			FTGB196	65	ps
		XA7S15	CPGA196	44	ps
			CSGA225	83	ps
			FTGB196	65	ps
		XA7S25	CSGA225	93	ps
			CSGA324	62	ps
			FTGB196	83	ps
		XA7S50	CSGA324	80	ps
			FGGA484	110	ps
			FTGB196	103	ps
		XA7S75	FGGA484	117	ps
			FGGA676	110	ps
		XC7S100	FGGA484	117	ps
			FGGA676	110	ps

Notes:

1. Package delay information is available for these device/package combinations. This information can be used to deskew the package.
2. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.

eFUSE Programming Conditions

Table 52 lists the programming conditions specifically for eFUSE. For more information, see the *7 Series FPGA Configuration User Guide* (UG470) [Ref 10].

Table 52: **eFUSE Programming Conditions(1)**

Symbol	Description	Min	Typ	Max	Units
I_{FS}	V_{CCAUX} supply current	–	–	115	mA
T_j	Temperature range	15	–	125	°C

Notes:

1. The FPGA must not be configured during eFUSE programming.

References

1. *7 Series FPGAs Overview* (DS180)
2. *XA Spartan-7 Automotive FPGA Data Sheet: Overview* (DS171)
3. *7 Series FPGAs SelectIO Resources User Guide* (UG471)
4. *7 Series FPGA Packaging and Pinout Specification* (UG475)
5. *7 Series FPGAs PCB Design Guide* (UG483)
6. *Xilinx Power Estimator* spreadsheet tool (XPE)
7. *Zynq-7000 AP SoC and 7 Series FPGAs Memory Interface Solutions User Guide* (UG586)
8. See the Clocking Wizard in Vivado software.
9. *7 Series FPGAs and Zynq-7000 AP SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480)
10. *7 Series FPGA Configuration User Guide* (UG470)