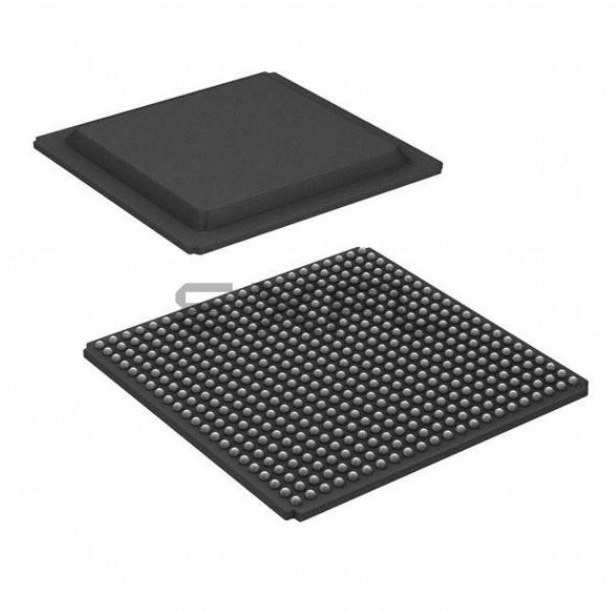
# AMD Xilinx - XC7S75-2FGGA484C Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 6000 |
| Number of Logic Elements/Cells | 76800 |
| Total RAM Bits | 4331520 |
| Number of I/O | 338 |
| Number of Gates | - |
| Voltage - Supply | 0.95V ~ 1.05V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 484-BGA |
| Supplier Device Package | 484-FPBGA (23x23) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc7s75-2fgga484c |

*Table 1:* **Absolute Maximum Ratings(1) *(Cont'd)***

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $V_{IN}$(2)(3)(4) | I/O input voltage. | –0.4 | $V_{CCO}$ + 0.55 | V |
| | I/O input voltage (when $V_{CCO}$ = 3.3V) for $V_{REF}$ and differential I/O standards except TMDS_33.(5) | –0.4 | 2.625 | V |
| $V_{CCBATT}$ | Key memory battery backup supply. | –0.5 | 2.0 | V |
| **XADC** | | | | |
| $V_{CCADC}$ | XADC supply relative to GNDADC. | –0.5 | 2.0 | V |
| $V_{REFP}$ | XADC reference input relative to GNDADC. | –0.5 | 2.0 | V |
| **Temperature** | | | | |
| $T_{STG}$ | Storage temperature (ambient). | –65 | 150 | °C |
| $T_{SOL}$ | Maximum soldering temperature for Pb/Sn component bodies.(6) | – | +220 | °C |
| | Maximum soldering temperature for Pb-free component bodies.(6) | – | +260 | °C |
| $T_j$ | Maximum junction temperature.(6) | – | +125 | °C |

**Notes:**

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. The lower absolute voltage specification always applies.
3. For I/O operation, refer to the *7 Series FPGAs SelectIO Resources User Guide* (UG471) [Ref 3].
4. The maximum limit applies to DC signals. For maximum undershoot and overshoot AC specifications, see Table 4.
5. See Table 9 for TMDS_33 specifications.
6. For soldering guidelines and thermal considerations, see the *7 Series FPGA Packaging and Pinout Specification* (UG475) [Ref 4].

*Table 2:* **Recommended Operating Conditions(1)(2)**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **FPGA Logic** | | | | | |
| $V_{CCINT}$(3) | For -2 and -1 (1.0V) devices: internal supply voltage. | 0.95 | 1.00 | 1.05 | V |
| | For -1L (0.95V) devices: internal supply voltage. | 0.92 | 0.95 | 0.98 | V |
| $V_{CCAUX}$ | Auxiliary supply voltage. | 1.71 | 1.80 | 1.89 | V |
| $V_{CCBRAM}$(3) | For -2 and -1 (1.0V) devices: block RAM supply voltage. | 0.95 | 1.00 | 1.05 | V |
| | For -1L (0.95V) devices: block RAM supply voltage. | 0.92 | 0.95 | 0.98 | V |
| $V_{CCO}$(4)(5) | Supply voltage for HR I/O banks. | 1.14 | – | 3.465 | V |
| $V_{IN}$(6) | I/O input voltage. | –0.20 | – | $V_{CCO}$ + 0.20 | V |
| | I/O input voltage (when $V_{CCO}$ = 3.3V) for $V_{REF}$ and differential I/O standards except TMDS_33.(7) | –0.20 | – | 2.625 | V |
| $I_{IN}$(8) | Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode. | – | – | 10 | mA |
| $V_{CCBATT}$(9) | Battery voltage. | 1.0 | – | 1.89 | V |
| **XADC** | | | | | |
| $V_{CCADC}$ | XADC supply relative to GNDADC. | 1.71 | 1.80 | 1.89 | V |
| $V_{REFP}$ | Externally supplied reference voltage. | 1.20 | 1.25 | 1.30 | V |
| **Temperature** | | | | | |
| $T_j$ | Junction temperature operating range for commercial (C) temperature devices. | 0 | – | 85 | °C |
| | Junction temperature operating range for industrial (I) temperature devices. | –40 | – | 100 | °C |
| | Junction temperature operating range for expanded (Q) temperature devices. | –40 | – | 125 | °C |

**Notes:**

1. All voltages are relative to ground.
2. For the design of the power distribution system consult the *7 Series FPGAs PCB Design Guide* (UG483) [Ref 5].
3. If $V_{CCINT}$ and $V_{CCBRAM}$ are operating at the same voltage, $V_{CCINT}$ and $V_{CCBRAM}$ should be connected to the same supply.
4. Configuration data is retained even if $V_{CCO}$ drops to 0V.
5. Includes $V_{CCO}$ of 1.2V, 1.35V, 1.5V, 1.8V, 2.5V, and 3.3V at ±5%.
6. The lower absolute voltage specification always applies.
7. See Table 9 for TMDS_33 specifications.
8. A total of 200 mA per bank should not be exceeded.
9. $V_{CCBATT}$ is required only when using bitstream encryption. If battery is not used, connect $V_{CCBATT}$ to either ground or $V_{CCAUX}$.

*Table 4:* **$V_{IN}$ Maximum Allowed AC Voltage Overshoot and Undershoot for HR I/O Banks(1)(2)**

| AC Voltage Overshoot | % of UI at –40°C to 125°C | AC Voltage Undershoot | % of UI at –40°C to 125°C |
|---|---|---|---|
| $V_{CCO}$ + 0.55 | 100 | –0.40 | 100 |
| | | –0.45 | 61.7 |
| | | –0.50 | 25.8 |
| | | –0.55 | 11.0 |
| $V_{CCO}$ + 0.60 | 46.6 | –0.60 | 4.77 |
| $V_{CCO}$ + 0.65 | 21.2 | –0.65 | 2.10 |
| $V_{CCO}$ + 0.70 | 9.75 | –0.70 | 0.94 |
| $V_{CCO}$ + 0.75 | 4.55 | –0.75 | 0.43 |
| $V_{CCO}$ + 0.80 | 2.15 | –0.80 | 0.20 |
| $V_{CCO}$ + 0.85 | 1.02 | –0.85 | 0.09 |
| $V_{CCO}$ + 0.90 | 0.49 | –0.90 | 0.04 |
| $V_{CCO}$ + 0.95 | 0.24 | –0.95 | 0.02 |

**Notes:**

1. A total of 200 mA per bank should not be exceeded.
2. The peak voltage of the overshoot or undershoot, and the duration above $V_{CCO}$ + 0.20V or below GND – 0.20V, must not exceed the values in this table.

*Table 5:* **Typical Quiescent Supply Current(1)(2)(3)**

| Symbol | Description | Device | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | | | 0.95V | |
| | | | -2C | -2I | -1C | -1I | -1Q | -1LI | |
| $I_{CCINTQ}$ | Quiescent $V_{CCINT}$ supply current. | XC7S6 | 36 | 36 | 36 | 36 | 36 | 32 | mA |
| | | XC7S15 | 36 | 36 | 36 | 36 | 36 | 32 | mA |
| | | XC7S25 | 48 | 48 | 48 | 48 | 48 | 43 | mA |
| | | XC7S50 | 95 | 95 | 95 | 95 | 95 | 59 | mA |
| | | XC7S75 | 148 | 148 | 148 | 148 | 148 | 134 | mA |
| | | XC7S100 | 148 | 148 | 148 | 148 | 148 | 134 | mA |
| | | XA7S6 | N/A | 36 | N/A | 36 | 36 | N/A | mA |
| | | XA7S15 | N/A | 36 | N/A | 36 | 36 | N/A | mA |
| | | XA7S25 | N/A | 48 | N/A | 48 | 48 | N/A | mA |
| | | XA7S50 | N/A | 95 | N/A | 95 | 95 | N/A | mA |
| | | XA7S75 | N/A | 148 | N/A | 148 | 148 | N/A | mA |
| | | XA7S100 | N/A | 148 | N/A | 148 | 148 | N/A | mA |

*Table 5:* **Typical Quiescent Supply Current[(1)(2)(3)] *(Cont'd)***

| Symbol | Description | Device | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | | | 0.95V | |
| | | | -2C | -2I | -1C | -1I | -1Q | -1LI | |
| $I_{CCBRAMQ}$ | Quiescent $V_{CCBRAM}$ supply current. | XC7S6 | 1 | 1 | 1 | 1 | 1 | 1 | mA |
| | | XC7S15 | 1 | 1 | 1 | 1 | 1 | 1 | mA |
| | | XC7S25 | 1 | 1 | 1 | 1 | 1 | 1 | mA |
| | | XC7S50 | 2 | 2 | 2 | 2 | 2 | 1 | mA |
| | | XC7S75 | 9 | 9 | 9 | 9 | 9 | 8 | mA |
| | | XC7S100 | 9 | 9 | 9 | 9 | 9 | 8 | mA |
| | | XA7S6 | N/A | 1 | N/A | 1 | 1 | N/A | mA |
| | | XA7S15 | N/A | 1 | N/A | 1 | 1 | N/A | mA |
| | | XA7S25 | N/A | 1 | N/A | 1 | 1 | N/A | mA |
| | | XA7S50 | N/A | 2 | N/A | 2 | 2 | N/A | mA |
| | | XA7S75 | N/A | 9 | N/A | 9 | 9 | N/A | mA |
| | | XA7S100 | N/A | 9 | N/A | 9 | 9 | N/A | mA |

**Notes:**

1. Typical values are specified at nominal voltage, 85°C junction temperature ($T_j$) with single-ended SelectIO™ resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the *Xilinx Power Estimator* spreadsheet tool [Ref 6] to estimate static power consumption for conditions other than those specified.

# Power-On/Off Power Supply Sequencing

The recommended power-on sequence is $V_{CCINT}$, $V_{CCBRAM}$, $V_{CCAUX}$, and $V_{CCO}$ to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If $V_{CCINT}$ and $V_{CCBRAM}$ have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If $V_{CCAUX}$ and $V_{CCO}$ have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously.

For $V_{CCO}$ voltages of 3.3V in HR I/O banks and configuration bank 0 the following conditions apply.

- The voltage difference between $V_{CCO}$ and $V_{CCAUX}$ must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

There is no recommended sequence for supplies not discussed in this section.

# LVDS DC Specifications (LVDS_25)

*Table 11:* **LVDS_25 DC Specifications**[1]

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCO}$ | Supply voltage. | | 2.375 | 2.500 | 2.625 | V |
| $V_{OH}$ | Output High voltage for Q and $\overline{Q}$. | $R_T$ = 100Ω across Q and $\overline{Q}$ signals. | – | – | 1.675 | V |
| $V_{OL}$ | Output Low voltage for Q and $\overline{Q}$. | $R_T$ = 100Ω across Q and $\overline{Q}$ signals. | 0.700 | – | – | V |
| $V_{ODIFF}$ | Differential output voltage:<br>(Q – $\overline{Q}$), Q = High<br>($\overline{Q}$ – Q), $\overline{Q}$ = High | $R_T$ = 100Ω across Q and $\overline{Q}$ signals. | 247 | 350 | 600 | mV |
| $V_{OCM}$ | Output common-mode voltage. | $R_T$ = 100Ω across Q and $\overline{Q}$ signals. | 1.000 | 1.250 | 1.425 | V |
| $V_{IDIFF}$ | Differential input voltage:<br>(Q – $\overline{Q}$), Q = High<br>($\overline{Q}$ – Q), $\overline{Q}$ = High | | 100 | 350 | 600 | mV |
| $V_{ICM}$ | Input common-mode voltage. | | 0.300 | 1.200 | 1.500 | V |

**Notes:**

1. Differential inputs for LVDS_25 can be placed in banks with $V_{CCO}$ levels that are different from the required level for outputs. Consult the *7 Series FPGAs SelectIO Resources User Guide* (UG471) [Ref 3] for more information.

*Table 14:* **Spartan-7 Device Production Software and Speed Specification Release**

| Device | $V_{CCINT}$ Operating Voltage, Speed Grade, and Temperature Range | | | | | |
|---|---|---|---|---|---|---|
| | 1.0V | | | | | 0.95V |
| | -2C | -2I | -1C | -1I | -1Q | -1LI |
| XC7S6 | Vivado tools 2018.2 v1.22 | | | | Vivado tools 2018.2.1 v1.23 | Vivado tools 2018.2 v1.22 |
| XC7S15 | Vivado tools 2018.2 v1.22 | | | | Vivado tools 2018.2.1 v1.23 | Vivado tools 2018.2 v1.22 |
| XC7S25 | Vivado tools 2017.4 v1.20 | | | | Vivado tools 2018.1 v1.21 | Vivado tools 2017.4 v1.20 |
| XC7S50 | Vivado tools 2017.2 v1.17 | | | | Vivado tools 2017.3 v1.19 | Vivado tools 2017.2 v1.17 |
| XC7S75 | Vivado tools 2018.1 v1.21 | | | | Vivado tools 2018.2.1 v1.23 | Vivado tools 2018.1 v1.21 |
| XC7S100 | Vivado tools 2018.1 v1.21 | | | | Vivado tools 2018.2.1 v1.23 | Vivado tools 2018.1 v1.21 |
| XA7S6 | N/A | Vivado tools 2018.2.1 v1.16 | N/A | Vivado tools 2018.2.1 v1.16 | | N/A |
| XA7S15 | N/A | Vivado tools 2018.2.1 v1.16 | N/A | Vivado tools 2018.2.1 v1.16 | | N/A |
| XA7S25 | N/A | Vivado tools 2018.1 v1.15 | N/A | Vivado tools 2018.1 v1.15 | | N/A |
| XA7S50 | N/A | Vivado tools 2017.3 v1.12 | N/A | Vivado tools 2017.3 v1.12 | | N/A |
| XA7S75 | N/A | Vivado tools 2018.2.1 v1.16 | N/A | Vivado tools 2018.2.1 v1.16 | | N/A |
| XA7S100 | N/A | Vivado tools 2018.2.1 v1.16 | N/A | Vivado tools 2018.2.1 v1.16 | | N/A |

# Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Spartan-7 FPGAs. These values are subject to the same guidelines as the AC Switching Characteristics, page 12.

*Table 15:* **Networking Applications Interface Performances**

| Description | $V_{CCINT}$ Operating Voltage, Speed Grade, and Temperature Range | | | Units |
|---|---|---|---|---|
| | 1.0V | | 0.95V | |
| | -2C/-2I | -1C/-1I/-1Q | -1LI | |
| SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8) | 680 | 600 | 600 | Mb/s |
| DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14) | 1250 | 950 | 950 | Mb/s |
| SDR LVDS receiver(1) | 680 | 600 | 600 | Mb/s |

*Table 20:* **Output Delay Measurement Methodology**

| Description | I/O Standard Attribute | $R_{REF}$ (Ω) | $C_{REF}$[1] (pF) | $V_{MEAS}$ (V) | $V_{REF}$ (V) |
|---|---|---|---|---|---|
| LVCMOS, 1.2V | LVCMOS12 | 1M | 0 | 0.6 | 0 |
| LVCMOS, 1.5V | LVCMOS15 | 1M | 0 | 0.75 | 0 |
| LVCMOS, 1.8V | LVCMOS18 | 1M | 0 | 0.9 | 0 |
| LVCMOS, 2.5V | LVCMOS25 | 1M | 0 | 1.25 | 0 |
| LVCMOS, 3.3V | LVCMOS33 | 1M | 0 | 1.65 | 0 |
| LVTTL, 3.3V | LVTTL | 1M | 0 | 1.65 | 0 |
| PCI33, 3.3V | PCI33_3 | 25 | 10 | 1.65 | 0 |
| HSTL (high-speed transceiver logic), Class I, 1.2V | HSTL_I_12 | 50 | 0 | $V_{REF}$ | 0.6 |
| HSTL, Class I, 1.5V | HSTL_I | 50 | 0 | $V_{REF}$ | 0.75 |
| HSTL, Class II, 1.5V | HSTL_II | 25 | 0 | $V_{REF}$ | 0.75 |
| HSTL, Class I, 1.8V | HSTL_I_18 | 50 | 0 | $V_{REF}$ | 0.9 |
| HSTL, Class II, 1.8V | HSTL_II_18 | 25 | 0 | $V_{REF}$ | 0.9 |
| HSUL (high-speed unterminated logic), 1.2V | HSUL_12 | 50 | 0 | $V_{REF}$ | 0.6 |
| SSTL12, 1.2V | SSTL12 | 50 | 0 | $V_{REF}$ | 0.6 |
| SSTL135/SSTL135_R, 1.35V | SSTL135, SSTL135_R | 50 | 0 | $V_{REF}$ | 0.675 |
| SSTL15/SSTL15_R, 1.5V | SSTL15, SSTL15_R | 50 | 0 | $V_{REF}$ | 0.75 |
| SSTL (stub-series terminated logic), Class I & Class II, 1.8V | SSTL18_I, SSTL18_II | 50 | 0 | $V_{REF}$ | 0.9 |
| DIFF_MOBILE_DDR, 1.8V | DIFF_MOBILE_DDR | 50 | 0 | $V_{REF}$ | 0.9 |
| DIFF_HSTL, Class I, 1.2V | DIFF_HSTL_I_12 | 50 | 0 | $V_{REF}$ | 0.6 |
| DIFF_HSTL, Class I & II, 1.5V | DIFF_HSTL_I, DIFF_HSTL_II | 50 | 0 | $V_{REF}$ | 0.75 |
| DIFF_HSTL, Class I & II, 1.8V | DIFF_HSTL_I_18, DIFF_HSTL_II_18 | 50 | 0 | $V_{REF}$ | 0.9 |
| DIFF_HSUL_12, 1.2V | DIFF_HSUL_12 | 50 | 0 | $V_{REF}$ | 0.6 |
| DIFF_SSTL135/DIFF_SSTL135_R, 1.35V | DIFF_SSTL135, DIFF_SSTL135_R | 50 | 0 | $V_{REF}$ | 0.675 |
| DIFF_SSTL15/DIFF_SSTL15_R, 1.5V | DIFF_SSTL15, DIFF_SSTL15_R | 50 | 0 | $V_{REF}$ | 0.75 |
| DIFF_SSTL18, Class I & II, 1.8V | DIFF_SSTL18_I, DIFF_SSTL18_II | 50 | 0 | $V_{REF}$ | 0.9 |
| LVDS, 2.5V | LVDS_25 | 100 | 0 | 0[2] | 0 |
| BLVDS (Bus LVDS), 2.5V | BLVDS_25 | 100 | 0 | 0[2] | 0 |
| Mini LVDS, 2.5V | MINI_LVDS_25 | 100 | 0 | 0[2] | 0 |
| PPDS_25 | PPDS_25 | 100 | 0 | 0[2] | 0 |
| RSDS_25 | RSDS_25 | 100 | 0 | 0[2] | 0 |
| TMDS_33 | TMDS_33 | 50 | 0 | 0[2] | 3.3 |

**Notes:**

1. $C_{REF}$ is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

# Input/Output Logic Switching Characteristics

*Table 21:* **ILOGIC Switching Characteristics**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| **Setup/Hold** | | | | | |
| $T_{ICE1CK}/T_{ICKCE1}$ | CE1 pin setup/hold with respect to CLK. | 0.54/0.02 | 0.76/0.02 | 0.76/0.02 | ns |
| $T_{ISRCK}/T_{ICKSR}$ | SR pin setup/hold with respect to CLK. | 0.70/0.01 | 1.13/0.01 | 1.13/0.01 | ns |
| $T_{IDOCK}/T_{IOCKD}$ | D pin setup/hold with respect to CLK without delay. | 0.01/0.29 | 0.01/0.33 | 0.01/0.33 | ns |
| $T_{IDOCKD}/T_{IOCKDD}$ | DDLY pin setup/hold with respect to CLK (using IDELAY). | 0.02/0.29 | 0.02/0.33 | 0.02/0.33 | ns |
| **Combinatorial** | | | | | |
| $T_{IDI}$ | D pin to O pin propagation delay, no delay. | 0.11 | 0.13 | 0.13 | ns |
| $T_{IDID}$ | DDLY pin to O pin propagation delay (using IDELAY). | 0.12 | 0.14 | 0.14 | ns |
| **Sequential Delays** | | | | | |
| $T_{IDLO}$ | D pin to Q1 pin using flip-flop as a latch without delay. | 0.44 | 0.51 | 0.51 | ns |
| $T_{IDLOD}$ | DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY). | 0.44 | 0.51 | 0.51 | ns |
| $T_{ICKQ}$ | CLK to Q outputs. | 0.57 | 0.66 | 0.66 | ns |
| $T_{RQ\_ILOGIC}$ | SR pin to OQ/TQ out. | 1.08 | 1.32 | 1.32 | ns |
| $T_{GSRQ\_ILOGIC}$ | Global set/reset to Q outputs. | 7.60 | 10.51 | 10.51 | ns |
| **Set/Reset** | | | | | |
| $T_{RPW\_ILOGIC}$ | Minimum pulse width, SR inputs. | 0.72 | 0.72 | 0.72 | ns, Min |

# Input Serializer/Deserializer Switching Characteristics

*Table 23:* **ISERDES Switching Characteristics**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| **Setup/Hold for Control Lines** | | | | | |
| $T_{ISCCK\_BITSLIP}$/ $T_{ISCKC\_BITSLIP}$ | BITSLIP pin setup/hold with respect to CLKDIV. | 0.02/0.15 | 0.02/0.17 | 0.02/0.17 | ns |
| $T_{ISCCK\_CE}$/ $T_{ISCKC\_CE}$ | CE pin setup/hold with respect to CLK (for CE1). | 0.50/–0.01 | 0.72/–0.01 | 0.72/–0.01 | ns |
| $T_{ISCCK\_CE2}$/ $T_{ISCKC\_CE2}$ | CE pin setup/hold with respect to CLKDIV (for CE2). | –0.10/0.36 | –0.10/0.40 | –0.10/0.40 | ns |
| **Setup/Hold for Data Lines** | | | | | |
| $T_{ISDCK\_D}$/ $T_{ISCKD\_D}$ | D pin setup/hold with respect to CLK. | –0.02/0.14 | –0.02/0.17 | –0.02/0.17 | ns |
| $T_{ISDCK\_DDLY}$/ $T_{ISCKD\_DDLY}$ | DDLY pin setup/hold with respect to CLK (using IDELAY).(1) | –0.02/0.14 | –0.02/0.17 | –0.02/0.17 | ns |
| $T_{ISDCK\_D\_DDR}$/ $T_{ISCKD\_D\_DDR}$ | D pin setup/hold with respect to CLK at DDR mode. | –0.02/0.14 | –0.02/0.17 | –0.02/0.17 | ns |
| $T_{ISDCK\_DDLY\_DDR}$/ $T_{ISCKD\_DDLY\_DDR}$ | D pin setup/hold with respect to CLK at DDR mode (using IDELAY).(1) | 0.14/0.14 | 0.17/0.17 | 0.17/0.17 | ns |
| **Sequential Delays** | | | | | |
| $T_{ISCKO\_Q}$ | CLKDIV to out at Q pin. | 0.54 | 0.66 | 0.66 | ns |
| **Propagation Delays** | | | | | |
| $T_{ISDO\_DO}$ | D input to DO output pin. | 0.11 | 0.13 | 0.13 | ns |

**Notes:**

1. Recorded at 0 tap value.

# CLB Switching Characteristics

*Table 27:* **CLB Switching Characteristics**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| **Combinatorial Delays** | | | | | |
| $T_{ILO}$ | An – Dn LUT address to A. | 0.11 | 0.13 | 0.13 | ns, Max |
| $T_{ILO\_2}$ | An – Dn LUT address to AMUX/CMUX. | 0.30 | 0.36 | 0.36 | ns, Max |
| $T_{ILO\_3}$ | An – Dn LUT address to BMUX_A. | 0.46 | 0.55 | 0.55 | ns, Max |
| $T_{ITO}$ | An – Dn inputs to A – D Q outputs. | 1.05 | 1.27 | 1.27 | ns, Max |
| $T_{AXA}$ | AX inputs to AMUX output. | 0.69 | 0.84 | 0.84 | ns, Max |
| $T_{AXB}$ | AX inputs to BMUX output. | 0.66 | 0.83 | 0.83 | ns, Max |
| $T_{AXC}$ | AX inputs to CMUX output. | 0.68 | 0.82 | 0.82 | ns, Max |
| $T_{AXD}$ | AX inputs to DMUX output. | 0.75 | 0.90 | 0.90 | ns, Max |
| $T_{BXB}$ | BX inputs to BMUX output. | 0.57 | 0.69 | 0.69 | ns, Max |
| $T_{BXD}$ | BX inputs to DMUX output. | 0.69 | 0.82 | 0.82 | ns, Max |
| $T_{CXC}$ | CX inputs to CMUX output. | 0.48 | 0.58 | 0.58 | ns, Max |
| $T_{CXD}$ | CX inputs to DMUX output. | 0.59 | 0.71 | 0.71 | ns, Max |
| $T_{DXD}$ | DX inputs to DMUX output. | 0.58 | 0.70 | 0.70 | ns, Max |
| **Sequential Delays** | | | | | |
| $T_{CKO}$ | Clock to AQ – DQ outputs. | 0.44 | 0.53 | 0.53 | ns, Max |
| $T_{SHCKO}$ | Clock to AMUX – DMUX outputs. | 0.53 | 0.66 | 0.66 | ns, Max |
| **Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK** | | | | | |
| $T_{AS}/T_{AH}$ | AN – DN input to CLK on A – D flip-flops. | 0.09/0.14 | 0.11/0.18 | 0.11/0.18 | ns, Min |
| $T_{DICK}/T_{CKDI}$ | AX – DX input to CLK on A – D flip-flops. | 0.07/0.21 | 0.09/0.26 | 0.09/0.26 | ns, Min |
| | AX – DX input through MUXs and/or carry logic to CLK on A – D flip-flops. | 0.66/0.09 | 0.81/0.11 | 0.81/0.11 | ns, Min |
| $T_{CECK\_CLB}/T_{CKCE\_CLB}$ | CE input to CLK on A – D flip-flops. | 0.17/0.00 | 0.21/0.01 | 0.21/0.01 | ns, Min |
| $T_{SRCK}/T_{CKSR}$ | SR input to CLK on A – D flip-flops. | 0.43/0.04 | 0.53/0.05 | 0.53/0.05 | ns, Min |
| **Set/Reset** | | | | | |
| $T_{SRMIN}$ | SR input minimum pulse width. | 0.78 | 1.04 | 1.04 | ns, Min |
| $T_{RQ}$ | Delay from SR input to AQ – DQ flip-flops. | 0.59 | 0.71 | 0.71 | ns, Max |
| $T_{CEO}$ | Delay from CE input to AQ – DQ flip-flops. | 0.58 | 0.70 | 0.70 | ns, Max |
| $F_{TOG}$ | Toggle frequency (for export control). | 1286 | 1098 | 1098 | MHz |

# Block RAM and FIFO Switching Characteristics

*Table 30:* **Block RAM and FIFO Switching Characteristics**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| **Block RAM and FIFO Clock-to-Out Delays** | | | | | |
| $T_{RCKO\_DO}$ and $T_{RCKO\_DO\_REG}$ | Clock CLK to DOUT output (without output register).(1)(2) | 2.13 | 2.46 | 2.46 | ns, Max |
| | Clock CLK to DOUT output (with output register).(3)(4) | 0.74 | 0.89 | 0.89 | ns, Max |
| $T_{RCKO\_DO\_ECC}$ and $T_{RCKO\_DO\_ECC\_REG}$ | Clock CLK to DOUT output with ECC (without output register).(1)(2) | 3.04 | 3.84 | 3.84 | ns, Max |
| | Clock CLK to DOUT output with ECC (with output register).(3)(4) | 0.81 | 0.94 | 0.94 | ns, Max |
| $T_{RCKO\_DO\_CASCOUT}$ and $T_{RCKO\_DO\_CASCOUT\_REG}$ | Clock CLK to DOUT output with cascade (without output register).(1) | 2.88 | 3.30 | 3.30 | ns, Max |
| | Clock CLK to DOUT output with cascade (with output register).(3) | 1.28 | 1.46 | 1.46 | ns, Max |
| $T_{RCKO\_FLAGS}$ | Clock CLK to FIFO flags outputs.(5) | 0.87 | 1.05 | 1.05 | ns, Max |
| $T_{RCKO\_POINTERS}$ | Clock CLK to FIFO pointers outputs.(6) | 1.02 | 1.15 | 1.15 | ns, Max |
| $T_{RCKO\_PARITY\_ECC}$ | Clock CLK to ECCPARITY in ECC encode only mode. | 0.85 | 0.94 | 0.94 | ns, Max |
| $T_{RCKO\_SDBIT\_ECC}$ and $T_{RCKO\_SDBIT\_ECC\_REG}$ | Clock CLK to BITERR (without output register). | 2.81 | 3.55 | 3.55 | ns, Max |
| | Clock CLK to BITERR (with output register). | 0.76 | 0.89 | 0.89 | ns, Max |
| $T_{RCKO\_RDADDR\_ECC}$ and $T_{RCKO\_RDADDR\_ECC\_REG}$ | Clock CLK to RDADDR output with ECC (without output register). | 0.88 | 1.07 | 1.07 | ns, Max |
| | Clock CLK to RDADDR output with ECC (with output register). | 0.93 | 1.08 | 1.08 | ns, Max |
| **Setup and Hold Times Before/After Clock CLK** | | | | | |
| $T_{RCCK\_ADDRA}$/ $T_{RCKC\_ADDRA}$ | ADDR inputs.(7) | 0.49/0.33 | 0.57/0.36 | 0.57/0.36 | ns, Min |
| $T_{RDCK\_DI\_WF\_NC}$/ $T_{RCKD\_DI\_WF\_NC}$ | Data input setup/hold time when block RAM is configured in WRITE_FIRST or NO_CHANGE mode.(8) | 0.65/0.63 | 0.74/0.67 | 0.74/0.67 | ns, Min |
| $T_{RDCK\_DI\_RF}$/ $T_{RCKD\_DI\_RF}$ | Data input setup/hold time when block RAM is configured in READ_FIRST mode.(8) | 0.22/0.34 | 0.25/0.41 | 0.25/0.41 | ns, Min |
| $T_{RDCK\_DI\_ECC}$/ $T_{RCKD\_DI\_ECC}$ | DIN inputs with block RAM ECC in standard mode.(8) | 0.55/0.46 | 0.63/0.50 | 0.63/0.50 | ns, Min |
| $T_{RDCK\_DI\_ECCW}$/ $T_{RCKD\_DI\_ECCW}$ | DIN inputs with block RAM ECC encode only.(8) | 1.02/0.46 | 1.17/0.50 | 1.17/0.50 | ns, Min |

*Table 30:* **Block RAM and FIFO Switching Characteristics *(Cont'd)***

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| $T_{RDCK\_DI\_ECC\_FIFO}$/ $T_{RCKD\_DI\_ECC\_FIFO}$ | DIN inputs with FIFO ECC in standard mode.(8) | 1.15/0.59 | 1.32/0.64 | 1.32/0.64 | ns, Min |
| $T_{RCCK\_INJECTBITERR}$/ $T_{RCKC\_INJECTBITERR}$ | Inject single/double bit error in ECC mode. | 0.64/0.37 | 0.74/0.40 | 0.74/0.40 | ns, Min |
| $T_{RCCK\_EN}$/$T_{RCKC\_EN}$ | Block RAM enable (EN) input. | 0.39/0.21 | 0.45/0.23 | 0.45/0.23 | ns, Min |
| $T_{RCCK\_REGCE}$/ $T_{RCKC\_REGCE}$ | CE input of output register. | 0.29/0.15 | 0.36/0.16 | 0.36/0.16 | ns, Min |
| $T_{RCCK\_RSTREG}$/ $T_{RCKC\_RSTREG}$ | Synchronous RSTREG input. | 0.32/0.07 | 0.35/0.07 | 0.35/0.07 | ns, Min |
| $T_{RCCK\_RSTRAM}$/ $T_{RCKC\_RSTRAM}$ | Synchronous RSTRAM input. | 0.34/0.43 | 0.36/0.46 | 0.36/0.46 | ns, Min |
| $T_{RCCK\_WEA}$/$T_{RCKC\_WEA}$ | Write enable (WE) input (block RAM only). | 0.48/0.19 | 0.54/0.20 | 0.54/0.20 | ns, Min |
| $T_{RCCK\_WREN}$/ $T_{RCKC\_WREN}$ | WREN FIFO inputs. | 0.46/0.35 | 0.47/0.43 | 0.47/0.43 | ns, Min |
| $T_{RCCK\_RDEN}$/ $T_{RCKC\_RDEN}$ | RDEN FIFO inputs. | 0.43/0.35 | 0.43/0.43 | 0.43/0.43 | ns, Min |
| **Reset Delays** | | | | | |
| $T_{RCO\_FLAGS}$ | Reset RST to FIFO flags/pointers.(9) | 0.98 | 1.10 | 1.10 | ns, Max |
| $T_{RREC\_RST}$/$T_{RREM\_RST}$ | FIFO reset recovery and removal timing.(10) | 2.07/–0.81 | 2.37/–0.81 | 2.37/–0.81 | ns, Max |
| **Maximum Frequency** | | | | | |
| $F_{MAX\_BRAM\_WF\_NC}$ | Block RAM (write first and no change modes) when not in SDP RF mode. | 460.83 | 388.20 | 388.20 | MHz |
| $F_{MAX\_BRAM\_RF\_PERFORMANCE}$ | Block RAM (read first, performance mode) when in SDP RF mode but no address overlap between port A and port B. | 460.83 | 388.20 | 388.20 | MHz |
| $F_{MAX\_BRAM\_RF\_DELAYED\_WRITE}$ | Block RAM (read first, delayed write mode) when in SDP RF mode and there is possibility of overlap between port A and port B addresses. | 404.53 | 339.67 | 339.67 | MHz |
| $F_{MAX\_CAS\_WF\_NC}$ | Block RAM cascade (write first, no change mode) when cascade but not in RF mode. | 418.59 | 345.78 | 345.78 | MHz |
| $F_{MAX\_CAS\_RF\_PERFORMANCE}$ | Block RAM cascade (read first, performance mode) when in cascade with RF mode and no possibility of address overlap/one port is disabled. | 418.59 | 345.78 | 345.78 | MHz |

# DSP48E1 Switching Characteristics

*Table 31:* **DSP48E1 Switching Characteristics**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| **Setup and Hold Times of Data/Control Pins to the Input Register Clock** | | | | | |
| $T_{DSPDCK\_A\_AREG}$/ $T_{DSPCKD\_A\_AREG}$ | A input to A register CLK. | 0.30/ 0.13 | 0.37/ 0.14 | 0.37/ 0.14 | ns |
| $T_{DSPDCK\_B\_BREG}$/ $T_{DSPCKD\_B\_BREG}$ | B input to B register CLK. | 0.38/ 0.16 | 0.45/ 0.18 | 0.45/ 0.18 | ns |
| $T_{DSPDCK\_C\_CREG}$/ $T_{DSPCKD\_C\_CREG}$ | C input to C register CLK. | 0.20/ 0.19 | 0.24/ 0.21 | 0.24/ 0.21 | ns |
| $T_{DSPDCK\_D\_DREG}$/ $T_{DSPCKD\_D\_DREG}$ | D input to D register CLK. | 0.32/ 0.27 | 0.42/ 0.27 | 0.42/ 0.27 | ns |
| $T_{DSPDCK\_ACIN\_AREG}$/ $T_{DSPCKD\_ACIN\_AREG}$ | ACIN input to A register CLK. | 0.27/ 0.13 | 0.32/ 0.14 | 0.32/ 0.14 | ns |
| $T_{DSPDCK\_BCIN\_BREG}$/ $T_{DSPCKD\_BCIN\_BREG}$ | BCIN input to B register CLK. | 0.29/ 0.16 | 0.36/ 0.18 | 0.36/ 0.18 | ns |
| **Setup and Hold Times of Data Pins to the Pipeline Register Clock** | | | | | |
| $T_{DSPDCK\_\{A, B\}\_MREG\_MULT}$/ $T_{DSPCKD\_\{A, B\}\_MREG\_MULT}$ | {A, B} input to M register CLK using multiplier. | 2.76/ –0.01 | 3.29/ –0.01 | 3.29/ –0.01 | ns |
| $T_{DSPDCK\_\{A, D\}\_ADREG}$/ $T_{DSPCKD\_\{A, D\}\_ADREG}$ | {A, D} input to AD register CLK. | 1.48/ –0.02 | 1.76/ –0.02 | 1.76/ –0.02 | ns |
| **Setup and Hold Times of Data/Control Pins to the Output Register Clock** | | | | | |
| $T_{DSPDCK\_\{A, B\}\_PREG\_MULT}$/ $T_{DSPCKD\_\{A, B\}\_PREG\_MULT}$ | {A, B} input to P register CLK using multiplier. | 4.60/ –0.28 | 5.48/ –0.28 | 5.48/ –0.28 | ns |
| $T_{DSPDCK\_D\_PREG\_MULT}$/ $T_{DSPCKD\_D\_PREG\_MULT}$ | D input to P register CLK using multiplier. | 4.50/ –0.73 | 5.35/ –0.73 | 5.35/ –0.73 | ns |
| $T_{DSPDCK\_\{A, B\}\_PREG}$/ $T_{DSPCKD\_\{A, B\}\_PREG}$ | A or B input to P register CLK not using multiplier. | 1.98/ –0.28 | 2.35/ –0.28 | 2.35/ –0.28 | ns |
| $T_{DSPDCK\_C\_PREG}$/ $T_{DSPCKD\_C\_PREG}$ | C input to P register CLK not using multiplier. | 1.76/ –0.26 | 2.10/ –0.26 | 2.10/ –0.26 | ns |
| $T_{DSPDCK\_PCIN\_PREG}$/ $T_{DSPCKD\_PCIN\_PREG}$ | PCIN input to P register CLK. | 1.51/ –0.15 | 1.80/ –0.15 | 1.80/ –0.15 | ns |
| **Setup and Hold Times of the CE Pins** | | | | | |
| $T_{DSPDCK\_\{CEA;CEB\}\_\{AREG;BREG\}}$/ $T_{DSPCKD\_\{CEA;CEB\}\_\{AREG;BREG\}}$ | {CEA; CEB} input to {A; B} register CLK. | 0.42/ 0.08 | 0.52/ 0.11 | 0.52/ 0.11 | ns |
| $T_{DSPDCK\_CEC\_CREG}$/ $T_{DSPCKD\_CEC\_CREG}$ | CEC input to C register CLK. | 0.34/ 0.11 | 0.42/ 0.13 | 0.42/ 0.13 | ns |
| $T_{DSPDCK\_CED\_DREG}$/ $T_{DSPCKD\_CED\_DREG}$ | CED input to D register CLK. | 0.43/ –0.03 | 0.52/ –0.03 | 0.52/ –0.03 | ns |

# Device Pin-to-Pin Output Parameter Guidelines

*Table 39:* **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)[1]**

| Symbol | Description | Device | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | 1.0V | | 0.95V | |
| | | | -2 | -1 | -1L | |
| **SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM/PLL.** | | | | | | |
| $T_{ICKOF}$ | Clock-capable clock input and OUTFF at pins/banks closest to the BUFGs *without* MMCM/PLL (near clock region).[2] | XC7S6 | 5.55 | 6.50 | 6.50 | ns |
| | | XC7S15 | 5.55 | 6.50 | 6.50 | ns |
| | | XC7S25 | 5.55 | 6.44 | 6.44 | ns |
| | | XC7S50 | 5.71 | 6.62 | 6.62 | ns |
| | | XC7S75 | 5.73 | 6.71 | 6.71 | ns |
| | | XC7S100 | 5.73 | 6.71 | 6.71 | ns |
| | | XA7S6 | 5.55 | 6.50 | N/A | ns |
| | | XA7S15 | 5.55 | 6.50 | N/A | ns |
| | | XA7S25 | 5.55 | 6.44 | N/A | ns |
| | | XA7S50 | 5.71 | 6.62 | N/A | ns |
| | | XA7S75 | 5.73 | 6.71 | N/A | ns |
| | | XA7S100 | 5.73 | 6.71 | N/A | ns |

**Notes:**

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Refer to the *Die Level Bank Numbering Overview* section of the *7 Series FPGA Packaging and Pinout Specification* (UG475) [Ref 4].

*Table 42:* **Clock-Capable Clock Input to Output Delay With PLL(1)**

| Symbol | Description | Device | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | 1.0V | | 0.95V | |
| | | | -2 | -1 | -1L | |
| **SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *with* PLL.** | | | | | | |
| $T_{ICKOFPLLCC}$ | Clock-capable clock input and OUTFF *with* PLL.(2) | XC7S6 | 0.85 | 0.85 | 0.85 | ns |
| | | XC7S15 | 0.85 | 0.85 | 0.85 | ns |
| | | XC7S25 | 0.83 | 0.83 | 0.83 | ns |
| | | XC7S50 | 0.83 | 0.83 | 0.83 | ns |
| | | XC7S75 | 0.83 | 0.83 | 0.83 | ns |
| | | XC7S100 | 0.83 | 0.83 | 0.83 | ns |
| | | XA7S6 | 0.85 | 0.85 | N/A | ns |
| | | XA7S15 | 0.85 | 0.85 | N/A | ns |
| | | XA7S25 | 0.83 | 0.83 | N/A | ns |
| | | XA7S50 | 0.83 | 0.83 | N/A | ns |
| | | XA7S75 | 0.83 | 0.83 | N/A | ns |
| | | XA7S100 | 0.83 | 0.83 | N/A | ns |

**Notes:**

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is already included in the timing calculation.

*Table 43:* **Pin-to-Pin, Clock-to-Out using BUFIO**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| **SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with BUFIO.** | | | | | |
| $T_{ICKOFCS}$ | Clock to out of I/O clock. | 5.61 | 6.64 | 6.64 | ns |

# Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

*Table 44:* **Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks**

| Symbol | Description | Device | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | 1.0V | | 0.95V | |
| | | | -2 | -1 | -1L | |
| **Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1)** | | | | | | |
| $T_{PSFD}$/ $T_{PHFD}$ | Full delay (legacy delay or default delay) global clock input and IFF(2) without MMCM/PLL with ZHOLD_DELAY on HR I/O banks. | XC7S6 | 2.76/–0.40 | 3.17/–0.40 | 3.17/–0.40 | ns |
| | | XC7S15 | 2.76/–0.40 | 3.17/–0.40 | 3.17/–0.40 | ns |
| | | XC7S25 | 2.67/–0.37 | 3.12/–0.37 | 3.12/–0.37 | ns |
| | | XC7S50 | 2.66/–0.28 | 3.11/–0.28 | 3.11/–0.28 | ns |
| | | XC7S75 | 2.91/–0.33 | 3.36/–0.33 | 3.36/–0.33 | ns |
| | | XC7S100 | 2.91/–0.33 | 3.36/–0.33 | 3.36/–0.33 | ns |
| | | XA7S6 | 2.76/–0.40 | 3.17/–0.40 | N/A | ns |
| | | XA7S15 | 2.76/–0.40 | 3.17/–0.40 | N/A | ns |
| | | XA7S25 | 2.67/–0.37 | 3.12/–0.37 | N/A | ns |
| | | XA7S50 | 2.66/–0.28 | 3.11/–0.28 | N/A | ns |
| | | XA7S75 | 2.91/–0.33 | 3.36/–0.33 | N/A | ns |
| | | XA7S100 | 2.91/–0.33 | 3.36/–0.33 | N/A | ns |

**Notes:**

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch.

*Table 46:* **Clock-Capable Clock Input Setup and Hold With PLL**

| Symbol | Description | Device | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | 1.0V | | 0.95V | |
| | | | -2 | -1 | -1L | |
| **Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard.(1)(2)** | | | | | | |
| $T_{PSPLLCC}$/ $T_{PHPLLCC}$ | No delay clock-capable clock input and IFF(3) with PLL. | XC7S6 | 3.07/–0.17 | 3.69/–0.17 | 3.69/–0.17 | ns |
| | | XC7S15 | 3.07/–0.17 | 3.69/–0.17 | 3.69/–0.17 | ns |
| | | XC7S25 | 3.04/–0.19 | 3.64/–0.19 | 3.64/–0.19 | ns |
| | | XC7S50 | 3.15/–0.19 | 3.77/–0.19 | 3.77/–0.19 | ns |
| | | XC7S75 | 3.15/–0.19 | 3.78/–0.19 | 3.78/–0.19 | ns |
| | | XC7S100 | 3.15/–0.19 | 3.78/–0.19 | 3.78/–0.19 | ns |
| | | XA7S6 | 3.07/–0.17 | 3.69/–0.17 | N/A | ns |
| | | XA7S15 | 3.07/–0.17 | 3.69/–0.17 | N/A | ns |
| | | XA7S25 | 3.04/–0.19 | 3.64/–0.19 | N/A | ns |
| | | XA7S50 | 3.15/–0.19 | 3.77/–0.19 | N/A | ns |
| | | XA7S75 | 3.15/–0.19 | 3.78/–0.19 | N/A | ns |
| | | XA7S100 | 3.15/–0.19 | 3.78/–0.19 | N/A | ns |

**Notes:**

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. Use IBIS to determine any duty-cycle distortion incurred using various standards.
3. IFF = Input flip-flop or latch.

*Table 47:* **Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| **Input Setup and Hold Time Relative to a Forwarded Clock Input Pin Using BUFIO for SSTL15 Standard.** | | | | | |
| $T_{PSCS}$/$T_{PHCS}$ | Setup and hold of I/O clock. | –0.38/1.46 | –0.38/1.73 | –0.38/1.76 | ns |

*Table 48:* **Sample Window**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| $T_{SAMP}$ | Sampling error at receiver pins.(1) | 0.64 | 0.70 | 0.70 | ns |
| $T_{SAMP\_BUFIO}$ | Sampling error at receiver pins using BUFIO.(2) | 0.40 | 0.46 | 0.46 | ns |

**Notes:**

1. This parameter indicates the total sampling error of the Spartan-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 MMCM jitter
   - MMCM accuracy (phase offset)
   - MMCM phase shift resolution

   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of the Spartan-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

# Configuration Switching Characteristics

*Table 51:* **Configuration Switching Characteristics**

| Symbol | Description | $V_{CCINT}$ Operating Voltage and Speed Grade | | | Units |
|---|---|---|---|---|---|
| | | 1.0V | | 0.95V | |
| | | -2 | -1 | -1L | |
| **Power-up Timing Characteristics** | | | | | |
| $T_{PL}$ (1) | Program latency. | 5.00 | 5.00 | 5.00 | ms, Max |
| $T_{POR}$ (2) | Power-on reset (50 ms ramp rate time). | 10/50 | 10/50 | 10/50 | ms, Min/Max |
| | Power-on reset (1 ms ramp rate time). | 10/35 | 10/35 | 10/35 | ms, Min/Max |
| $T_{PROGRAM}$ | Program pulse width. | 250.00 | 250.00 | 250.00 | ns, Min |
| **CCLK Output (Master Mode)** | | | | | |
| $T_{ICCK}$ | Master CCLK output delay. | 150.00 | 150.00 | 150.00 | ns, Min |
| $T_{MCCKL}$ | Master CCLK clock Low time duty cycle. | 40/60 | 40/60 | 40/60 | %, Min/Max |
| $T_{MCCKH}$ | Master CCLK clock High time duty cycle. | 40/60 | 40/60 | 40/60 | %, Min/Max |
| $F_{MCCK}$ | Master CCLK frequency. | 100.00 | 100.00 | 100.00 | MHz, Max |
| | Master CCLK frequency for AES encrypted x16. (2) | 50.00 | 50.00 | 50.00 | MHz, Max |
| $F_{MCCK\_START}$ | Master CCLK frequency at start of configuration. | 3.00 | 3.00 | 3.00 | MHz, Typ |
| $F_{MCCKTOL}$ | Frequency tolerance, master mode with respect to nominal CCLK. | ±50 | ±50 | ±50 | %, Max |
| **CCLK Input (Slave Modes)** | | | | | |
| $T_{SCCKL}$ | Slave CCLK clock minimum Low time. | 2.50 | 2.50 | 2.50 | ns, Min |
| $T_{SCCKH}$ | Slave CCLK clock minimum High time. | 2.50 | 2.50 | 2.50 | ns, Min |
| $F_{SCCK}$ | Slave CCLK frequency. | 100.00 | 100.00 | 100.00 | MHz, Max |
| **EMCCLK Input (Master Mode)** | | | | | |
| $T_{EMCCKL}$ | External master CCLK Low time. | 2.50 | 2.50 | 2.50 | ns, Min |
| $T_{EMCCKH}$ | External master CCLK High time. | 2.50 | 2.50 | 2.50 | ns, Min |
| $F_{EMCCK}$ | External master CCLK frequency. | 100.00 | 100.00 | 100.00 | MHz, Max |
| **Internal Configuration Access Port** | | | | | |
| $F_{ICAPCK}$ | Internal configuration access port (ICAPE2) clock frequency. | 100.00 | 100.00 | 100.00 | MHz, Max |
| **Master/Slave Serial Mode Programming Switching** | | | | | |
| $T_{DCCK}$/ $T_{CCKD}$ | $D_{IN}$ setup/hold. | 4.00/0.00 | 4.00/0.00 | 4.00/0.00 | ns, Min |
| $T_{CCO}$ | $D_{OUT}$ clock to out. | 8.00 | 8.00 | 8.00 | ns, Max |
| **SelectMAP Mode Programming Switching** | | | | | |
| $T_{SMDCCK}$/ $T_{SMCCKD}$ | D[31:00] setup/hold. | 4.00/0.00 | 4.00/0.00 | 4.00/0.00 | ns, Min |

# eFUSE Programming Conditions

Table 52 lists the programming conditions specifically for eFUSE. For more information, see the *7 Series FPGA Configuration User Guide* (UG470) [Ref 10].

*Table 52:* **eFUSE Programming Conditions(1)**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $I_{FS}$ | $V_{CCAUX}$ supply current | – | – | 115 | mA |
| $T_j$ | Temperature range | 15 | – | 125 | °C |

**Notes:**

1. The FPGA must not be configured during eFUSE programming.

# References

1. *7 Series FPGAs Overview* (DS180)
2. *XA Spartan-7 Automotive FPGA Data Sheet: Overview* (DS171)
3. *7 Series FPGAs SelectIO Resources User Guide* (UG471)
4. *7 Series FPGA Packaging and Pinout Specification* (UG475)
5. *7 Series FPGAs PCB Design Guide* (UG483)
6. *Xilinx Power Estimator* spreadsheet tool (XPE)
7. *Zynq-7000 AP SoC and 7 Series FPGAs Memory Interface Solutions User Guide* (UG586)
8. See the Clocking Wizard in Vivado software.
9. *7 Series FPGAs and Zynq-7000 AP SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480)
10. *7 Series FPGA Configuration User Guide* (UG470)