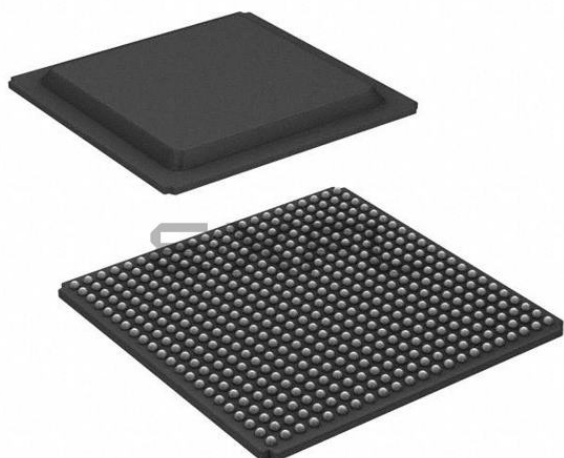




Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	6000
Number of Logic Elements/Cells	76800
Total RAM Bits	4331520
Number of I/O	338
Number of Gates	-
Voltage - Supply	0.95V ~ 1.05V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7s75-2fgga484i

Table 1: Absolute Maximum Ratings⁽¹⁾ (Cont'd)

Symbol	Description	Min	Max	Units
$V_{IN}^{(2)(3)(4)}$	I/O input voltage.	−0.4	$V_{CCO} + 0.55$	V
	I/O input voltage (when $V_{CCO} = 3.3V$) for V_{REF} and differential I/O standards except TMDS_33. ⁽⁵⁾	−0.4	2.625	V
V_{CCBATT}	Key memory battery backup supply.	−0.5	2.0	V
XADC				
V_{CCADC}	XADC supply relative to GNDADC.	−0.5	2.0	V
V_{REFP}	XADC reference input relative to GNDADC.	−0.5	2.0	V
Temperature				
T_{STG}	Storage temperature (ambient).	−65	150	°C
T_{SOL}	Maximum soldering temperature for Pb/Sn component bodies. ⁽⁶⁾	—	+220	°C
	Maximum soldering temperature for Pb-free component bodies. ⁽⁶⁾	—	+260	°C
T_j	Maximum junction temperature. ⁽⁶⁾	—	+125	°C

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
- The lower absolute voltage specification always applies.
- For I/O operation, refer to the *7 Series FPGAs SelectIO Resources User Guide* (UG471) [Ref 3].
- The maximum limit applies to DC signals. For maximum undershoot and overshoot AC specifications, see Table 4.
- See Table 9 for TMDS_33 specifications.
- For soldering guidelines and thermal considerations, see the *7 Series FPGA Packaging and Pinout Specification* (UG475) [Ref 4].

Table 2: Recommended Operating Conditions⁽¹⁾⁽²⁾

Symbol	Description	Min	Typ	Max	Units
FPGA Logic					
$V_{CCINT}^{(3)}$	For -2 and -1 (1.0V) devices: internal supply voltage.	0.95	1.00	1.05	V
	For -1L (0.95V) devices: internal supply voltage.	0.92	0.95	0.98	V
V_{CCAUX}	Auxiliary supply voltage.	1.71	1.80	1.89	V
$V_{CCBRAM}^{(3)}$	For -2 and -1 (1.0V) devices: block RAM supply voltage.	0.95	1.00	1.05	V
	For -1L (0.95V) devices: block RAM supply voltage.	0.92	0.95	0.98	V
$V_{CCO}^{(4)(5)}$	Supply voltage for HR I/O banks.	1.14	–	3.465	V
$V_{IN}^{(6)}$	I/O input voltage.	–0.20	–	$V_{CCO} + 0.20$	V
	I/O input voltage (when $V_{CCO} = 3.3V$) for V_{REF} and differential I/O standards except TMD5_33. ⁽⁷⁾	–0.20	–	2.625	V
$I_{IN}^{(8)}$	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	–	–	10	mA
$V_{CCBATT}^{(9)}$	Battery voltage.	1.0	–	1.89	V
XADC					
V_{CCADC}	XADC supply relative to GNDADC.	1.71	1.80	1.89	V
V_{REFP}	Externally supplied reference voltage.	1.20	1.25	1.30	V
Temperature					
T_j	Junction temperature operating range for commercial (C) temperature devices.	0	–	85	°C
	Junction temperature operating range for industrial (I) temperature devices.	–40	–	100	°C
	Junction temperature operating range for expanded (Q) temperature devices.	–40	–	125	°C

Notes:

- All voltages are relative to ground.
- For the design of the power distribution system consult the *7 Series FPGAs PCB Design Guide* (UG483) [Ref 5].
- If V_{CCINT} and V_{CCBRAM} are operating at the same voltage, V_{CCINT} and V_{CCBRAM} should be connected to the same supply.
- Configuration data is retained even if V_{CCO} drops to 0V.
- Includes V_{CCO} of 1.2V, 1.35V, 1.5V, 1.8V, 2.5V, and 3.3V at $\pm 5\%$.
- The lower absolute voltage specification always applies.
- See Table 9 for TMD5_33 specifications.
- A total of 200 mA per bank should not be exceeded.
- V_{CCBATT} is required only when using bitstream encryption. If battery is not used, connect V_{CCBATT} to either ground or V_{CCAUX} .

Table 5: Typical Quiescent Supply Current⁽¹⁾⁽²⁾⁽³⁾ (Cont'd)

Symbol	Description	Device	Speed Grade						Units
			1.0V					0.95V	
			-2C	-2I	-1C	-1I	-1Q	-1LI	
$I_{CCBRAMQ}$	Quiescent V_{CCBRAM} supply current.	XC7S6	1	1	1	1	1	1	mA
		XC7S15	1	1	1	1	1	1	mA
		XC7S25	1	1	1	1	1	1	mA
		XC7S50	2	2	2	2	2	1	mA
		XC7S75	9	9	9	9	9	8	mA
		XC7S100	9	9	9	9	9	8	mA
		XA7S6	N/A	1	N/A	1	1	N/A	mA
		XA7S15	N/A	1	N/A	1	1	N/A	mA
		XA7S25	N/A	1	N/A	1	1	N/A	mA
		XA7S50	N/A	2	N/A	2	2	N/A	mA
		XA7S75	N/A	9	N/A	9	9	N/A	mA
		XA7S100	N/A	9	N/A	9	9	N/A	mA

Notes:

- Typical values are specified at nominal voltage, 85°C junction temperature (T_j) with single-ended SelectIO™ resources.
- Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
- Use the *Xilinx Power Estimator* spreadsheet tool [Ref 6] to estimate static power consumption for conditions other than those specified.

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT} , V_{CCBRAM} , V_{CCAUX} , and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCBRAM} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If V_{CCAUX} and V_{CCO} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously.

For V_{CCO} voltages of 3.3V in HR I/O banks and configuration bank 0 the following conditions apply.

- The voltage difference between V_{CCO} and V_{CCAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

There is no recommended sequence for supplies not discussed in this section.

LVDS DC Specifications (LVDS_25)

Table 11: LVDS_25 DC Specifications⁽¹⁾

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply voltage.		2.375	2.500	2.625	V
V_{OH}	Output High voltage for Q and $\overline{Q}$.	$R_T = 100\Omega$ across Q and $\overline{Q}$ signals.	–	–	1.675	V
V_{OL}	Output Low voltage for Q and $\overline{Q}$.	$R_T = 100\Omega$ across Q and $\overline{Q}$ signals.	0.700	–	–	V
V_{ODIFF}	Differential output voltage: (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	$R_T = 100\Omega$ across Q and $\overline{Q}$ signals.	247	350	600	mV
V_{OCM}	Output common-mode voltage.	$R_T = 100\Omega$ across Q and $\overline{Q}$ signals.	1.000	1.250	1.425	V
V_{IDIFF}	Differential input voltage: (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input common-mode voltage.		0.300	1.200	1.500	V

Notes:

1. Differential inputs for LVDS_25 can be placed in banks with V_{CCO} levels that are different from the required level for outputs. Consult the *7 Series FPGAs SelectIO Resources User Guide* (UG471) [Ref 3] for more information.

Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. [Table 13](#) correlates the current status of each Spartan-7 device on a per speed grade basis.

Table 13: Spartan-7 Device Speed Grade Designations

Device	Speed Grade, Temperature Range, and V_{CCINT} Operating Voltage		
	Advance	Preliminary	Production
XC7S6			-2C (1.0V), -2I (1.0V), -1C (1.0V), -1I (1.0V), -1Q (1.0V), and -1LI (0.95V) ⁽¹⁾
XC7S15			-2C (1.0V), -2I (1.0V), -1C (1.0V), -1I (1.0V), -1Q (1.0V), and -1LI (0.95V) ⁽¹⁾
XC7S25			-2C (1.0V), -2I (1.0V), -1C (1.0V), -1I (1.0V), -1Q (1.0V), and -1LI (0.95V) ⁽¹⁾
XC7S50			-2C (1.0V), -2I (1.0V), -1C (1.0V), -1I (1.0V), -1Q (1.0V), and -1LI (0.95V) ⁽¹⁾
XC7S75			-2C (1.0V), -2I (1.0V), -1C (1.0V), -1I (1.0V), -1Q (1.0V), and -1LI (0.95V) ⁽¹⁾
XC7S100			-2C (1.0V), -2I (1.0V), -1C (1.0V), -1I (1.0V), -1Q (1.0V), and -1LI (0.95V) ⁽¹⁾
XA7S6			-2I (1.0V), -1I (1.0V), -1Q (1.0V)
XA7S15			-2I (1.0V), -1I (1.0V), -1Q (1.0V)
XA7S25			-2I (1.0V), -1I (1.0V), -1Q (1.0V)
XA7S50			-2I (1.0V), -1I (1.0V), -1Q (1.0V)
XA7S75			-2I (1.0V), -1I (1.0V), -1Q (1.0V)
XA7S100			-2I (1.0V), -1I (1.0V), -1Q (1.0V)

Notes:

1. The lowest power -1LI devices, where $V_{CCINT} = 0.95V$, are listed in the Vivado Design Suite as -1IL.

Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

[Table 14](#) lists the production released Spartan-7 device, speed grade, and the minimum corresponding supported speed specification version and software revisions. The software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 14: Spartan-7 Device Production Software and Speed Specification Release

Device	V_{CCINT} Operating Voltage, Speed Grade, and Temperature Range					
	1.0V					0.95V
	-2C	-2I	-1C	-1I	-1Q	-1LI
XC7S6	Vivado tools 2018.2 v1.22				Vivado tools 2018.2.1 v1.23	Vivado tools 2018.2 v1.22
XC7S15	Vivado tools 2018.2 v1.22				Vivado tools 2018.2.1 v1.23	Vivado tools 2018.2 v1.22
XC7S25	Vivado tools 2017.4 v1.20				Vivado tools 2018.1 v1.21	Vivado tools 2017.4 v1.20
XC7S50	Vivado tools 2017.2 v1.17				Vivado tools 2017.3 v1.19	Vivado tools 2017.2 v1.17
XC7S75	Vivado tools 2018.1 v1.21				Vivado tools 2018.2.1 v1.23	Vivado tools 2018.1 v1.21
XC7S100	Vivado tools 2018.1 v1.21				Vivado tools 2018.2.1 v1.23	Vivado tools 2018.1 v1.21
XA7S6	N/A	Vivado tools 2018.2.1 v1.16	N/A	Vivado tools 2018.2.1 v1.16		N/A
XA7S15	N/A	Vivado tools 2018.2.1 v1.16	N/A	Vivado tools 2018.2.1 v1.16		N/A
XA7S25	N/A	Vivado tools 2018.1 v1.15	N/A	Vivado tools 2018.1 v1.15		N/A
XA7S50	N/A	Vivado tools 2017.3 v1.12	N/A	Vivado tools 2017.3 v1.12		N/A
XA7S75	N/A	Vivado tools 2018.2.1 v1.16	N/A	Vivado tools 2018.2.1 v1.16		N/A
XA7S100	N/A	Vivado tools 2018.2.1 v1.16	N/A	Vivado tools 2018.2.1 v1.16		N/A

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Spartan-7 FPGAs. These values are subject to the same guidelines as the [AC Switching Characteristics, page 12](#).

Table 15: Networking Applications Interface Performances

Description	V_{CCINT} Operating Voltage, Speed Grade, and Temperature Range			Units
	1.0V		0.95V	
	-2C/-2I	-1C/-1I/-1Q	-1LI	
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	680	600	600	Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14)	1250	950	950	Mb/s
SDR LVDS receiver ⁽¹⁾	680	600	600	Mb/s

Table 17: IOB High Range (HR) Switching Characteristics (Cont'd)

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	V _{CCINT} Operating Voltage and Speed Grade									
	1.0V		0.95V	1.0V		0.95V	1.0V		0.95V	
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
LVC MOS15_F8	0.86	0.93	0.93	1.72	1.98	1.98	1.75	1.99	1.99	ns
LVC MOS15_F12	0.86	0.93	0.93	1.47	1.73	1.73	1.50	1.74	1.74	ns
LVC MOS15_F16	0.86	0.93	0.93	1.46	1.71	1.71	1.49	1.73	1.73	ns
LVC MOS12_S4	0.95	1.02	1.02	2.69	2.95	2.95	2.72	2.96	2.96	ns
LVC MOS12_S8	0.95	1.02	1.02	2.21	2.46	2.46	2.24	2.48	2.48	ns
LVC MOS12_S12	0.95	1.02	1.02	1.91	2.17	2.17	1.94	2.18	2.18	ns
LVC MOS12_F4	0.95	1.02	1.02	2.10	2.35	2.35	2.13	2.37	2.37	ns
LVC MOS12_F8	0.95	1.02	1.02	1.66	1.92	1.92	1.69	1.93	1.93	ns
LVC MOS12_F12	0.95	1.02	1.02	1.51	1.76	1.76	1.54	1.77	1.77	ns
SSTL135_S	0.75	0.82	0.82	1.47	1.73	1.73	1.50	1.74	1.74	ns
SSTL15_S	0.68	0.75	0.75	1.43	1.68	1.68	1.46	1.69	1.69	ns
SSTL18_I_S	0.75	0.82	0.82	1.79	2.04	2.04	1.82	2.06	2.06	ns
SSTL18_II_S	0.75	0.82	0.82	1.43	1.68	1.68	1.46	1.70	1.70	ns
DIFF_SSTL135_S	0.76	0.83	0.83	1.47	1.73	1.73	1.50	1.74	1.74	ns
DIFF_SSTL15_S	0.76	0.83	0.83	1.43	1.68	1.68	1.46	1.69	1.69	ns
DIFF_SSTL18_I_S	0.79	0.86	0.86	1.80	2.06	2.06	1.83	2.07	2.07	ns
DIFF_SSTL18_II_S	0.79	0.86	0.86	1.51	1.76	1.76	1.54	1.77	1.77	ns
SSTL135_F	0.75	0.82	0.82	1.24	1.49	1.49	1.27	1.51	1.51	ns
SSTL15_F	0.68	0.75	0.75	1.19	1.45	1.45	1.22	1.46	1.46	ns
SSTL18_I_F	0.75	0.82	0.82	1.24	1.49	1.49	1.27	1.51	1.51	ns
SSTL18_II_F	0.75	0.82	0.82	1.24	1.49	1.49	1.27	1.51	1.51	ns
DIFF_SSTL135_F	0.76	0.83	0.83	1.24	1.49	1.49	1.27	1.51	1.51	ns
DIFF_SSTL15_F	0.76	0.83	0.83	1.19	1.45	1.45	1.22	1.46	1.46	ns
DIFF_SSTL18_I_F	0.79	0.86	0.86	1.35	1.60	1.60	1.38	1.62	1.62	ns
DIFF_SSTL18_II_F	0.79	0.86	0.86	1.33	1.59	1.59	1.36	1.60	1.60	ns

Table 18 specifies the values of T_{IOTPHZ} and $T_{IOIBUFDISABLE}$. T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). $T_{IOIBUFDISABLE}$ is described as the IOB delay from IBUFDISABLE to O output. In HR I/O banks, the internal IN_TERM termination turn-off time is always faster than T_{IOTPHZ} when the INTERMDISABLE pin is used.

I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

Table 19 shows the test setup parameters used for measuring input delay.

Table 19: Input Delay Measurement Methodology

Description	I/O Standard Attribute	$V_L^{(1)}$	$V_H^{(1)}$	$V_{MEAS}^{(3)(5)}$	$V_{REF}^{(2)(4)}$
LVCMOS, 1.2V	LVCMOS12	0.1	1.1	0.6	—
LVCMOS, 1.5V	LVCMOS15	0.1	1.4	0.75	—
LVCMOS, 1.8V	LVCMOS18	0.1	1.7	0.9	—
LVCMOS, 2.5V	LVCMOS25	0.1	2.4	1.25	—
LVCMOS, 3.3V	LVCMOS33	0.1	3.2	1.65	—
LVTTL, 3.3V	LVTTL	0.1	3.2	1.65	—
MOBILE_DDR, 1.8V	MOBILE_DDR	0.1	1.7	0.9	—
PCI33, 3.3V	PCI33_3	0.1	3.2	1.65	—
HSTL (high-speed transceiver logic), Class I, 1.2V	HSTL_I_12	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.60
HSTL, Class I & II, 1.5V	HSTL_I, HSTL_II	$V_{REF} - 0.65$	$V_{REF} + 0.65$	V_{REF}	0.75
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	$V_{REF} - 0.8$	$V_{REF} + 0.8$	V_{REF}	0.90
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.60
SSTL (stub-terminated transceiver logic), 1.2V	SSTL12	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.60
SSTL, 1.35V	SSTL135, SSTL135_R	$V_{REF} - 0.575$	$V_{REF} + 0.575$	V_{REF}	0.675
SSTL, 1.5V	SSTL15, SSTL15_R	$V_{REF} - 0.65$	$V_{REF} + 0.65$	V_{REF}	0.75
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	$V_{REF} - 0.8$	$V_{REF} + 0.8$	V_{REF}	0.90
DIFF_MOBILE_DDR, 1.8V	DIFF_MOBILE_DDR	$0.9 - 0.125$	$0.9 + 0.125$	$0^{(5)}$	—
DIFF_HSTL, Class I, 1.2V	DIFF_HSTL_I_12	$0.6 - 0.125$	$0.6 + 0.125$	$0^{(5)}$	—
DIFF_HSTL, Class I & II, 1.5V	DIFF_HSTL_I, DIFF_HSTL_II	$0.75 - 0.125$	$0.75 + 0.125$	$0^{(5)}$	—
DIFF_HSTL, Class I & II, 1.8V	DIFF_HSTL_I_18, DIFF_HSTL_II_18	$0.9 - 0.125$	$0.9 + 0.125$	$0^{(5)}$	—
DIFF_HSUL, 1.2V	DIFF_HSUL_12	$0.6 - 0.125$	$0.6 + 0.125$	$0^{(5)}$	—
DIFF_SSTL135/ DIFF_SSTL135_R, 1.35V	DIFF_SSTL135, DIFF_SSTL135_R	$0.675 - 0.125$	$0.675 + 0.125$	$0^{(5)}$	—
DIFF_SSTL15/ DIFF_SSTL15_R, 1.5V	DIFF_SSTL15, DIFF_SSTL15_R	$0.75 - 0.125$	$0.75 + 0.125$	$0^{(5)}$	—
DIFF_SSTL18_I/ DIFF_SSTL18_II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	$0.9 - 0.125$	$0.9 + 0.125$	$0^{(5)}$	—
LVDS_25, 2.5V	LVDS_25	$1.2 - 0.125$	$1.2 + 0.125$	$0^{(5)}$	—
BLVDS_25, 2.5V	BLVDS_25	$1.25 - 0.125$	$1.25 + 0.125$	$0^{(5)}$	—
MINI_LVDS_25, 2.5V	MINI_LVDS_25	$1.25 - 0.125$	$1.25 + 0.125$	$0^{(5)}$	—

Table 19: Input Delay Measurement Methodology (Cont'd)

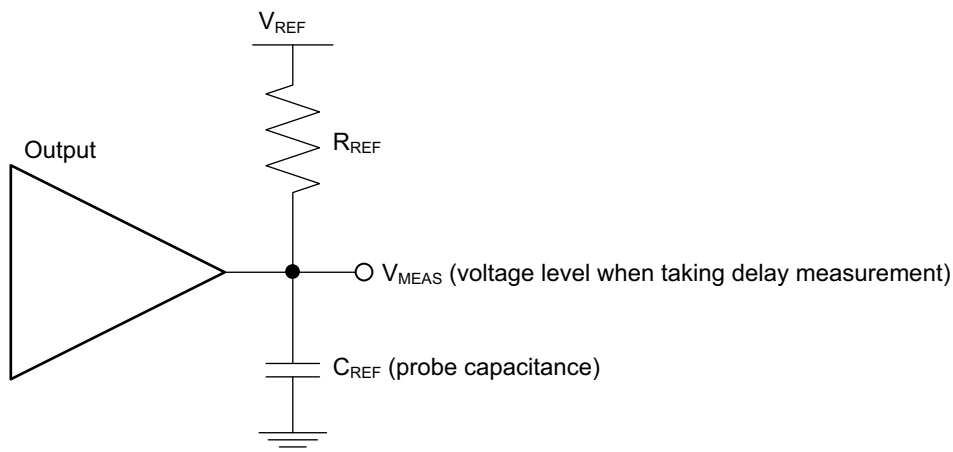
Description	I/O Standard Attribute	$V_L^{(1)}$	$V_H^{(1)}$	$V_{MEAS}^{(3)(5)}$	$V_{REF}^{(2)(4)}$
PPDS_25	PPDS_25	1.25 – 0.125	1.25 + 0.125	0 ⁽⁵⁾	–
RSDS_25	RSDS_25	1.25 – 0.125	1.25 + 0.125	0 ⁽⁵⁾	–
TMDS_33	TMDS_33	3 – 0.125	3 + 0.125	0 ⁽⁵⁾	–

Notes:

1. Input waveform switches between V_L and V_H .
2. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
3. Input voltage level from which measurement starts.
4. This is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in [Figure 1](#).
5. The value given is the differential input voltage.

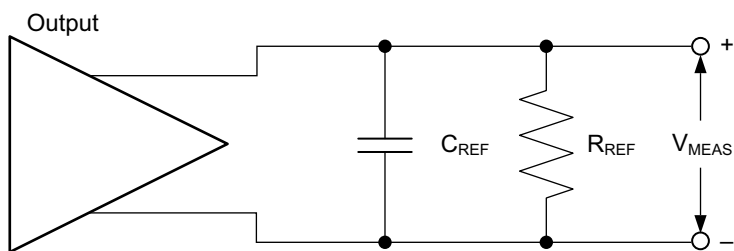
Output Delay Measurements

Output delays are measured with short output traces. Standard termination was used for all testing. The propagation delay of the trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in [Figure 1](#) and [Figure 2](#).



X16654-092616

Figure 1: Single-ended Test Setup



X16640-092616

Figure 2: Differential Test Setup

Parameters V_{REF} , R_{REF} , C_{REF} , and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using this method:

1. Simulate the output driver of choice into the generalized test setup using values from [Table 20](#).
2. Record the time to V_{MEAS} .
3. Simulate the output driver of choice into the actual PCB trace and load using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS} .
5. Compare the results of [step 2](#) and [step 4](#). The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 20: Output Delay Measurement Methodology

Description	I/O Standard Attribute	R _{REF} (Ω)	C _{REF} ⁽¹⁾ (pF)	V _{MEAS} (V)	V _{REF} (V)
LVC MOS, 1.2V	LVC MOS12	1M	0	0.6	0
LVC MOS, 1.5V	LVC MOS15	1M	0	0.75	0
LVC MOS, 1.8V	LVC MOS18	1M	0	0.9	0
LVC MOS, 2.5V	LVC MOS25	1M	0	1.25	0
LVC MOS, 3.3V	LVC MOS33	1M	0	1.65	0
LVTTL, 3.3V	LVTTL	1M	0	1.65	0
PCI33, 3.3V	PCI33_3	25	10	1.65	0
HSTL (high-speed transceiver logic), Class I, 1.2V	HSTL_I_12	50	0	V _{REF}	0.6
HSTL, Class I, 1.5V	HSTL_I	50	0	V _{REF}	0.75
HSTL, Class II, 1.5V	HSTL_II	25	0	V _{REF}	0.75
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V _{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V _{REF}	0.9
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	50	0	V _{REF}	0.6
SSTL12, 1.2V	SSTL12	50	0	V _{REF}	0.6
SSTL135/SSTL135_R, 1.35V	SSTL135, SSTL135_R	50	0	V _{REF}	0.675
SSTL15/SSTL15_R, 1.5V	SSTL15, SSTL15_R	50	0	V _{REF}	0.75
SSTL (stub-series terminated logic), Class I & Class II, 1.8V	SSTL18_I, SSTL18_II	50	0	V _{REF}	0.9
DIFF_MOBILE_DDR, 1.8V	DIFF_MOBILE_DDR	50	0	V _{REF}	0.9
DIFF_HSTL, Class I, 1.2V	DIFF_HSTL_I_12	50	0	V _{REF}	0.6
DIFF_HSTL, Class I & II, 1.5V	DIFF_HSTL_I, DIFF_HSTL_II	50	0	V _{REF}	0.75
DIFF_HSTL, Class I & II, 1.8V	DIFF_HSTL_I_18, DIFF_HSTL_II_18	50	0	V _{REF}	0.9
DIFF_HSUL_12, 1.2V	DIFF_HSUL_12	50	0	V _{REF}	0.6
DIFF_SSTL135/DIFF_SSTL135_R, 1.35V	DIFF_SSTL135, DIFF_SSTL135_R	50	0	V _{REF}	0.675
DIFF_SSTL15/DIFF_SSTL15_R, 1.5V	DIFF_SSTL15, DIFF_SSTL15_R	50	0	V _{REF}	0.75
DIFF_SSTL18, Class I & II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	50	0	V _{REF}	0.9
LVDS, 2.5V	LVDS_25	100	0	0 ⁽²⁾	0
BLVDS (Bus LVDS), 2.5V	BLVDS_25	100	0	0 ⁽²⁾	0
Mini LVDS, 2.5V	MINI_LVDS_25	100	0	0 ⁽²⁾	0
PPDS_25	PPDS_25	100	0	0 ⁽²⁾	0
RS DS_25	RS DS_25	100	0	0 ⁽²⁾	0
TMDS_33	TMDS_33	50	0	0 ⁽²⁾	3.3

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Input/Output Delay Switching Characteristics

Table 25: Input/Output Delay Switching Characteristics

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
IDELAYCTRL					
T _{DLYCCO_RDY}	Reset to ready for IDELAYCTRL.	3.67	3.67	3.67	μs
F _{IDELAYCTRL_REF}	Attribute REFCLK frequency = 200.00. ⁽¹⁾	200.00	200.00	200.00	MHz
	Attribute REFCLK frequency = 300.00. ⁽¹⁾	300.00	300.00	300.00	MHz
	Attribute REFCLK frequency = 400.00. ⁽¹⁾	400.00	N/A	N/A	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	±10	MHz
T _{IDELAYCTRL_RPW}	Minimum reset pulse width.	59.28	59.28	59.28	ns
IDELAY					
T _{IDELAYRESOLUTION}	IDELAY chain delay resolution.	1/(32 x 2 x F _{REF})			μs
T _{IDELAYPAT_JIT}	Pattern dependent period jitter in delay chain for clock pattern. ⁽²⁾	0	0	0	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23). ⁽³⁾	±5	±5	±5	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23). ⁽⁴⁾	±9	±9	±9	ps per tap
T _{IDELAY_CLK_MAX}	Maximum frequency of CLK input to IDELAY.	680.00	600.00	600.00	MHz
T _{IDCCK_CE} / T _{IDCKC_CE}	CE pin setup/hold with respect to C for IDELAY.	0.16/0.13	0.21/0.16	0.21/0.16	ns
T _{IDCCK_INC} /T _{IDCKC_INC}	INC pin setup/hold with respect to C for IDELAY.	0.14/0.18	0.16/0.22	0.16/0.22	ns
T _{IDCCK_RST} /T _{IDCKC_RST}	RST pin setup/hold with respect to C for IDELAY.	0.16/0.11	0.18/0.14	0.18/0.14	ns
T _{IDDO_IDATAIN}	Propagation delay through IDELAY.	Note 5	Note 5	Note 5	ps

Notes:

1. Average tap delay at 200 MHz = 78 ps, at 300 MHz = 52 ps, and at 400 MHz = 39 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE.
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY tap setting. See the timing report for actual values.

Table 26: IO_FIFO Switching Characteristics

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
IO_FIFO Clock to Out Delays					
T _{OFFCKO_DO}	RDCLK to Q outputs.	0.60	0.68	0.68	ns
T _{CKO_FLAGS}	Clock to IO_FIFO flags.	0.61	0.77	0.77	ns
Setup/Hold					
T _{CCK_D} /T _{CKC_D}	D inputs to WRCLK.	0.51/0.02	0.58/0.02	0.58/0.02	ns
T _{IFFCCK_WREN} / T _{IFFCKC_WREN}	WREN to WRCLK.	0.47/−0.01	0.53/−0.01	0.53/−0.01	ns
T _{OFFCCK_RDEN} / T _{OFFCKC_RDEN}	RDEN to RDCLK.	0.58/0.02	0.66/0.02	0.66/0.02	ns
Minimum Pulse Width					
T _{PWH_IO_FIFO}	RESET, RDCLK, WRCLK.	2.15	2.15	2.15	ns
T _{PWL_IO_FIFO}	RESET, RDCLK, WRCLK.	2.15	2.15	2.15	ns
Maximum Frequency					
F _{MAX}	RDCLK and WRCLK.	200.00	200.00	200.00	MHz

Table 31: DSP48E1 Switching Characteristics (Cont'd)

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
T _{DSPDO_PCIN_CARRYCASCOUT}	PCIN input to CARRYCASCOUT output.	1.56	1.85	1.85	ns
Clock to Outs from Output Register Clock to Output Pins					
T _{DSPCKO_P_PREG}	CLK PREG to P output.	0.37	0.44	0.44	ns
T _{DSPCKO_CARRYCASCOUT_PREG}	CLK PREG to CARRYCASCOUT output.	0.59	0.69	0.69	ns
Clock to Outs from Pipeline Register Clock to Output Pins					
T _{DSPCKO_P_MREG}	CLK MREG to P output.	1.93	2.31	2.31	ns
T _{DSPCKO_CARRYCASCOUT_MREG}	CLK MREG to CARRYCASCOUT output.	2.21	2.64	2.64	ns
T _{DSPCKO_P_ADREG_MULT}	CLK ADREG to P output using multiplier.	3.10	3.69	3.69	ns
T _{DSPCKO_CARRYCASCOUT_ADREG_MULT}	CLK ADREG to CARRYCASCOUT output using multiplier.	3.38	4.02	4.02	ns
Clock to Outs from Input Register Clock to Output Pins					
T _{DSPCKO_P_AREG_MULT}	CLK AREG to P output using multiplier.	4.51	5.37	5.37	ns
T _{DSPCKO_P_BREG}	CLK BREG to P output not using multiplier.	1.87	2.22	2.22	ns
T _{DSPCKO_P_CREG}	CLK CREG to P output not using multiplier.	1.93	2.30	2.30	ns
T _{DSPCKO_P_DREG_MULT}	CLK DREG to P output using multiplier.	4.48	5.32	5.32	ns
Clock to Outs from Input Register Clock to Cascading Output Pins					
T _{DSPCKO_{ACOUT; BCOUT}_{AREG; BREG}}	CLK (ACOUT, BCOUT) to {A,B} register output.	0.73	0.87	0.87	ns
T _{DSPCKO_CARRYCASCOUT_{AREG; BREG}_MULT}	CLK (AREG, BREG) to CARRYCASCOUT output using multiplier.	4.79	5.70	5.70	ns
T _{DSPCKO_CARRYCASCOUT_BREG}	CLK BREG to CARRYCASCOUT output not using multiplier.	2.15	2.55	2.55	ns
T _{DSPCKO_CARRYCASCOUT_DREG_MULT}	CLK DREG to CARRYCASCOUT output using multiplier.	4.76	5.65	5.65	ns
T _{DSPCKO_CARRYCASCOUT_CREG}	CLK CREG to CARRYCASCOUT output.	2.21	2.63	2.63	ns
Maximum Frequency					
F _{MAX}	With all registers used.	550.66	464.25	464.25	MHz
F _{MAX_PATDET}	With pattern detector.	465.77	392.93	392.93	MHz
F _{MAX_MULT_NOMREG}	Two register multiply without MREG.	305.62	257.47	257.47	MHz
F _{MAX_MULT_NOMREG_PATDET}	Two register multiply without MREG with pattern detect.	277.62	233.92	233.92	MHz
F _{MAX_PREADD_MULT_NOADREG}	Without ADREG.	346.26	290.44	290.44	MHz
F _{MAX_PREADD_MULT_NOADREG_PATDET}	Without ADREG with pattern detect.	346.26	290.44	290.44	MHz
F _{MAX_NOPIPELINEREG}	Without pipeline registers (MREG, ADREG).	227.01	190.69	190.69	MHz
F _{MAX_NOPIPELINEREG_PATDET}	Without pipeline registers (MREG, ADREG) with pattern detect.	211.15	177.43	177.43	MHz

Table 38: PLL Specification

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
PLL_F _{BANDWIDTH}	Low PLL bandwidth at typical.	1.00	1.00	1.00	MHz
	High PLL bandwidth at typical. ⁽¹⁾	4.00	4.00	4.00	MHz
PLL_T _{STATPHAOFFSET}	Static phase offset of the PLL outputs. ⁽²⁾	0.12	0.12	0.12	ns
PLL_T _{OUTJITTER}	PLL output jitter.	Note 3			
PLL_T _{OUTDUTY}	PLL output clock duty-cycle precision. ⁽⁴⁾	0.20	0.20	0.20	ns
PLL_T _{LOCKMAX}	PLL maximum lock time.	100.00	100.00	100.00	μs
PLL_F _{OUTMAX}	PLL maximum output frequency.	800.00	800.00	800.00	MHz
PLL_F _{OUTMIN}	PLL minimum output frequency. ⁽⁵⁾	6.25	6.25	6.25	MHz
PLL_T _{EXTFDVAR}	External clock feedback variation.	< 20% of clock input period or 1 ns Max			
PLL_RST _{MINPULSE}	Minimum reset pulse width.	5.00	5.00	5.00	ns
PLL_F _{PFDMAX}	Maximum frequency at the phase frequency detector.	500.00	450.00	450.00	MHz
PLL_F _{PFDMIN}	Minimum frequency at the phase frequency detector.	19.00	19.00	19.00	MHz
PLL_T _{FBDELAY}	Maximum delay in the feedback path.	3 ns Max or one CLKIN cycle			
Dynamic Reconfiguration Port (DRP) for PLL Before and After DCLK					
T _{PLLDCK_DADDR} / T _{PLLCKD_DADDR}	Setup and hold of D address.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
T _{PLLDCK_DI} / T _{PLLCKD_DI}	Setup and hold of D input.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
T _{PLLDCK_DEN} / T _{PLLCKD_DEN}	Setup and hold of D enable.	1.97/0.00	2.29/0.00	2.29/0.00	ns, Min
T _{PLLDCK_DWE} / T _{PLLCKD_DWE}	Setup and hold of D write enable.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
T _{PLLCKO_DRDY}	CLK to out of DRDY.	0.72	0.99	0.99	ns, Max
F _{DCK}	DCLK frequency.	200.00	200.00	200.00	MHz, Max

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the *Clocking Wizard* [Ref 8].
4. Includes global clock buffer.
5. Calculated as FVCO/128 assuming output duty cycle is 50%.

Table 40: Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Far Clock Region)⁽¹⁾

Symbol	Description	Device	V _{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM/PLL.						
T _{ICKOFFAR}	Clock-capable clock input and OUTFF at pins/banks farthest from the BUFGs <i>without</i> MMCM/PLL (far clock region). ⁽²⁾	XC7S6	5.55	6.50	6.50	ns
		XC7S15	5.55	6.50	6.50	ns
		XC7S25	5.55	6.44	6.44	ns
		XC7S50	5.71	6.62	6.62	ns
		XC7S75	6.01	7.02	7.02	ns
		XC7S100	6.01	7.02	7.02	ns
		XA7S6	5.55	6.50	N/A	ns
		XA7S15	5.55	6.50	N/A	ns
		XA7S25	5.55	6.44	N/A	ns
		XA7S50	5.71	6.62	N/A	ns
		XA7S75	6.01	7.02	N/A	ns
		XA7S100	6.01	7.02	N/A	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Refer to the *Die Level Bank Numbering Overview* section of the *7 Series FPGA Packaging and Pinout Specification* (UG475) [Ref 4].

Table 41: Clock-Capable Clock Input to Output Delay With MMCM⁽¹⁾

Symbol	Description	Device	V _{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>with</i> MMCM.						
T _{ICKOFMMCMCC}	Clock-capable clock input and OUTFF <i>with</i> MMCM. ⁽²⁾	XC7S6	1.03	1.03	1.03	ns
		XC7S15	1.03	1.03	1.03	ns
		XC7S25	1.00	1.00	1.00	ns
		XC7S50	1.00	1.00	1.00	ns
		XC7S75	1.00	1.00	1.00	ns
		XC7S100	1.00	1.00	1.00	ns
		XA7S6	1.03	1.03	N/A	ns
		XA7S15	1.03	1.03	N/A	ns
		XA7S25	1.00	1.00	N/A	ns
		XA7S50	1.00	1.00	N/A	ns
		XA7S75	1.00	1.00	N/A	ns
		XA7S100	1.00	1.00	N/A	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 42: Clock-Capable Clock Input to Output Delay With PLL⁽¹⁾

Symbol	Description	Device	V _{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>with</i> PLL.						
T _{ICKOFFLLCC}	Clock-capable clock input and OUTFF <i>with</i> PLL. ⁽²⁾	XC7S6	0.85	0.85	0.85	ns
		XC7S15	0.85	0.85	0.85	ns
		XC7S25	0.83	0.83	0.83	ns
		XC7S50	0.83	0.83	0.83	ns
		XC7S75	0.83	0.83	0.83	ns
		XC7S100	0.83	0.83	0.83	ns
		XA7S6	0.85	0.85	N/A	ns
		XA7S15	0.85	0.85	N/A	ns
		XA7S25	0.83	0.83	N/A	ns
		XA7S50	0.83	0.83	N/A	ns
		XA7S75	0.83	0.83	N/A	ns
		XA7S100	0.83	0.83	N/A	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is already included in the timing calculation.

Table 43: Pin-to-Pin, Clock-to-Out using BUFIO

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with BUFIO.					
T _{ICKOFCS}	Clock to out of I/O clock.	5.61	6.64	6.64	ns

Table 46: Clock-Capable Clock Input Setup and Hold With PLL

Symbol	Description	Device	V _{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard. ⁽¹⁾⁽²⁾						
T _{PSPLLCC} / T _{PHPLLCC}	No delay clock-capable clock input and IFF ⁽³⁾ with PLL.	XC7S6	3.07/−0.17	3.69/−0.17	3.69/−0.17	ns
		XC7S15	3.07/−0.17	3.69/−0.17	3.69/−0.17	ns
		XC7S25	3.04/−0.19	3.64/−0.19	3.64/−0.19	ns
		XC7S50	3.15/−0.19	3.77/−0.19	3.77/−0.19	ns
		XC7S75	3.15/−0.19	3.78/−0.19	3.78/−0.19	ns
		XC7S100	3.15/−0.19	3.78/−0.19	3.78/−0.19	ns
		XA7S6	3.07/−0.17	3.69/−0.17	N/A	ns
		XA7S15	3.07/−0.17	3.69/−0.17	N/A	ns
		XA7S25	3.04/−0.19	3.64/−0.19	N/A	ns
		XA7S50	3.15/−0.19	3.77/−0.19	N/A	ns
		XA7S75	3.15/−0.19	3.78/−0.19	N/A	ns
		XA7S100	3.15/−0.19	3.78/−0.19	N/A	ns

Notes:

- Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
- Use IBIS to determine any duty-cycle distortion incurred using various standards.
- IFF = Input flip-flop or latch.

Table 47: Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Input Setup and Hold Time Relative to a Forwarded Clock Input Pin Using BUFIO for SSTL15 Standard.					
T _{PSCS} /T _{PHCS}	Setup and hold of I/O clock.	−0.38/1.46	−0.38/1.73	−0.38/1.76	ns

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
07/31/2018	1.7	In Table 12 , updated Vivado tools version to 2018.2.1. In Table 13 , moved all speed grades for all devices to Production. In Table 14 , added Vivado tools version for XC7S6, XC7S15, XC7S75, XC7S100, XA7S6, XA7S15, XA7S75, and XA7S100.
06/18/2018	1.6	In Table 12 , updated Vivado tools version to 2018.2. In Table 13 , moved all speed grades except -1Q (1.0V) for XC7S6 and XC7S15 to Production. In Table 14 , added Vivado tools version for XC7S6 and XC7S15.
04/04/2018	1.5	Added XA7S6, XA7S15, XA7S25, XA7S75, and XA7S100 devices throughout. In Table 5 , updated typical quiescent supply current values for XC7S25 and XC7S50 devices, and added values for XC7S6, XC7S15, XC7S75, and XC7S100 devices. In Table 6 , updated table title and $I_{CCINTMIN}$ and $I_{CCAUXMIN}$ for XC7S75 and XC7S100 devices. In Table 13 , moved all speed grades for XC7S6 and XC7S15 to Preliminary, moved -1LI (0.95V) speed grade for XC7S25 to Production, and moved all speed grades except -1Q (1.0V) for XC7S75 and XC7S100 from Preliminary to Production. In Table 14 , added Vivado tools version for XC7S25, XC7S75, and XC7S100. In Table 36 , Table 39 , Table 40 , Table 41 , Table 42 , Table 44 , Table 45 , and Table 46 , changed parameter value for XA7S50 to N/A. In Table 49 , added package skew values for XC7S6 and XC7S15 devices.
12/22/2017	1.4	In Table 12 , updated Vivado tools version to 2017.4. In Table 13 , moved all speed grades for XC7S75 and XC7S100 from Advance to Preliminary and all speed grades except -1LI (0.95V) for XC7S25 from Advance to Production. In Table 14 , added Vivado tools version for XC7S25. Added Note 2 to Table 16 . In Table 49 , added package skew values for XC7S25 device in CSGA324 package and XC7S75 and XC7S100 devices in FGGA676 package.
11/20/2017	1.3	Added XA7S50 device throughout. Updated description of offered temperature ranges in second paragraph of Introduction . Added row for junction temperature (T_j) at expanded (Q) temperature to Table 2 . Added -1Q (1.0V) speed grade to Table 5 , and Table 13 to Table 16 . In Table 12 , updated Vivado tools version to 2017.3. In Table 49 , added package skew values for XC7S25, XC7S50, XC7S75, and XC7S100 devices in CSGA225, FTGB196, and FGGA484 packages. Added <i>XA Spartan-7 Automotive FPGA Data Sheet: Overview (DS171)</i> to References .
06/20/2017	1.2	Updated paragraph before Table 6 . In Table 12 , updated Vivado tools version to 2017.2. In Table 13 , moved all speed grades for XC7S50 from Preliminary to Production and updated Note 1 . In Table 14 , added Vivado tools version for XC7S50. In Table 49 , added package skew value for XC7S50 device in FGGA484 package.
04/07/2017	1.1	Added 1.35V to Note 5 in Table 2 . In Table 12 , updated Vivado tools version to 2016.4. In Table 13 , moved all speed grades for XC7S50 from Advance to Preliminary. Removed SFI-4.1 and SPI-4.2 from descriptions of SDR LVDS receiver and DDR LVDS receiver, respectively, in Table 15 . In Table 25 , changed $T_{IDELAYRESOLUTION}$ units from ps to μ s. Removed BUFMR from Note 1 in Table 34 . In Table 49 , replaced TQGA144 with FTGB196 for XC7S6, XC7S15, and XC7S25 devices, added FTGB196 package for XC7S50 device, and added package skew value for XC7S50 device in CSGA324 package.
09/27/2016	1.0	Initial Xilinx release.