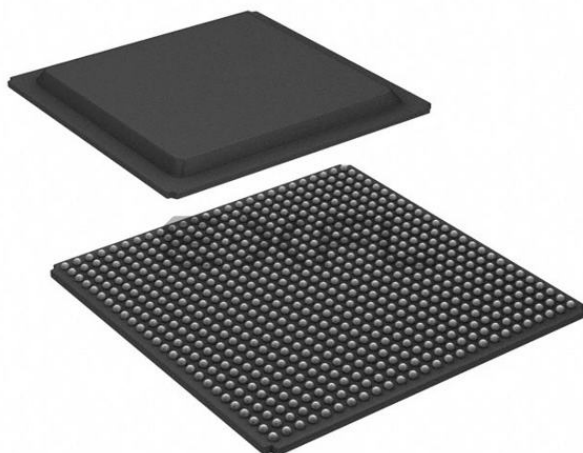




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	6000
Number of Logic Elements/Cells	76800
Total RAM Bits	4331520
Number of I/O	400
Number of Gates	-
Voltage - Supply	0.92V ~ 0.98V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FPBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc7s75-l1fgga676i

Table 2: Recommended Operating Conditions⁽¹⁾⁽²⁾

Symbol	Description	Min	Typ	Max	Units
FPGA Logic					
$V_{CCINT}^{(3)}$	For -2 and -1 (1.0V) devices: internal supply voltage.	0.95	1.00	1.05	V
	For -1L (0.95V) devices: internal supply voltage.	0.92	0.95	0.98	V
V_{CCAUX}	Auxiliary supply voltage.	1.71	1.80	1.89	V
$V_{CCBRAM}^{(3)}$	For -2 and -1 (1.0V) devices: block RAM supply voltage.	0.95	1.00	1.05	V
	For -1L (0.95V) devices: block RAM supply voltage.	0.92	0.95	0.98	V
$V_{CCO}^{(4)(5)}$	Supply voltage for HR I/O banks.	1.14	–	3.465	V
$V_{IN}^{(6)}$	I/O input voltage.	–0.20	–	$V_{CCO} + 0.20$	V
	I/O input voltage (when $V_{CCO} = 3.3V$) for V_{REF} and differential I/O standards except TMD5_33. ⁽⁷⁾	–0.20	–	2.625	V
$I_{IN}^{(8)}$	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	–	–	10	mA
$V_{CCBATT}^{(9)}$	Battery voltage.	1.0	–	1.89	V
XADC					
V_{CCADC}	XADC supply relative to GNDADC.	1.71	1.80	1.89	V
V_{REFP}	Externally supplied reference voltage.	1.20	1.25	1.30	V
Temperature					
T_j	Junction temperature operating range for commercial (C) temperature devices.	0	–	85	°C
	Junction temperature operating range for industrial (I) temperature devices.	–40	–	100	°C
	Junction temperature operating range for expanded (Q) temperature devices.	–40	–	125	°C

Notes:

- All voltages are relative to ground.
- For the design of the power distribution system consult the *7 Series FPGAs PCB Design Guide* (UG483) [Ref 5].
- If V_{CCINT} and V_{CCBRAM} are operating at the same voltage, V_{CCINT} and V_{CCBRAM} should be connected to the same supply.
- Configuration data is retained even if V_{CCO} drops to 0V.
- Includes V_{CCO} of 1.2V, 1.35V, 1.5V, 1.8V, 2.5V, and 3.3V at $\pm 5\%$.
- The lower absolute voltage specification always applies.
- See Table 9 for TMD5_33 specifications.
- A total of 200 mA per bank should not be exceeded.
- V_{CCBATT} is required only when using bitstream encryption. If battery is not used, connect V_{CCBATT} to either ground or V_{CCAUX} .

Table 4: V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for HR I/O Banks⁽¹⁾⁽²⁾

AC Voltage Overshoot	% of UI at –40°C to 125°C	AC Voltage Undershoot	% of UI at –40°C to 125°C
$V_{CCO} + 0.55$	100	–0.40	100
		–0.45	61.7
		–0.50	25.8
		–0.55	11.0
$V_{CCO} + 0.60$	46.6	–0.60	4.77
$V_{CCO} + 0.65$	21.2	–0.65	2.10
$V_{CCO} + 0.70$	9.75	–0.70	0.94
$V_{CCO} + 0.75$	4.55	–0.75	0.43
$V_{CCO} + 0.80$	2.15	–0.80	0.20
$V_{CCO} + 0.85$	1.02	–0.85	0.09
$V_{CCO} + 0.90$	0.49	–0.90	0.04
$V_{CCO} + 0.95$	0.24	–0.95	0.02

Notes:

1. A total of 200 mA per bank should not be exceeded.
2. The peak voltage of the overshoot or undershoot, and the duration above $V_{CCO} + 0.20V$ or below $GND - 0.20V$, must not exceed the values in this table.

Table 5: Typical Quiescent Supply Current⁽¹⁾⁽²⁾⁽³⁾

Symbol	Description	Device	Speed Grade						Units
			1.0V					0.95V	
			-2C	-2I	-1C	-1I	-1Q	-1LI	
I_{CCINTQ}	Quiescent V_{CCINT} supply current.	XC7S6	36	36	36	36	36	32	mA
		XC7S15	36	36	36	36	36	32	mA
		XC7S25	48	48	48	48	48	43	mA
		XC7S50	95	95	95	95	95	59	mA
		XC7S75	148	148	148	148	148	134	mA
		XC7S100	148	148	148	148	148	134	mA
		XA7S6	N/A	36	N/A	36	36	N/A	mA
		XA7S15	N/A	36	N/A	36	36	N/A	mA
		XA7S25	N/A	48	N/A	48	48	N/A	mA
		XA7S50	N/A	95	N/A	95	95	N/A	mA
		XA7S75	N/A	148	N/A	148	148	N/A	mA
		XA7S100	N/A	148	N/A	148	148	N/A	mA

Table 5: Typical Quiescent Supply Current⁽¹⁾⁽²⁾⁽³⁾ (Cont'd)

Symbol	Description	Device	Speed Grade						Units
			1.0V					0.95V	
			-2C	-2I	-1C	-1I	-1Q	-1LI	
I_{CCOQ}	Quiescent V_{CCO} supply current.	XC7S6	1	1	1	1	1	1	mA
		XC7S15	1	1	1	1	1	1	mA
		XC7S25	1	1	1	1	1	1	mA
		XC7S50	1	1	1	1	1	1	mA
		XC7S75	4	4	4	4	4	4	mA
		XC7S100	4	4	4	4	4	4	mA
		XA7S6	N/A	1	N/A	1	1	N/A	mA
		XA7S15	N/A	1	N/A	1	1	N/A	mA
		XA7S25	N/A	1	N/A	1	1	N/A	mA
		XA7S50	N/A	1	N/A	1	1	N/A	mA
		XA7S75	N/A	4	N/A	4	4	N/A	mA
		XA7S100	N/A	4	N/A	4	4	N/A	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current.	XC7S6	10	10	10	10	10	10	mA
		XC7S15	10	10	10	10	10	10	mA
		XC7S25	13	13	13	13	13	13	mA
		XC7S50	22	22	22	22	22	20	mA
		XC7S75	43	43	43	43	43	43	mA
		XC7S100	43	43	43	43	43	43	mA
		XA7S6	N/A	10	N/A	10	10	N/A	mA
		XA7S15	N/A	10	N/A	10	10	N/A	mA
		XA7S25	N/A	13	N/A	13	13	N/A	mA
		XA7S50	N/A	22	N/A	22	22	N/A	mA
		XA7S75	N/A	43	N/A	43	43	N/A	mA
		XA7S100	N/A	43	N/A	43	43	N/A	mA

Table 9: Differential SelectIO DC Input and Output Levels

I/O Standard	$V_{ICM}^{(1)}$			$V_{ID}^{(2)}$			$V_{OCM}^{(3)}$			$V_{OD}^{(4)}$		
	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max
BLVDS_25	0.300	1.200	1.425	0.100	—	—	—	1.250	—	Note 5		
MINI_LVDS_25	0.300	1.200	V_{CCAUX}	0.200	0.400	0.600	1.000	1.200	1.400	0.300	0.450	0.600
PPDS_25	0.200	0.900	V_{CCAUX}	0.100	0.250	0.400	0.500	0.950	1.400	0.100	0.250	0.400
RSDS_25	0.300	0.900	1.500	0.100	0.350	0.600	1.000	1.200	1.400	0.100	0.350	0.600
TMDS_33	2.700	2.965	3.230	0.150	0.675	1.200	$V_{CCO} - 0.405$	$V_{CCO} - 0.300$	$V_{CCO} - 0.190$	0.400	0.600	0.800

Notes:

- V_{ICM} is the input common mode voltage.
- V_{ID} is the input differential voltage ($Q - \overline{Q}$).
- V_{OCM} is the output common mode voltage.
- V_{OD} is the output differential voltage ($Q - \overline{Q}$).
- V_{OD} for BLVDS will vary significantly depending on topology and loading.

Table 10: Complementary Differential SelectIO DC Input and Output Levels

I/O Standard	$V_{ICM}^{(1)}$			$V_{ID}^{(2)}$		$V_{OL}^{(3)}$	$V_{OH}^{(4)}$	I_{OL}	I_{OH}
	V, Min	V, Typ	V, Max	V, Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
DIFF_HSTL_I	0.300	0.750	1.125	0.100	—	0.400	$V_{CCO} - 0.400$	8.00	–8.00
DIFF_HSTL_I_18	0.300	0.900	1.425	0.100	—	0.400	$V_{CCO} - 0.400$	8.00	–8.00
DIFF_HSTL_II	0.300	0.750	1.125	0.100	—	0.400	$V_{CCO} - 0.400$	16.00	–16.00
DIFF_HSTL_II_18	0.300	0.900	1.425	0.100	—	0.400	$V_{CCO} - 0.400$	16.00	–16.00
DIFF_HSUL_12	0.300	0.600	0.850	0.100	—	20% V_{CCO}	80% V_{CCO}	0.100	–0.100
DIFF_MOBILE_DDR	0.300	0.900	1.425	0.100	—	10% V_{CCO}	90% V_{CCO}	0.100	–0.100
DIFF_SSTL135	0.300	0.675	1.000	0.100	—	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	13.0	–13.0
DIFF_SSTL135_R	0.300	0.675	1.000	0.100	—	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	8.9	–8.9
DIFF_SSTL15	0.300	0.750	1.125	0.100	—	$(V_{CCO}/2) - 0.175$	$(V_{CCO}/2) + 0.175$	13.0	–13.0
DIFF_SSTL15_R	0.300	0.750	1.125	0.100	—	$(V_{CCO}/2) - 0.175$	$(V_{CCO}/2) + 0.175$	8.9	–8.9
DIFF_SSTL18_I	0.300	0.900	1.425	0.100	—	$(V_{CCO}/2) - 0.470$	$(V_{CCO}/2) + 0.470$	8.00	–8.00
DIFF_SSTL18_II	0.300	0.900	1.425	0.100	—	$(V_{CCO}/2) - 0.600$	$(V_{CCO}/2) + 0.600$	13.4	–13.4

Notes:

- V_{ICM} is the input common mode voltage.
- V_{ID} is the input differential voltage ($Q - \overline{Q}$).
- V_{OL} is the single-ended low-output voltage.
- V_{OH} is the single-ended high-output voltage.

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications from the Vivado® Design Suite as outlined in [Table 12](#).

Table 12: Speed Specification Version By Device

2018.2.1	Device
1.23	XC7S6, XC7S15, XC7S25, XC7S50, XC7S75, XC7S100
1.16	XA7S6, XA7S15, XA7S25, XA7S50, XA7S75, XA7S100

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows.

Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Spartan-7 FPGAs.

Table 15: Networking Applications Interface Performances (Cont'd)

Description	V _{CCINT} Operating Voltage, Speed Grade, and Temperature Range			Units
	1.0V		0.95V	
	-2C/-2I	-1C/-1I/-1Q	-1LI	
DDR LVDS receiver ⁽¹⁾	1250	950	950	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

Table 16: Maximum Physical Interface (PHY) Rate for Memory Interface IP available with the Memory Interface Generator⁽¹⁾

Memory Standard	V _{CCINT} Operating Voltage, Speed Grade, and Temperature Range			Units
	1.0V		0.95V	
	-2C/-2I	-1C/-1I/-1Q	-1LI	
4:1 Memory Controllers				
DDR3	800 ⁽²⁾	667	667	Mb/s
DDR3L	800 ⁽²⁾	667	667	Mb/s
DDR2	800 ⁽²⁾	667	667	Mb/s
2:1 Memory Controllers				
DDR3	800 ⁽²⁾	667	667	Mb/s
DDR3L	800 ⁽²⁾	667	667	Mb/s
DDR2	800 ⁽²⁾	667	667	Mb/s
LPDDR2	667	533	533	Mb/s

Notes:

1. V_{REF} tracking is required. For more information, see the *Zynq-7000 AP SoC and 7 Series FPGAs Memory Interface Solutions User Guide* (UG586) [Ref 7].
2. The maximum PHY rate is 667 Mb/s in the FTGB196 package.

IOB Pad Input/Output/3-State

Table 17 summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- T_{IOPi} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- T_{IOPo} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- T_{IOTp} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HR I/O banks, the IN_TERM termination turn-on time is always faster than T_{IOTp} when the INTERMDISABLE pin is used.

Table 17: IOB High Range (HR) Switching Characteristics (Cont'd)

I/O Standard	T _{IOPI}			T _{IOOP}			T _{IOTP}			Units
	V _{CCINT} Operating Voltage and Speed Grade									
	1.0V		0.95V	1.0V		0.95V	1.0V		0.95V	
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
LVC MOS15_F8	0.86	0.93	0.93	1.72	1.98	1.98	1.75	1.99	1.99	ns
LVC MOS15_F12	0.86	0.93	0.93	1.47	1.73	1.73	1.50	1.74	1.74	ns
LVC MOS15_F16	0.86	0.93	0.93	1.46	1.71	1.71	1.49	1.73	1.73	ns
LVC MOS12_S4	0.95	1.02	1.02	2.69	2.95	2.95	2.72	2.96	2.96	ns
LVC MOS12_S8	0.95	1.02	1.02	2.21	2.46	2.46	2.24	2.48	2.48	ns
LVC MOS12_S12	0.95	1.02	1.02	1.91	2.17	2.17	1.94	2.18	2.18	ns
LVC MOS12_F4	0.95	1.02	1.02	2.10	2.35	2.35	2.13	2.37	2.37	ns
LVC MOS12_F8	0.95	1.02	1.02	1.66	1.92	1.92	1.69	1.93	1.93	ns
LVC MOS12_F12	0.95	1.02	1.02	1.51	1.76	1.76	1.54	1.77	1.77	ns
SSTL135_S	0.75	0.82	0.82	1.47	1.73	1.73	1.50	1.74	1.74	ns
SSTL15_S	0.68	0.75	0.75	1.43	1.68	1.68	1.46	1.69	1.69	ns
SSTL18_I_S	0.75	0.82	0.82	1.79	2.04	2.04	1.82	2.06	2.06	ns
SSTL18_II_S	0.75	0.82	0.82	1.43	1.68	1.68	1.46	1.70	1.70	ns
DIFF_SSTL135_S	0.76	0.83	0.83	1.47	1.73	1.73	1.50	1.74	1.74	ns
DIFF_SSTL15_S	0.76	0.83	0.83	1.43	1.68	1.68	1.46	1.69	1.69	ns
DIFF_SSTL18_I_S	0.79	0.86	0.86	1.80	2.06	2.06	1.83	2.07	2.07	ns
DIFF_SSTL18_II_S	0.79	0.86	0.86	1.51	1.76	1.76	1.54	1.77	1.77	ns
SSTL135_F	0.75	0.82	0.82	1.24	1.49	1.49	1.27	1.51	1.51	ns
SSTL15_F	0.68	0.75	0.75	1.19	1.45	1.45	1.22	1.46	1.46	ns
SSTL18_I_F	0.75	0.82	0.82	1.24	1.49	1.49	1.27	1.51	1.51	ns
SSTL18_II_F	0.75	0.82	0.82	1.24	1.49	1.49	1.27	1.51	1.51	ns
DIFF_SSTL135_F	0.76	0.83	0.83	1.24	1.49	1.49	1.27	1.51	1.51	ns
DIFF_SSTL15_F	0.76	0.83	0.83	1.19	1.45	1.45	1.22	1.46	1.46	ns
DIFF_SSTL18_I_F	0.79	0.86	0.86	1.35	1.60	1.60	1.38	1.62	1.62	ns
DIFF_SSTL18_II_F	0.79	0.86	0.86	1.33	1.59	1.59	1.36	1.60	1.60	ns

Table 18 specifies the values of T_{IOTPHZ} and $T_{IOIBUFDISABLE}$. T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). $T_{IOIBUFDISABLE}$ is described as the IOB delay from IBUFDISABLE to O output. In HR I/O banks, the internal IN_TERM termination turn-off time is always faster than T_{IOTPHZ} when the INTERMDISABLE pin is used.

Input Serializer/Deserializer Switching Characteristics

Table 23: ISERDES Switching Characteristics

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Setup/Hold for Control Lines					
T _{ISCKC_BITSLIP} / T _{ISCKC_BITSLIP}	BITSLIP pin setup/hold with respect to CLKDIV.	0.02/0.15	0.02/0.17	0.02/0.17	ns
T _{ISCKC_CE} / T _{ISCKC_CE}	CE pin setup/hold with respect to CLK (for CE1).	0.50/−0.01	0.72/−0.01	0.72/−0.01	ns
T _{ISCKC_CE2} / T _{ISCKC_CE2}	CE pin setup/hold with respect to CLKDIV (for CE2).	−0.10/0.36	−0.10/0.40	−0.10/0.40	ns
Setup/Hold for Data Lines					
T _{ISDCK_D} / T _{ISCKD_D}	D pin setup/hold with respect to CLK.	−0.02/0.14	−0.02/0.17	−0.02/0.17	ns
T _{ISDCK_DDLY} / T _{ISCKD_DDLY}	DDLY pin setup/hold with respect to CLK (using IDELAY). ⁽¹⁾	−0.02/0.14	−0.02/0.17	−0.02/0.17	ns
T _{ISDCK_D_DDR} / T _{ISCKD_D_DDR}	D pin setup/hold with respect to CLK at DDR mode.	−0.02/0.14	−0.02/0.17	−0.02/0.17	ns
T _{ISDCK_DDLY_DDR} / T _{ISCKD_DDLY_DDR}	D pin setup/hold with respect to CLK at DDR mode (using IDELAY). ⁽¹⁾	0.14/0.14	0.17/0.17	0.17/0.17	ns
Sequential Delays					
T _{ISCKO_Q}	CLKDIV to out at Q pin.	0.54	0.66	0.66	ns
Propagation Delays					
T _{ISDO_DO}	D input to DO output pin.	0.11	0.13	0.13	ns

Notes:

- Recorded at 0 tap value.

Output Serializer/Deserializer Switching Characteristics

Table 24: OSERDES Switching Characteristics

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Setup/Hold					
T _{OSDCK_D} / T _{OSCKD_D}	D input setup/hold with respect to CLKDIV.	0.45/0.03	0.63/0.03	0.63/0.03	ns
T _{OSDCK_T} / T _{OSCKD_T}	T input setup/hold with respect to CLK.	0.73/−0.13	0.88/−0.13	0.88/−0.13	ns
T _{OSDCK_T2} / T _{OSCKD_T2}	T input setup/hold with respect to CLKDIV.	0.34/−0.13	0.39/−0.13	0.39/−0.13	ns
T _{OSCKCK_OCE} / T _{OSCKC_OCE}	OCE input setup/hold with respect to CLK.	0.34/0.58	0.51/0.58	0.51/0.58	ns
T _{OSCKCK_S}	SR (reset) input setup with respect to CLKDIV.	0.52	0.85	0.85	ns
T _{OSCKCK_TCE} / T _{OSCKC_TCE}	TCE input setup/hold with respect to CLK.	0.34/0.01	0.51/0.01	0.51/0.01	ns
Sequential Delays					
T _{OSCKO_OQ}	Clock to out from CLK to OQ.	0.42	0.48	0.48	ns
T _{OSCKO_TQ}	Clock to out from CLK to TQ.	0.49	0.56	0.56	ns
Combinatorial					
T _{OSDO_TTQ}	T input to TQ out.	0.92	1.11	1.11	ns

Table 31: DSP48E1 Switching Characteristics (Cont'd)

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
T _{DSPDO_PCIN_CARRYCASCOUT}	PCIN input to CARRYCASCOUT output.	1.56	1.85	1.85	ns
Clock to Outs from Output Register Clock to Output Pins					
T _{DSPCKO_P_PREG}	CLK PREG to P output.	0.37	0.44	0.44	ns
T _{DSPCKO_CARRYCASCOUT_PREG}	CLK PREG to CARRYCASCOUT output.	0.59	0.69	0.69	ns
Clock to Outs from Pipeline Register Clock to Output Pins					
T _{DSPCKO_P_MREG}	CLK MREG to P output.	1.93	2.31	2.31	ns
T _{DSPCKO_CARRYCASCOUT_MREG}	CLK MREG to CARRYCASCOUT output.	2.21	2.64	2.64	ns
T _{DSPCKO_P_ADREG_MULT}	CLK ADREG to P output using multiplier.	3.10	3.69	3.69	ns
T _{DSPCKO_CARRYCASCOUT_ADREG_MULT}	CLK ADREG to CARRYCASCOUT output using multiplier.	3.38	4.02	4.02	ns
Clock to Outs from Input Register Clock to Output Pins					
T _{DSPCKO_P_AREG_MULT}	CLK AREG to P output using multiplier.	4.51	5.37	5.37	ns
T _{DSPCKO_P_BREG}	CLK BREG to P output not using multiplier.	1.87	2.22	2.22	ns
T _{DSPCKO_P_CREG}	CLK CREG to P output not using multiplier.	1.93	2.30	2.30	ns
T _{DSPCKO_P_DREG_MULT}	CLK DREG to P output using multiplier.	4.48	5.32	5.32	ns
Clock to Outs from Input Register Clock to Cascading Output Pins					
T _{DSPCKO_{ACOUT; BCOUT}_{AREG; BREG}}	CLK (ACOUT, BCOUT) to {A,B} register output.	0.73	0.87	0.87	ns
T _{DSPCKO_CARRYCASCOUT_{AREG; BREG}_MULT}	CLK (AREG, BREG) to CARRYCASCOUT output using multiplier.	4.79	5.70	5.70	ns
T _{DSPCKO_CARRYCASCOUT_BREG}	CLK BREG to CARRYCASCOUT output not using multiplier.	2.15	2.55	2.55	ns
T _{DSPCKO_CARRYCASCOUT_DREG_MULT}	CLK DREG to CARRYCASCOUT output using multiplier.	4.76	5.65	5.65	ns
T _{DSPCKO_CARRYCASCOUT_CREG}	CLK CREG to CARRYCASCOUT output.	2.21	2.63	2.63	ns
Maximum Frequency					
F _{MAX}	With all registers used.	550.66	464.25	464.25	MHz
F _{MAX_PATDET}	With pattern detector.	465.77	392.93	392.93	MHz
F _{MAX_MULT_NOMREG}	Two register multiply without MREG.	305.62	257.47	257.47	MHz
F _{MAX_MULT_NOMREG_PATDET}	Two register multiply without MREG with pattern detect.	277.62	233.92	233.92	MHz
F _{MAX_PREADD_MULT_NOADREG}	Without ADREG.	346.26	290.44	290.44	MHz
F _{MAX_PREADD_MULT_NOADREG_PATDET}	Without ADREG with pattern detect.	346.26	290.44	290.44	MHz
F _{MAX_NOPIPELINEREG}	Without pipeline registers (MREG, ADREG).	227.01	190.69	190.69	MHz
F _{MAX_NOPIPELINEREG_PATDET}	Without pipeline registers (MREG, ADREG) with pattern detect.	211.15	177.43	177.43	MHz

Clock Buffers and Networks

Table 32: Global Clock Switching Characteristics (Including BUFGCTRL)

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
T _{BCCCK_CE} /T _{BCCCK_CE} ⁽¹⁾	CE pins setup/hold.	0.13/0.40	0.16/0.41	0.16/0.41	ns
T _{BCCCK_S} /T _{BCCCK_S} ⁽¹⁾	S pins setup/hold.	0.13/0.40	0.16/0.41	0.16/0.41	ns
T _{BCKO_O} ⁽²⁾	BUFGCTRL delay from I0/I1 to O.	0.09	0.10	0.10	ns
Maximum Frequency					
F _{MAX_BUFG}	Global clock tree (BUFG).	628.00	464.00	464.00	MHz

Notes:

1. T_{BCCCK_CE} and T_{BCCCK_CE} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. T_{BCKO_O} (BUFG delay from I0 to O) values are the same as T_{BCKO_O} values.

Table 33: Input/Output Clock Switching Characteristics (BUFIO)

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
T _{BIOCKO_O}	Clock to out delay from I to O.	1.26	1.54	1.54	ns
Maximum Frequency					
F _{MAX_BUFIO}	I/O clock tree (BUFIO).	680.00	600.00	600.00	MHz

Table 34: Regional Clock Buffer Switching Characteristics (BUFR)

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
T _{BRCKO_O}	Clock to out delay from I to O.	0.76	0.99	0.99	ns
T _{BRCKO_O_BYP}	Clock to out delay from I to O with Divide Bypass attribute set.	0.39	0.52	0.52	ns
T _{BRDO_O}	Propagation delay from CLR to O.	0.85	1.09	1.09	ns
Maximum Frequency					
F _{MAX_BUFR} ⁽¹⁾	Regional clock tree (BUFR).	375.00	315.00	315.00	MHz

Notes:

1. The maximum input frequency to the BUFR is the BUFIO F_{MAX} frequency.

Table 35: Horizontal Clock Buffer Switching Characteristics (BUFH)

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
T _{BHCKO_O}	BUFH delay from I to O.	0.11	0.13	0.13	ns
T _{BHCKK_CE} / T _{BHCKC_CE}	CE pin setup and hold.	0.22/0.15	0.28/0.21	0.28/0.21	ns
Maximum Frequency					
F _{MAX_BUFH}	Horizontal clock buffer (BUFH).	628.00	464.00	464.00	MHz

Table 36: Duty Cycle Distortion and Clock-Tree Skew

Symbol	Description	Device	V _{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
T _{DCD_CLK}	Global clock tree duty-cycle distortion. ⁽¹⁾	All	0.20	0.20	0.20	ns
T _{CKSKEW}	Global clock tree skew. ⁽²⁾	XC7S6	0.05	0.06	0.06	ns
		XC7S15	0.05	0.06	0.06	ns
		XC7S25	0.26	0.26	0.26	ns
		XC7S50	0.26	0.26	0.26	ns
		XC7S75	0.33	0.36	0.36	ns
		XC7S100	0.33	0.36	0.36	ns
		XA7S6	0.05	0.06	N/A	ns
		XA7S15	0.05	0.06	N/A	ns
		XA7S25	0.26	0.26	N/A	ns
		XA7S50	0.26	0.26	N/A	ns
		XA7S75	0.33	0.36	N/A	ns
		XA7S100	0.33	0.36	N/A	ns
T _{DCD_BUFIO}	I/O clock tree duty cycle distortion.	All	0.14	0.14	0.14	ns
T _{BUFIOSKEW}	I/O clock tree skew across one clock region.	All	0.03	0.03	0.03	ns
T _{DCD_BUFR}	Regional clock tree duty cycle distortion.	All	0.18	0.18	0.18	ns

Notes:

- These parameters represent the worst-case duty cycle distortion observable at the I/O flip flops. For all I/O standards, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
- The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx timing analysis tools to evaluate clock skew specific to your application.

Table 38: PLL Specification

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
PLL_F _{BANDWIDTH}	Low PLL bandwidth at typical.	1.00	1.00	1.00	MHz
	High PLL bandwidth at typical. ⁽¹⁾	4.00	4.00	4.00	MHz
PLL_T _{STATPHAOFFSET}	Static phase offset of the PLL outputs. ⁽²⁾	0.12	0.12	0.12	ns
PLL_T _{OUTJITTER}	PLL output jitter.	Note 3			
PLL_T _{OUTDUTY}	PLL output clock duty-cycle precision. ⁽⁴⁾	0.20	0.20	0.20	ns
PLL_T _{LOCKMAX}	PLL maximum lock time.	100.00	100.00	100.00	μs
PLL_F _{OUTMAX}	PLL maximum output frequency.	800.00	800.00	800.00	MHz
PLL_F _{OUTMIN}	PLL minimum output frequency. ⁽⁵⁾	6.25	6.25	6.25	MHz
PLL_T _{EXTFDVAR}	External clock feedback variation.	< 20% of clock input period or 1 ns Max			
PLL_RST _{MINPULSE}	Minimum reset pulse width.	5.00	5.00	5.00	ns
PLL_F _{PFDMAX}	Maximum frequency at the phase frequency detector.	500.00	450.00	450.00	MHz
PLL_F _{PFDMIN}	Minimum frequency at the phase frequency detector.	19.00	19.00	19.00	MHz
PLL_T _{FBDELAY}	Maximum delay in the feedback path.	3 ns Max or one CLKIN cycle			
Dynamic Reconfiguration Port (DRP) for PLL Before and After DCLK					
T _{PLLDCK_DADDR} / T _{PLLCKD_DADDR}	Setup and hold of D address.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
T _{PLLDCK_DI} / T _{PLLCKD_DI}	Setup and hold of D input.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
T _{PLLDCK_DEN} / T _{PLLCKD_DEN}	Setup and hold of D enable.	1.97/0.00	2.29/0.00	2.29/0.00	ns, Min
T _{PLLDCK_DWE} / T _{PLLCKD_DWE}	Setup and hold of D write enable.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
T _{PLLCKO_DRDY}	CLK to out of DRDY.	0.72	0.99	0.99	ns, Max
F _{DCK}	DCLK frequency.	200.00	200.00	200.00	MHz, Max

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the *Clocking Wizard* [Ref 8].
4. Includes global clock buffer.
5. Calculated as FVCO/128 assuming output duty cycle is 50%.

Device Pin-to-Pin Output Parameter Guidelines

Table 39: Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)⁽¹⁾

Symbol	Description	Device	V _{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM/PLL.						
T _{ICKOF}	Clock-capable clock input and OUTFF at pins/banks closest to the BUFGs <i>without</i> MMCM/PLL (near clock region). ⁽²⁾	XC7S6	5.55	6.50	6.50	ns
		XC7S15	5.55	6.50	6.50	ns
		XC7S25	5.55	6.44	6.44	ns
		XC7S50	5.71	6.62	6.62	ns
		XC7S75	5.73	6.71	6.71	ns
		XC7S100	5.73	6.71	6.71	ns
		XA7S6	5.55	6.50	N/A	ns
		XA7S15	5.55	6.50	N/A	ns
		XA7S25	5.55	6.44	N/A	ns
		XA7S50	5.71	6.62	N/A	ns
		XA7S75	5.73	6.71	N/A	ns
		XA7S100	5.73	6.71	N/A	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Refer to the *Die Level Bank Numbering Overview* section of the *7 Series FPGA Packaging and Pinout Specification* (UG475) [Ref 4].

Table 41: Clock-Capable Clock Input to Output Delay With MMCM⁽¹⁾

Symbol	Description	Device	V _{CCINT} Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>with</i> MMCM.						
T _{ICKOFMMCMCC}	Clock-capable clock input and OUTFF <i>with</i> MMCM. ⁽²⁾	XC7S6	1.03	1.03	1.03	ns
		XC7S15	1.03	1.03	1.03	ns
		XC7S25	1.00	1.00	1.00	ns
		XC7S50	1.00	1.00	1.00	ns
		XC7S75	1.00	1.00	1.00	ns
		XC7S100	1.00	1.00	1.00	ns
		XA7S6	1.03	1.03	N/A	ns
		XA7S15	1.03	1.03	N/A	ns
		XA7S25	1.00	1.00	N/A	ns
		XA7S50	1.00	1.00	N/A	ns
		XA7S75	1.00	1.00	N/A	ns
		XA7S100	1.00	1.00	N/A	ns

Notes:

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 48: Sample Window

Symbol	Description	V _{CCINT} Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
T _{SAMP}	Sampling error at receiver pins. ⁽¹⁾	0.64	0.70	0.70	ns
T _{SAMP_BUFIO}	Sampling error at receiver pins using BUFIO. ⁽²⁾	0.40	0.46	0.46	ns

Notes:

1. This parameter indicates the total sampling error of the Spartan-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
 - CLK0 MMCM jitter
 - MMCM accuracy (phase offset)
 - MMCM phase shift resolution
These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of the Spartan-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Additional Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for Spartan-7 FPGA clock transmitter and receiver data-valid windows.

Table 49: Package Skew⁽¹⁾

Symbol	Description	Device	Package	Value	Units
$T_{PKGSKEW}$	Package skew. ⁽²⁾	XC7S6	CPGA196	44	ps
			CSGA225	83	ps
			FTGB196	65	ps
		XC7S15	CPGA196	44	ps
			CSGA225	83	ps
			FTGB196	65	ps
		XC7S25	CSGA225	93	ps
			CSGA324	62	ps
			FTGB196	83	ps
		XC7S50	CSGA324	80	ps
			FGGA484	110	ps
			FTGB196	103	ps
		XC7S75	FGGA484	117	ps
			FGGA676	110	ps
		XC7S100	FGGA484	117	ps
			FGGA676	110	ps
		XA7S6	CPGA196	44	ps
			CSGA225	83	ps
			FTGB196	65	ps
		XA7S15	CPGA196	44	ps
			CSGA225	83	ps
			FTGB196	65	ps
		XA7S25	CSGA225	93	ps
			CSGA324	62	ps
			FTGB196	83	ps
		XA7S50	CSGA324	80	ps
			FGGA484	110	ps
			FTGB196	103	ps
		XA7S75	FGGA484	117	ps
			FGGA676	110	ps
		XC7S100	FGGA484	117	ps
			FGGA676	110	ps

Notes:

- Package delay information is available for these device/package combinations. This information can be used to deskew the package.
- These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.

XADC Specifications

The 7 Series FPGAs Overview (DS180) [Ref 1] and XA Spartan-7 Automotive FPGA Data Sheet: Overview (DS171) [Ref 2] list the devices that contain a 7 series XADC dual 12-Bit 1 MSPS analog-to-digital converter.

Table 50: XADC Specifications

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
$V_{CCADC} = 1.8V \pm 5\%$, $V_{REFP} = 1.25V$, $V_{REFN} = 0V$, $ADCCLK = 26\text{ MHz}$, $-55^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$. Typical values at $T_j = +40^{\circ}\text{C}$.						
ADC Accuracy⁽¹⁾						
Resolution			12	–	–	Bits
Integral nonlinearity ⁽²⁾	INL	$-40^{\circ}\text{C} \leq T_j \leq 100^{\circ}\text{C}$	–	–	± 2	LSBs
		$-55^{\circ}\text{C} \leq T_j < -40^{\circ}\text{C}$; $100^{\circ}\text{C} < T_j \leq 125^{\circ}\text{C}$	–	–	± 3	LSBs
Differential nonlinearity	DNL	No missing codes, guaranteed monotonic.	–	–	± 1	LSBs
Offset error	Unipolar	$-40^{\circ}\text{C} \leq T_j \leq 100^{\circ}\text{C}$	–	–	± 8	LSBs
		$-55^{\circ}\text{C} \leq T_j < -40^{\circ}\text{C}$; $100^{\circ}\text{C} < T_j \leq 125^{\circ}\text{C}$	–	–	± 12	LSBs
	Bipolar	$-55^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$	–	–	± 4	LSBs
Gain error			–	–	± 0.5	%
Offset matching			–	–	4	LSBs
Gain matching			–	–	0.3	%
Sample rate			–	–	1	MS/s
Signal to noise ratio ⁽²⁾	SNR	$F_{SAMPLE} = 500\text{ KS/s}$, $F_{IN} = 20\text{ kHz}$	60	–	–	dB
RMS code noise		External 1.25V reference.	–	–	2	LSBs
		On-chip reference.	–	3	–	LSBs
Total harmonic distortion ⁽²⁾	THD	$F_{SAMPLE} = 500\text{ KS/s}$, $F_{IN} = 20\text{ kHz}$	70	–	–	dB
Analog Inputs⁽³⁾						
ADC input ranges		Unipolar operation.	0	–	1	V
		Bipolar operation.	–0.5	–	+0.5	V
		Unipolar common mode range (FS input).	0	–	+0.5	V
		Bipolar common mode range (FS input).	+0.5	–	+0.6	V
Maximum external channel input ranges		Adjacent analog channels set within these ranges should not corrupt measurements on adjacent channels.	–0.1	–	V_{CCADC}	V
Full-resolution bandwidth	FRBW	Auxiliary channel full resolution bandwidth.	250	–	–	kHz
On-chip Sensors						
Temperature sensor error		$-40^{\circ}\text{C} \leq T_j \leq 100^{\circ}\text{C}$	–	–	± 4	$^{\circ}\text{C}$
		$-55^{\circ}\text{C} \leq T_j < -40^{\circ}\text{C}$; $100^{\circ}\text{C} < T_j \leq 125^{\circ}\text{C}$	–	–	± 6	$^{\circ}\text{C}$
Supply sensor error		$-40^{\circ}\text{C} \leq T_j \leq 100^{\circ}\text{C}$	–	–	± 1	%
		$-55^{\circ}\text{C} \leq T_j < -40^{\circ}\text{C}$; $100^{\circ}\text{C} < T_j \leq 125^{\circ}\text{C}$	–	–	± 2	%

eFUSE Programming Conditions

Table 52 lists the programming conditions specifically for eFUSE. For more information, see the *7 Series FPGA Configuration User Guide* (UG470) [Ref 10].

Table 52: eFUSE Programming Conditions⁽¹⁾

Symbol	Description	Min	Typ	Max	Units
I_{FS}	V_{CCAUX} supply current	–	–	115	mA
T_j	Temperature range	15	–	125	°C

Notes:

1. The FPGA must not be configured during eFUSE programming.

References

1. *7 Series FPGAs Overview* (DS180)
2. *XA Spartan-7 Automotive FPGA Data Sheet: Overview* (DS171)
3. *7 Series FPGAs SelectIO Resources User Guide* (UG471)
4. *7 Series FPGA Packaging and Pinout Specification* (UG475)
5. *7 Series FPGAs PCB Design Guide* (UG483)
6. *Xilinx Power Estimator* spreadsheet tool (XPE)
7. *Zynq-7000 AP SoC and 7 Series FPGAs Memory Interface Solutions User Guide* (UG586)
8. See the [Clocking Wizard](#) in Vivado software.
9. *7 Series FPGAs and Zynq-7000 AP SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480)
10. *7 Series FPGA Configuration User Guide* (UG470)

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
07/31/2018	1.7	In Table 12 , updated Vivado tools version to 2018.2.1. In Table 13 , moved all speed grades for all devices to Production. In Table 14 , added Vivado tools version for XC7S6, XC7S15, XC7S75, XC7S100, XA7S6, XA7S15, XA7S75, and XA7S100.
06/18/2018	1.6	In Table 12 , updated Vivado tools version to 2018.2. In Table 13 , moved all speed grades except -1Q (1.0V) for XC7S6 and XC7S15 to Production. In Table 14 , added Vivado tools version for XC7S6 and XC7S15.
04/04/2018	1.5	Added XA7S6, XA7S15, XA7S25, XA7S75, and XA7S100 devices throughout. In Table 5 , updated typical quiescent supply current values for XC7S25 and XC7S50 devices, and added values for XC7S6, XC7S15, XC7S75, and XC7S100 devices. In Table 6 , updated table title and $I_{CCINTMIN}$ and $I_{CCAUXMIN}$ for XC7S75 and XC7S100 devices. In Table 13 , moved all speed grades for XC7S6 and XC7S15 to Preliminary, moved -1LI (0.95V) speed grade for XC7S25 to Production, and moved all speed grades except -1Q (1.0V) for XC7S75 and XC7S100 from Preliminary to Production. In Table 14 , added Vivado tools version for XC7S25, XC7S75, and XC7S100. In Table 36 , Table 39 , Table 40 , Table 41 , Table 42 , Table 44 , Table 45 , and Table 46 , changed parameter value for XA7S50 to N/A. In Table 49 , added package skew values for XC7S6 and XC7S15 devices.
12/22/2017	1.4	In Table 12 , updated Vivado tools version to 2017.4. In Table 13 , moved all speed grades for XC7S75 and XC7S100 from Advance to Preliminary and all speed grades except -1LI (0.95V) for XC7S25 from Advance to Production. In Table 14 , added Vivado tools version for XC7S25. Added Note 2 to Table 16 . In Table 49 , added package skew values for XC7S25 device in CSGA324 package and XC7S75 and XC7S100 devices in FGGA676 package.
11/20/2017	1.3	Added XA7S50 device throughout. Updated description of offered temperature ranges in second paragraph of Introduction . Added row for junction temperature (T_j) at expanded (Q) temperature to Table 2 . Added -1Q (1.0V) speed grade to Table 5 , and Table 13 to Table 16 . In Table 12 , updated Vivado tools version to 2017.3. In Table 49 , added package skew values for XC7S25, XC7S50, XC7S75, and XC7S100 devices in CSGA225, FTGB196, and FGGA484 packages. Added <i>XA Spartan-7 Automotive FPGA Data Sheet: Overview (DS171)</i> to References .
06/20/2017	1.2	Updated paragraph before Table 6 . In Table 12 , updated Vivado tools version to 2017.2. In Table 13 , moved all speed grades for XC7S50 from Preliminary to Production and updated Note 1 . In Table 14 , added Vivado tools version for XC7S50. In Table 49 , added package skew value for XC7S50 device in FGGA484 package.
04/07/2017	1.1	Added 1.35V to Note 5 in Table 2 . In Table 12 , updated Vivado tools version to 2016.4. In Table 13 , moved all speed grades for XC7S50 from Advance to Preliminary. Removed SFI-4.1 and SPI-4.2 from descriptions of SDR LVDS receiver and DDR LVDS receiver, respectively, in Table 15 . In Table 25 , changed $T_{IDELAYRESOLUTION}$ units from ps to μ s. Removed BUFMR from Note 1 in Table 34 . In Table 49 , replaced TQGA144 with FTGB196 for XC7S6, XC7S15, and XC7S25 devices, added FTGB196 package for XC7S50 device, and added package skew value for XC7S50 device in CSGA324 package.
09/27/2016	1.0	Initial Xilinx release.