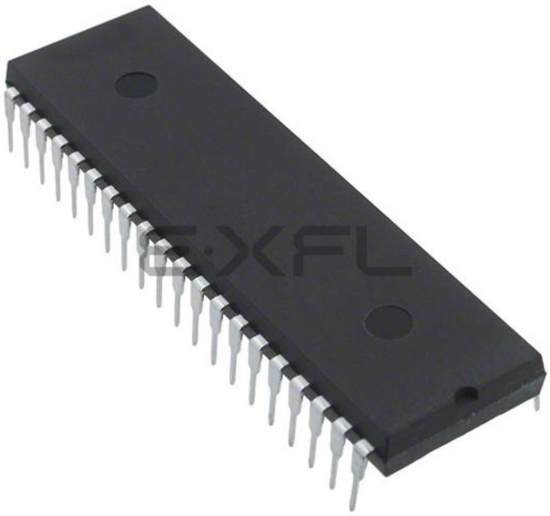

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C251
Core Size	8/16-Bit
Speed	24MHz
Connectivity	EBI/EMI, I²C, Microwire, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIL
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at80251g2d-3csum

Block Diagram

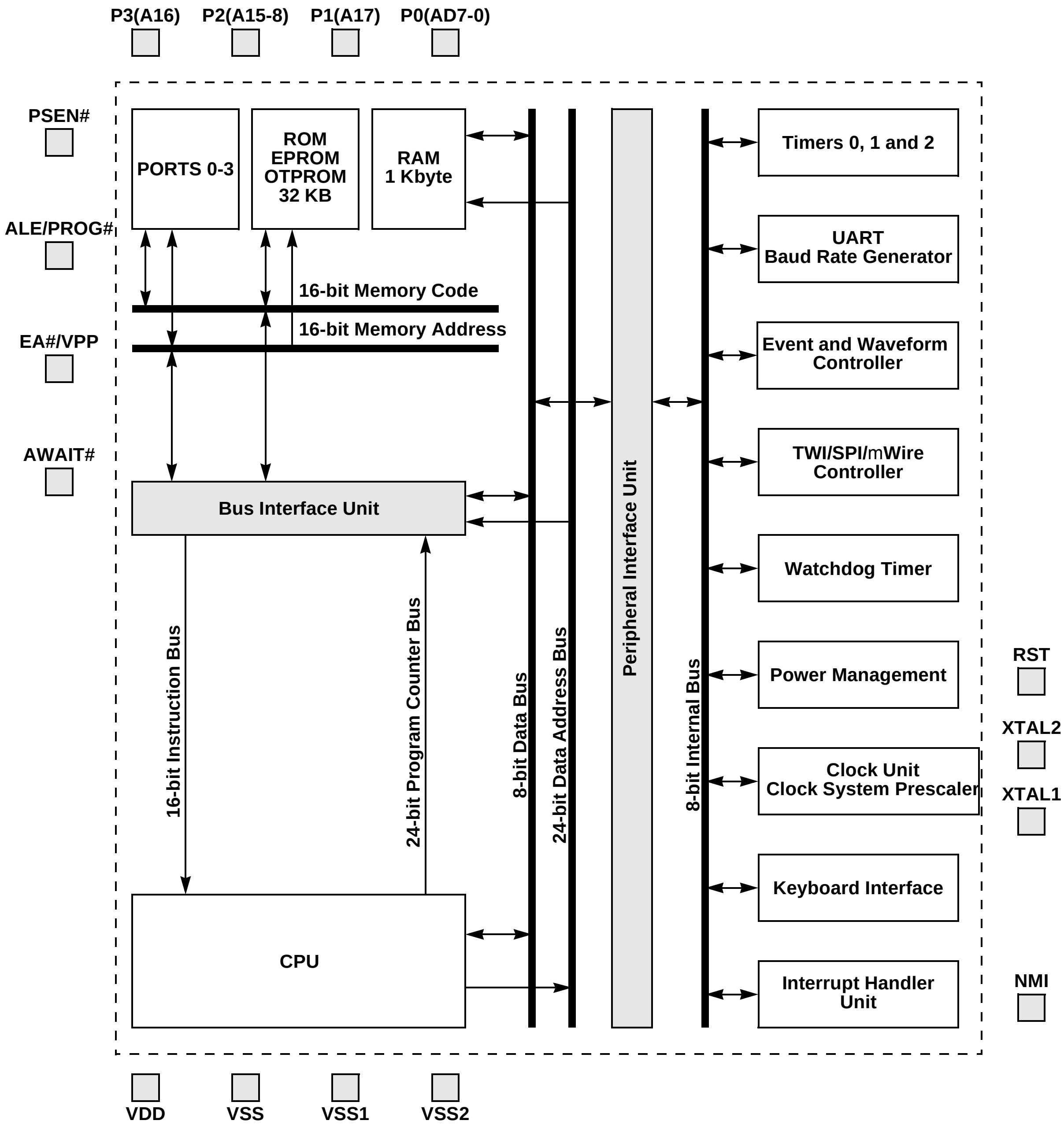


Table 1. TSC80251G2D Pin Assignment

DIP	PLCC	VQFP	Name	DIP	PLCC	VQFP	Name
	1	39	VSS1		23	17	VSS2
1	2	40	P1.0/T2	21	24	18	P2.0/A8
2	3	41	P1.1/T2EX	22	25	19	P2.1/A9
3	4	42	P1.2/ECI	23	26	20	P2.2/A10
4	5	43	P1.3/CEX0	24	27	21	P2.3/A11
5	6	44	P1.4/CEX1/SS#	25	28	22	P2.4/A12
6	7	1	P1.5/CEX2/MISO	26	29	23	P2.5/A13
7	8	2	P1.6/CEX3/SCL/SCK/WAIT#	27	30	24	P2.6/A14
8	9	3	P1.7/A17/CEX4/SDA/MOSI/WCLK	28	31	25	P2.7/A15
9	10	4	RST	29	32	26	PSEN#
10	11	5	P3.0/RXD	30	33	27	ALE/PROG#
	12	6	AWAIT#		34	28	NMI
11	13	7	P3.1/TXD	31	35	29	EA#/VPP
12	14	8	P3.2/INT0#	32	36	30	P0.7/AD7
13	15	9	P3.3/INT1#	33	37	31	P0.6/AD6
14	16	10	P3.4/T0	34	38	32	P0.5/AD5
15	17	11	P3.5/T1	35	39	33	P0.4/AD4
16	18	12	P3.6/WR#	36	40	34	P0.3/AD3
17	19	13	P3.7/A16/RD#	37	41	35	P0.2/AD2
18	20	14	XTAL2	38	42	36	P0.1/AD1
19	21	15	XTAL1	39	43	37	P0.0/AD0
20	22	16	VSS	40	44	38	VDD

Table 2. Product Name Signal Description (Continued)

Signal Name	Type	Description	Alternate Function
XTAL2	O	**Output of the on-chip inverting oscillator amplifier** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, leave XTAL2 unconnected.	–

Note: The description of A15:8/P2.7:0 and AD7:0/P0.7:0 are for the Non-Page mode chip configuration. If the chip is configured in Page mode operation, port 0 carries the lower address bits (A7:0) while port 2 carries the upper address bits (A15:8) and the data (D7:0).

Address Spaces

The TSC80251G2D derivatives implement four different address spaces:

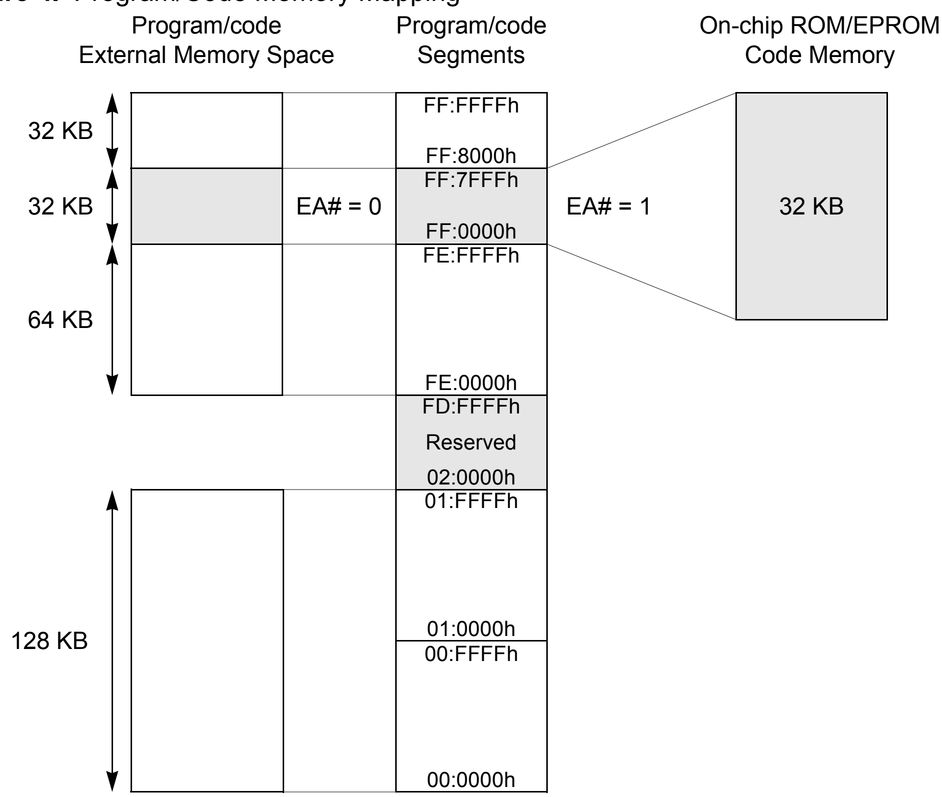
- On-chip ROM program/code memory (not present in ROMless devices)
- On-chip RAM data memory
- Special Function Registers (SFRs)
- Configuration array

Program/Code Memory

The TSC83251G2D and TSC87251G2D implement 32 KB of on-chip program/code memory. Figure 4 shows the split of the internal and external program/code memory spaces. If EA# is tied to a high level, the 32-Kbyte on-chip program memory is mapped in the lower part of segment FF: where the C251 core jumps after reset. The rest of the program/code memory space is mapped to the external memory. If EA# is tied to a low level, the internal program/code memory is not used and all the accesses are directed to the external memory.

The TSC83251G2D products provide the internal program/code memory in a masked ROM memory while the TSC87251G2D products provide it in an EPROM memory. For the TSC80251G2D products, there is no internal program/code memory and EA# must be tied to a low level.

Figure 4. Program/Code Memory Mapping



Note: Special care should be taken when the Program Counter (PC) increments:
If the program executes exclusively from on-chip code memory (not from external memory), beware of executing code from the upper eight bytes of the on-chip ROM (FF:7FF8h-FF:7FFFh). Because of its pipeline capability, the TSC80251G2D derivative may attempt to prefetch code from external memory (at an address above FF:7FFFh) and thereby disrupt I/O Ports 0 and 2. Fetching code constants from these 8 bytes does not affect Ports 0 and 2.
When PC reaches the end of segment FF:, it loops to the reset address FF:0000h (for

compatibility with the C51 Architecture). When PC increments beyond the end of segment FE:, it continues at the reset address FF:0000h (linearity). When PC increments beyond the end of segment 01:, it loops to the beginning of segment 00: (this prevents from its going into the reserved area).

Data Memory

The TSC80251G2D derivatives implement 1 Kbyte of on-chip data RAM. Figure 5 shows the split of the internal and external data memory spaces. This memory is mapped in the data space just over the 32 bytes of registers area (see TSC80251 Programmers' Guide). Hence, the part of the on-chip RAM located from 20h to FFh is bit addressable. This on-chip RAM is not accessible through the program/code memory space.

For faster computation with the on-chip ROM/EPROM code of the TSC83251G2D/TSC87251G2D, its upper 16 KB are also mapped in the upper part of the region 00: if the On-Chip Code Memory Map configuration bit is cleared (EMAP# bit in UCONFIG1 byte, see Figure). However, if EA# is tied to a low level, the TSC80251G2D derivative is running as a ROMless product and the code is actually fetched in the corresponding external memory (i.e. the upper 16 KB of the lower 32 KB of the segment FF:). If EMAP# bit is set, the on-chip ROM is not accessible through the region 00:.

All the accesses to the portion of the data space with no on-chip memory mapped onto are redirected to the external memory.

Figure 5. Data Memory Mapping

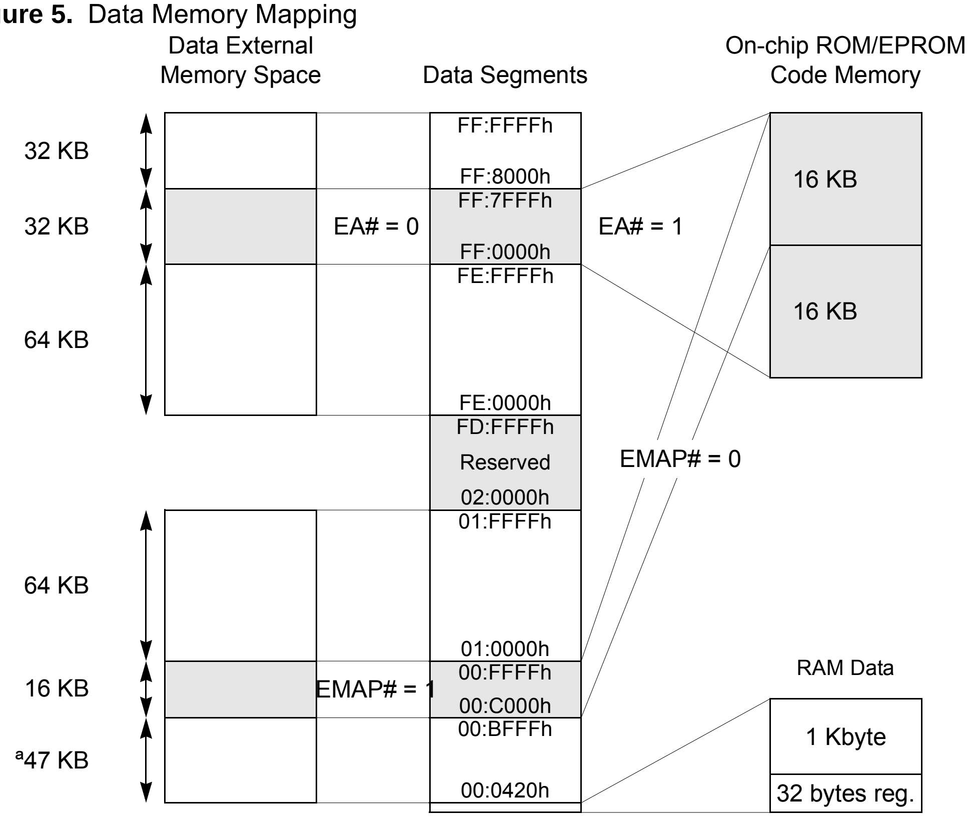


Table 7. System Management SFRs

Mnemonic	Name	Mnemonic	Name
PCON	Power Control	CKRL	Clock Reload
POWM	Power Management	WCON	Synchronous Real-Time Wait State Control

Table 8. Interrupt SFRs

Mnemonic	Name	Mnemonic	Name
IE0	Interrupt Enable Control 0	IPL0	Interrupt Priority Control Low 0
IE1	Interrupt Enable Control 1	IPH1	Interrupt Priority Control High 1
IPH0	Interrupt Priority Control High 0	IPL1	Interrupt Priority Control Low 1

Table 9. Keyboard Interface SFRs

Mnemonic	Name	Mnemonic	Name
P1IE	Port 1 Input Interrupt Enable	P1LS	Port 1 Level Selection
P1F	Port 1 Flag		

Table 19. Notation for Register Operands

Register	Description	C251	C51
at Ri	A memory location (00h-FFh) addressed indirectly via byte registers R0 or R1	–	3
Rn n	Byte register R0-R7 of the currently selected register bank Byte register index: n = 0-7	–	3
Rm Rmd Rms m, md, ms	Byte register R0-R15 of the currently selected register file Destination register Source register Byte register index: m, md, ms = 0-15	3	–
WRj WRjd WRjs at WRj at WRj +dis16 j, jd, js	Word register WR0, WR2, ..., WR30 of the currently selected register file Destination register Source register A memory location (00:0000h-00:FFFFh) addressed indirectly through word register WR0-WR30, is the target address for jump instructions. A memory location (00:0000h-00:FFFFh) addressed indirectly through word register (WR0-WR30) + 16-bit signed (two’s complement) displacement value Word register index: j, jd, js = 0-30	3	–
DRk DRkd DRks at DRk at DRk +dis16 k, kd, ks	Dword register DR0, DR4, ..., DR28, DR56, DR60 of the currently selected register file Destination register Source register A memory location (00:0000h-FF:FFFFh) addressed indirectly through dword register DR0-DR28, DR56 and DR60, is the target address for jump instruction A memory location (00:0000h-FF:FFFFh) addressed indirectly through dword register (DR0-DR28, DR56, DR60) + 16-bit (two’s complement) signed displacement value Dword register index: k, kd, ks = 0, 4, 8..., 28, 56, 60	3	–

4. If this instruction addresses external memory location, add 2(N+2) to the number of states (N: number of wait states).

Table 21. Summary of Increment and Decrement Instructions

IncrementINC <dest>dest opnd ← dest opnd + 1
IncrementINC <dest>, <src>dest opnd ← dest opnd + src opnd
DecrementDEC <dest>dest opnd ← dest opnd - 1
DecrementDEC <dest>, <src>dest opnd ← dest opnd - src opnd

Mnemonic	<dest>, <src>[1]	Comments	Binary Mode		Source Mode	
			Bytes	States	Bytes	States
INC DEC	A	ACC by 1	1	1	1	1
	Rn	Register by 1	1	1	2	2
	dir8	Direct address (on-chip RAM or SFR) by 1	2	2[2]	2	2[2]
	at Ri	Indirect address by 1	1	3	2	4
INC DEC	Rm, #short	Byte register by 1, 2, or 4	3	2	2	1
	WRj, #short	Word register by 1, 2, or 4	3	2	2	1
INC	DRk, #short	Double word register by 1, 2, or 4	3	4	2	3
DEC	DRk, #short	Double word register by 1, 2, or 4	3	5	2	4
INC	DPTR	Data pointer by 1	1	1	1	1

Notes: 1. A shaded cell denotes an instruction in the C51 Architecture.
2. If this instruction addresses an I/O Port (Px, x = 0-3), add 2 to the number of states. Add 3 if it addresses a Peripheral SFR.

Table 30. Summary of Conditional Jump Instructions (2/2)

Jump if bitJB <src>, rel(PC) ← (PC) + size (instr);
IF [src opnd = 1] THEN (PC) ← (PC) + rel

Jump if not bitJNB <src>, rel(PC) ← (PC) + size (instr);
IF [src opnd = 0] THEN (PC) ← (PC) + rel

Jump if bit and clearJBC <dest>, rel(PC) ← (PC) + size (instr);
IF [dest opnd = 1] THEN
dest opnd ← 0
(PC) ← (PC) + rel

Jump if accumulator is zeroJZ rel(PC) ← (PC) + size (instr);
IF [(A) = 0] THEN (PC) ← (PC) + rel

Jump if accumulator is not zeroJNZ rel(PC) ← (PC) + size (instr);
IF [(A) ≠ 0] THEN (PC) ← (PC) + rel

Compare and jump if not equalCJNE <src1>, <src2>, rel(PC) ← (PC) + size (instr);
IF [src opnd1 < src opnd2] THEN (CY) ← 1
IF [src opnd1 ≥ src opnd2] THEN (CY) ← 0
IF [src opnd1 ≠ src opnd2] THEN (PC) ← (PC) + rel

Decrement and jump if not zeroDJNZ <dest>, rel(PC) ← (PC) + size (instr); dest opnd ← dest opnd -1;
IF [φ (Z)] THEN (PC) ← (PC) + rel

Mnemonic	<dest>, <src>(1)	Comments	Binary Mode(2)		Source Mode(2)	
			Bytes	States	Bytes	States
JB	bit51, rel	Jump if direct bit is set	3	2/5(3)(6)	3	2/5(3)(6)
	bit, rel	Jump if direct bit of 8-bit address location is set	5	4/7(3)(6)	4	3/6(3)(6)
JNB	bit51, rel	Jump if direct bit is not set	3	2/5(3)(6)	3	2/5(3)(6)
	bit, rel	Jump if direct bit of 8-bit address location is not set	5	4/7(3)(6)	4	3/6(3)
JBC	bit51, rel	Jump if direct bit is set & clear bit	3	4/7(5)(6)	3	4/7(5)(6)
	bit, rel	Jump if direct bit of 8-bit address location is set and clear	5	7/10(5)(6)	4	6/9(5)(6)
JZ	rel	Jump if ACC is zero	2	2/5(6)	2	2/5(6)
JNZ	rel	Jump if ACC is not zero	2	2/5(6)	2	2/5(6)
CJNE	A, dir8, rel	Compare direct address to ACC and jump if not equal	3	2/5(3)(6)	3	2/5(3)(6)
	A, #data, rel	Compare immediate to ACC and jump if not equal	3	2/5(6)	3	2/5(6)
	Rn, #data, rel	Compare immediate to register and jump if not equal	3	2/5(6)	4	3/6(6)
	at Ri, #data, rel	Compare immediate to indirect and jump if not equal	3	3/6(6)	4	4/7(6)
DJNZ	Rn, rel	Decrement register and jump if not zero	2	2/5(6)	3	3/6(6)
	dir8, rel	Decrement direct address and jump if not zero	3	3/6(4)(6)	3	3/6(4)(6)

Notes:
1. A shaded cell denotes an instruction in the C51 Architecture.
2. States are given as jump not-taken/taken.
3. If this instruction addresses an I/O Port (Px, x = 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.
4. If this instruction addresses an I/O Port (Px, x = 0-3), add 2 to the number of states.

Table 32. Summary of Call and Return Instructions

Absolute callACALL <src>(PC) ← (PC) +2; push $(PC)_{15:0}$;
$(PC)_{10:0}$ ← src opnd
Extended callECALL <src>(PC) ← (PC) + size (instr); push $(PC)_{23:0}$;
$(PC)_{23:0}$ ← src opnd
Long callLCALL <src>(PC) ← (PC) + size (instr); push $(PC)_{15:0}$;
$(PC)_{15:0}$ ← src opnd
Return from subroutineRETpop $(PC)_{15:0}$
Extended return from subroutineERETpop $(PC)_{23:0}$
Return from interruptRETIIF [INTR = 0] THEN pop $(PC)_{15:0}$
IF [INTR = 1] THEN pop $(PC)_{23:0}$; pop (PSW1)
Trap interruptTRAP(PC) ← (PC) + size (instr);
IF [INTR = 0] THEN push $(PC)_{15:0}$
IF [INTR = 1] THEN push (PSW1); push $(PC)_{23:0}$

Mnemonic	<dest>, <src>(1)	Comments	Binary Mode		Source Mode	
			Bytes	States	Bytes	States
ACALL	addr11	Absolute subroutine call	2	9(2)(3)	2	9(2)(3)
ECALL	at DRk	Extended subroutine call (indirect)	3	14(2)(3)	2	13(2)(3)
	addr24	Extended subroutine call	5	14(2)(3)	4	13(2)(3)
LCALL	at WRj	Long subroutine call (indirect)	3	10(2)(3)	2	9(2)(3)
	addr16	Long subroutine call	3	9(2)(3)	3	9(2)(3)
RET		Return from subroutine	1	7(2)	1	7(2)
ERET		Extended subroutine return	3	9(2)	2	8(2)
RETI		Return from interrupt	1	7(2)(4)	1	7(2)(4)
TRAP		Jump to the trap interrupt vector	2	12(4)	1	11(4)

Notes:
1. A shaded cell denotes an instruction in the C51 Architecture.
2. In internal execution only, add 1 to the number of states if the destination/return address is internal and odd.
3. Add 2 to the number of states if the destination address is external.
4. Add 5 to the number of states if INTR = 1.

Lock Bit System

The TSC87251G2D products implement 3 levels of security for User's program as described in Table 33. The TSC83251G2D products implement only the first level of security.

Level 0 is the level of an erased part and does not enable any security features.

Level 1 locks the programming of the User's internal Code Memory, the Configuration Bytes and the Encryption Array.

Level 2 locks the verifying of the User's internal Code Memory. It is always possible to verify the Configuration Bytes and the Lock Bits. It is not possible to verify the Encryption Array.

Level 3 locks the external execution.

Table 33. Lock Bits Programming

Level	Lock bits LB[2:0]	Internal Execution	External Execution	Verification	Programming	External PROM read (MOVC)
0	000	Enable	Enable	Enable(1)	Enable	Enable(2)
1	001	Enable	Enable	Enable(1)	Disable	Disable
2	01x(3)	Enable	Enable	Disable	Disable	Disable
3	1xx(3)	Enable	Disable	Disable	Disable	Disable

Notes:
1. Returns encrypted data if Encryption Array is programmed.
2. Returns non encrypted data.
3. x means don't care. Level 2 always enables level 1, and level 3 always enables levels 1 and 2.

The security level may be verified according to Table 34.

Table 34. Lock Bits Verifying

Level	Lock bits Data(1)
0	xxxxx000
1	xxxxx001
2	xxxxx01x
3	xxxxx1xx

Note: 1. x means don't care.

Encryption Array

The TSC83251G2D and TSC87251G2D products include a 128-byte Encryption Array located in non-volatile memory outside the memory address space. During verification of the on-chip code memory, the seven low-order address bits also address the Encryption Array. As the byte of the code memory is read, it is exclusive-NOR'ed (XNOR) with the key byte from the Encryption Array. If the Encryption Array is not programmed (still all 1s), the user program code is placed on the data bus in its original, unencrypted form. If the Encryption Array is programmed with key bytes, the user program code is encrypted and cannot be used without knowledge of the key byte sequence.

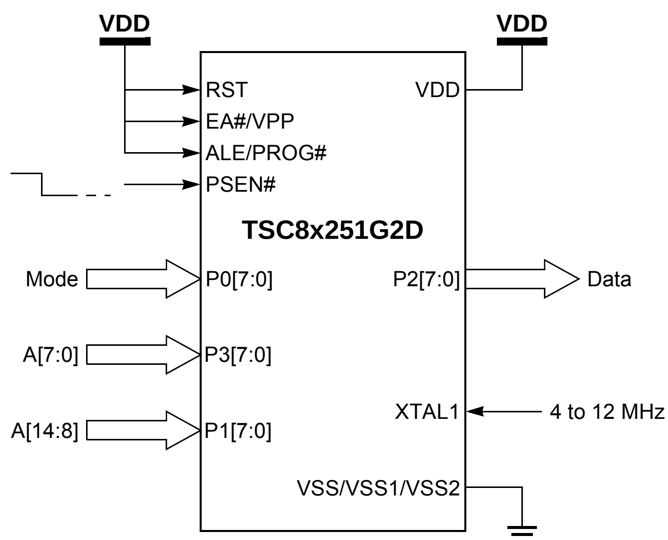
- Then device is driving the data on Port 2.
- It is possible to alternate programming and verification operation (see Paragraph Programming Algorithm). Please make sure the voltage on the EA# pin has actually been lowered to V_{DD} before performing the verifying operation.
- PSEN# and the other control signals have to be released to complete a sequence of verifying operations or a sequence of programming and verifying operations.

Table 37. Verifying Modes

ROM Area[(1)]	RST	EA#/VPP	PSEN#	ALE/PROG#	P0	P2	P1(MSB) P3(LSB)
On-chip code memory	1	1	0	1	28h	Data	16-bit Address 0000h-7FFFh (32 kilobytes)
Configuration Bytes	1	1	0	1	29h	Data	CONFIG0: FFF8h CONFIG1: FFF9h
Lock Bits	1	1	0	1	2Bh	Data	0000h
Signature Bytes	1	1	0	1	29h	Data	0030h, 0031h, 0060h, 0061h

Notes: 1. To preserve the secrecy of on-chip code memory when encrypted, the Encryption Array can not be verified.

Figure 7. Setup for Verifying



AC Characteristics - Commercial & Industrial

AC Characteristics - External Bus Cycles

Definition of Symbols

Table 38. External Bus Cycles Timing Symbol Definitions

Signals	
A	Address
D	Data In
L	ALE
Q	Data Out
R	RD#/PSEN#
W	WR#

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid
Z	Floating

Timings

Test conditions: capacitive load on all pins = 50 pF.

Table 39 and Table 40 list the AC timing parameters for the TSC80251G2D derivatives with no wait states. External wait states can be added by extending PSEN#/RD#/WR# and or by extending ALE. In these tables, Note 2 marks parameters affected by one ALE wait state, and Note 3 marks parameters affected by PSEN#/RD#/WR# wait states.

Figure 8 to Figure 13 show the bus cycles with the timing parameters.

AC Characteristics - SSLC: SPI Interface

Definition of Symbols

Table 48. SPI Interface Timing Symbol Definitions

Signals	
C	Clock
I	Data In
O	Data Out
S	SS#

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid
Z	Floating

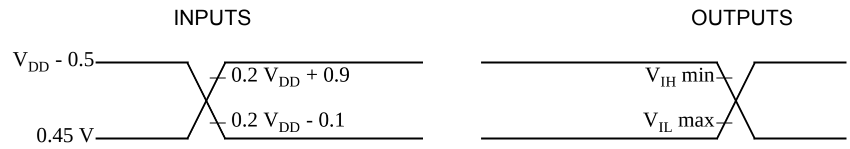
Timings

Table 49. SPI Interface AC Timing; V_{DD} = 2.7 to 5.5 V, T_A = -40 to 85°C

Symbol	Parameter	Min	Max	Unit
		Slave Mode[1]		
T_{CHCH}	Clock Period	8		T_{OSC}
T_{CHCX}	Clock High Time	3.2		T_{OSC}
T_{CLCX}	Clock Low Time	3.2		T_{OSC}
T_{SLCH}, T_{SLCL}	SS# Low to Clock edge	200		ns
T_{IVCL}, T_{IVCH}	Input Data Valid to Clock Edge	100		ns
T_{CLIX}, T_{CHIX}	Input Data Hold after Clock Edge	100		ns
T_{CLOV}, T_{CHOV}	Output Data Valid after Clock Edge		100	ns
T_{CLOX}, T_{CHOX}	Output Data Hold Time after Clock Edge	0		ns
T_{CLSH}, T_{CHSH}	SS# High after Clock Edge	0		ns
T_{IVCL}, T_{IVCH}	Input Data Valid to Clock Edge	100		ns
T_{CLIX}, T_{CHIX}	Input Data Hold after Clock Edge	100		ns
T_{SLOV}	SS# Low to Output Data Valid		130	ns
T_{SHOX}	Output Data Hold after SS# High		130	ns
T_{SHSL}	SS# High to SS# Low	(2)		
T_{ILIH}	Input Rise Time		2	µs
T_{IHIL}	Input Fall Time		2	µs
T_{OLOH}	Output Rise time		100	ns
T_{OHOL}	Output Fall Time		100	ns
		Master Mode[3]		
T_{CHCH}	Clock Period	4		T_{OSC}
T_{CHCX}	Clock High Time	1.6		T_{OSC}
T_{CLCX}	Clock Low Time	1.6		T_{OSC}
T_{IVCL}, T_{IVCH}	Input Data Valid to Clock Edge	50		ns
T_{CLIX}, T_{CHIX}	Input Data Hold after Clock Edge	50		ns
T_{CLOV}, T_{CHOV}	Output Data Valid after Clock Edge		65	ns
T_{CLOX}, T_{CHOX}	Output Data Hold Time after Clock Edge	0		ns
T_{ILIH}	Input Data Rise Time		2	µs
T_{IHIL}	Input Data Fall Time		2	µs
T_{OLOH}	Output Data Rise time		50	ns
T_{OHOL}	Output Data Fall Time		50	ns

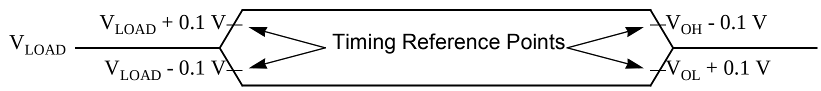
Notes:
1. Capacitive load on all pins = 200 pF in slave mode.
2. The value of this parameter depends on software.
3. Capacitive load on all pins = 100 pF in master mode.

Figure 26. AC Testing Input/Output Waveforms



Note: For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loading V_{OH}/V_{OL} level occurs with $I_{OL}/I_{OH} = \pm 20$ mA.

Figure 27. Float Waveforms



Low Voltage Versions - Commercial & Industrial

Table 56. DC Characteristics; V_{DD} = 2.7 to 5.5 V, T_A = -40 to +85°C

Symbol	Parameter	Min	Typical(4)	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (except EA#, SCL, SDA)	-0.5		$0.2 \cdot V_{DD}$ - 0.1	V	
V_{IL1}(5)	Input Low Voltage (SCL, SDA)	-0.5		$0.3 \cdot V_{DD}$	V	
V_{IL2}	Input Low Voltage (EA#)	0		$0.2 \cdot V_{DD}$ - 0.3	V	
V_{IH}	Input high Voltage (except XTAL1, RST, SCL, SDA)	$0.2 \cdot V_{DD}$ + 0.9		V_{DD} + 0.5	V	
V_{IH1}(5)	Input high Voltage (XTAL1, RST, SCL, SDA)	$0.7 \cdot V_{DD}$		V_{DD} + 0.5	V	
V_{OL}	Output Low Voltage (Ports 1, 2, 3)			0.45	V	I_{OL} = 0.8 mA(1)(2)
V_{OL1}	Output Low Voltage (Ports 0, ALE, PSEN#, Port 2 in Page Mode during External Address)			0.45	V	I_{OL} = 1.6 mA(1)(2)
V_{OH}	Output high Voltage (Ports 1, 2, 3, ALE, PSEN#)	$0.9 \cdot V_{DD}$			V	I_{OH} = -10 µA(3)
V_{OH1}	Output high Voltage (Port 0, Port 2 in Page Mode during External Address)	$0.9 \cdot V_{DD}$			V	I_{OH} = -40 µA
V_{RET}	V_{DD} data retention limit			1.8	V	
I_{IL0}	Logical 0 Input Current (Ports 1, 2, 3 - AWAIT#)			- 50	µA	V_{IN} = 0.45 V
I_{IL1}	Logical 1 Input Current (NMI)			+ 50	µA	$V_{IN} = V_{DD}$
I_{LI}	Input Leakage Current (Port 0)			± 10	µA	0.45 V < V_{IN} < V_{DD}
I_{TL}	Logical 1-to-0 Transition Current (Ports 1, 2, 3)			- 650	µA	V_{IN} = 2.0 V
R_{RST}	RST Pull-Down Resistor	40	110	225	kΩ	
C_{IO}	Pin Capacitance		10		pF	T_A = 25°C
I_{DD}	Operating Current		4 8 9 11	8 11 12 14	mA	5 MHz, V_{DD} < 3.6 V 10 MHz, V_{DD} < 3.6 V 12 MHz, V_{DD} < 3.6 V 16 MHz, V_{DD} < 3.6 V
I_{DL}	Idle Mode Current		0.5 1.5 2 3	1 4 5 7	mA	5 MHz, V_{DD} < 3.6 V 10 MHz, V_{DD} < 3.6 V 12 MHz, V_{DD} < 3.6 V 16 MHz, V_{DD} < 3.6 V
I_{PD}	Power-Down Current		1	10	µA	V_{RET} < V_{DD} < 3.6 V

Notes: 1. Under steady-state (non-transient) conditions, I_{OL} must be externally limited as follows:

Maximum IOL per port pin: 10 mA

Maximum IOL per 8-bit port: Port 0 26 mA

Ports 1-315 mA

CDIL 40 with Window - Mechanical Outline

Figure 34. Ceramic Dual In Line

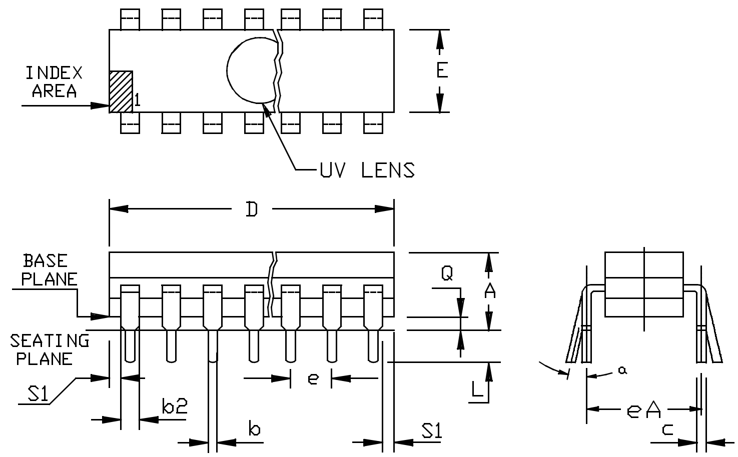


Table 58. CDIL Package Size

	MM		Inch	
	Min	Max	Min	Max
A	-	5.71	-	.225
b	0.36	0.58	.014	.023
b2	1.14	1.65	.045	.065
c	0.20	0.38	.008	.015
D	-	53.47	-	2.105
E	13.06	15.37	.514	.605
e	2.54 B.S.C.		.100 B.S.C.	
eA	15.24 B.S.C.		.600 B.S.C.	
L	3.18	5.08	.125	.200
Q	0.38	1.40	.015	.055
S1	0.13	-	.005	-
a	0 - 15		0 - 15	
N	40			

VQFP 44 (10x10) - Mechanical Outline

Figure 37. Shrink Quad Flat Pack (Plastic)

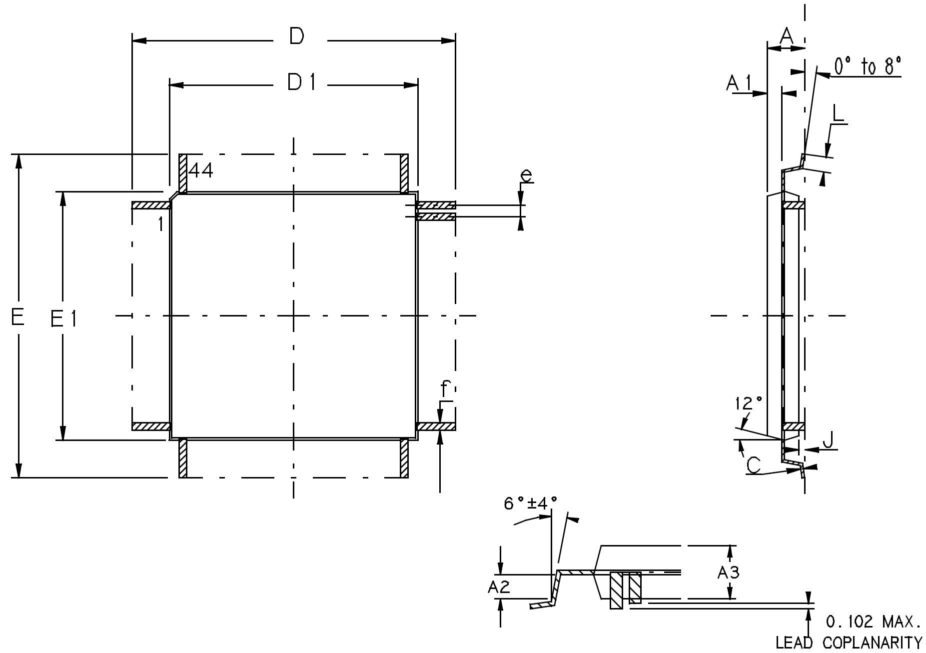


Table 61. VQFP Package Size

	MM		Inch	
	Min	Max	Min	Max
A	-	1.60	-	.063
A1	0.64 REF		.025 REF	
A2	0.64 REF		.025REF	
A3	1.35	1.45	.053	.057
D	11.90	12.10	.468	.476
D1	9.90	10.10	.390	.398
E	11.90	12.10	.468	.476
E1	9.90	10.10	.390	.398
J	0.05	-	.002	6
L	0.45	0.75	.018	.030
e	0.80 BSC		.0315 BSC	
f	0.35 BSC		.014 BSC	

AT/TSC87251G2D OTPROM

Part Number	ROM	Description
High Speed Versions 4.5 to 5.5 V, Commercial and Industrial		
TSC87251G2D-16CB	32K OTPROM	16 MHz, Commercial 0° to 70°C, PLCC 44
TSC87251G2D-24CB	32K OTPROM	24 MHz, Commercial 0° to 70°C, PLCC 44
TSC87251G2D-24CED	32K OTPROM	24 MHz, Commercial 0° to 70°C, VQFP 44
TSC87251G2D-24IA	32K OTPROM	24 MHz, Industrial -40° to 85°C, PDIL 40
TSC87251G2D-24IB	32K OTPROM	24 MHz, Industrial -40° to 85°C, PLCC 44
AT87251G2D-SLSUM	32K OTPROM	24 MHz, Industrial & Green -40° to 85°C, PLCC 44
AT87251G2D-3CSUM	32K OTPROM	24 MHz, Industrial & Green -40° to 85°C, PDIL 40
AT87251G2D-RLTUM	32K OTPROM	24 MHz, Industrial & Green -40° to 85°C, VQFP 44
Low Voltage Versions 2.7 to 5.5 V		
TSC87251G2D-L16CB	32K OTPROM	16 MHz, Commercial 0° to 70°C, PLCC 44
TSC87251G2D-L16CED	32K OTPROM	16 MHz, Commercial 0° to 70°C, VQFP 44
AT87251G2D-SLSUL	32K OTPROM	16 MHz, Industrial & Green, 0° to 70°C, PLCC 44
AT87251G2D-RLTUL	32K OTPROM	16 MHz, Industrial & Green, 0° to 70°C, VQFP 44

Document Revision History

Changes from 4135D to 4135E

1. Added automotive qualification, and ordering information for ROM product version.

Changes from 4135E to 4135F

1. Absolute Maximum Ratings added for automotive product version.