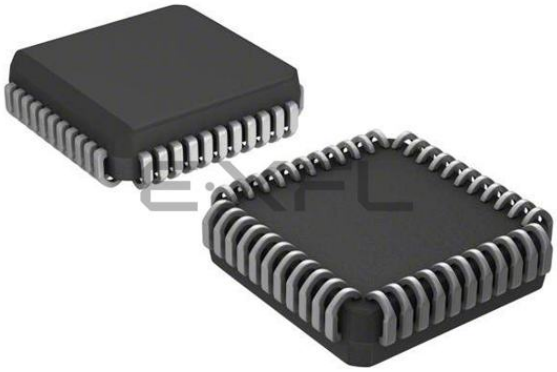

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C251
Core Size	8/16-Bit
Speed	16MHz
Connectivity	EBI/EMI, I²C, Microwire, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.6x16.6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at80251g2d-slsul

Block Diagram

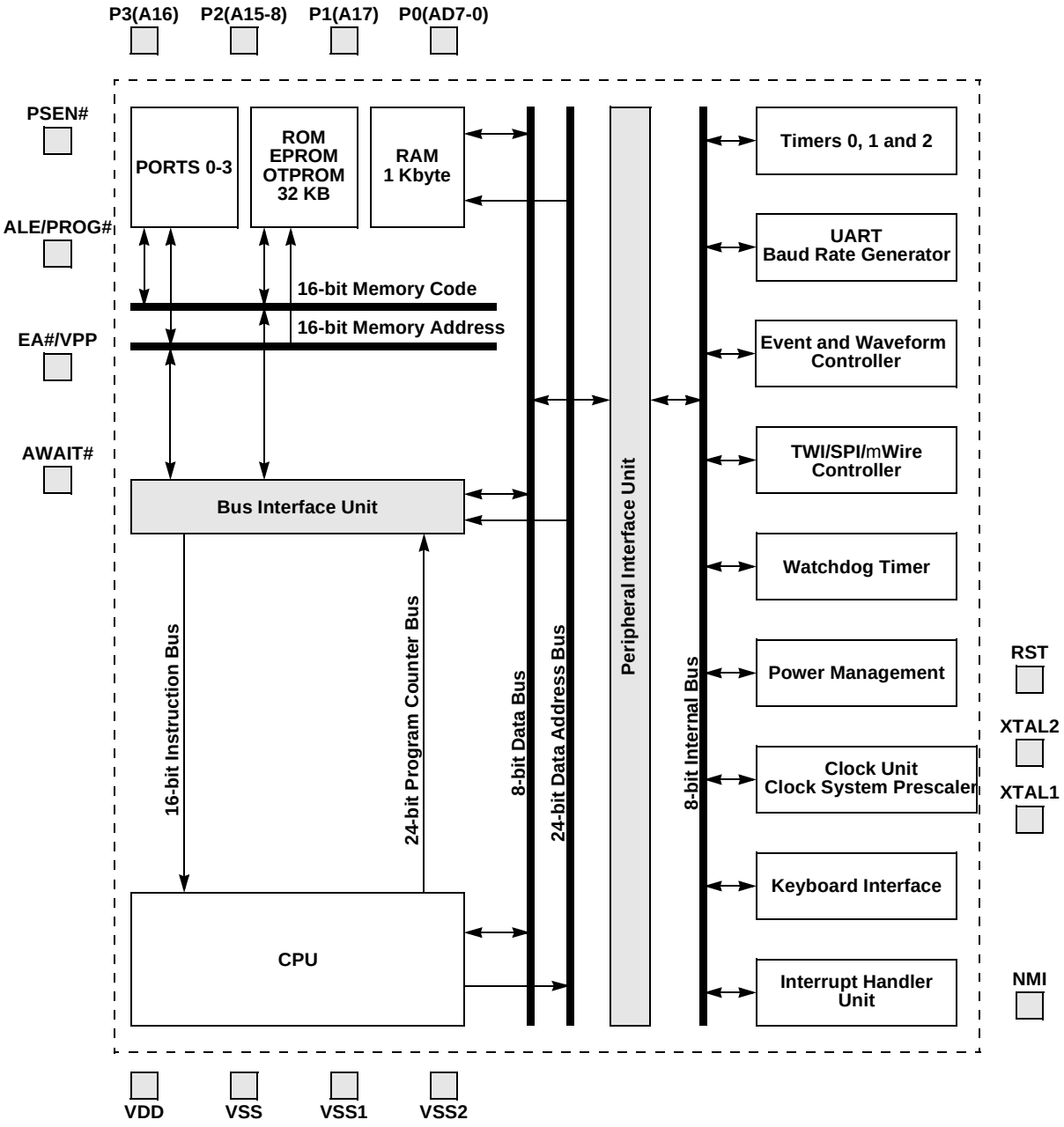


Table 2. Product Name Signal Description (Continued)

Signal Name	Type	Description	Alternate Function
NMI	I	**Non Maskable Interrupt** Holding this pin high for 24 oscillator periods triggers an interrupt. When using the Product Name as a pin-for-pin replacement for a 8xC51 product, NMI can be unconnected without loss of compatibility or power consumption increase (on-chip pull-down). Not available on DIP package.	–
P0.0:7	I/O	**Port 0** P0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. To avoid any paraitic current consumption, Floating P0 inputs must be polarized to V_{DD} or V_{SS}.	AD7:0
P1.0:7	I/O	**Port 1** P1 is an 8-bit bidirectional I/O port with internal pull-ups. P1 provides interrupt capability for a keyboard interface.	–
P2.0:7	I/O	**Port 2** P2 is an 8-bit bidirectional I/O port with internal pull-ups.	A15:8
P3.0:7	I/O	**Port 3** P3 is an 8-bit bidirectional I/O port with internal pull-ups.	–
PROG#	I	**Programming Pulse input** The programming pulse is applied to this input for programming the on-chip EPROM/OTPROM.	–
PSEN#	O	**Program Store Enable/Read signal output** PSEN# is asserted for a memory address range that depends on bits RD0 and RD1 in UCONFIG0 byte (see).	–
RD#	O	**Read or 17th Address Bit (A16)** Read signal output to external data memory depending on the values of bits RD0 and RD1 in UCONFIG0 byte (see Table 13, Page 20).	P3.7
RST	I	**Reset input to the chip** Holding this pin high for 64 oscillator periods while the oscillator is running resets the device. The Port pins are driven to their reset conditions when a voltage greater than V_{IH1} is applied, whether or not the oscillator is running. This pin has an internal pull-down resistor which allows the device to be reset by connecting a capacitor between this pin and VDD. Asserting RST when the chip is in Idle mode or Power-Down mode returns the chip to normal operation.	–
RXD	I/O	**Receive Serial Data** RXD sends and receives data in serial I/O mode 0 and receives data in serial I/O modes 1, 2 and 3.	P3.0
SCL	I/O	**TWI Serial Clock** When TWI controller is in master mode, SCL outputs the serial clock to slave peripherals. When TWI controller is in slave mode, SCL receives clock from the master controller.	P1.6
SCK	I/O	**SPI Serial Clock** When SPI is in master mode, SCK outputs clock to the slave peripheral. When SPI is in slave mode, SCK receives clock from the master controller.	P1.6
SDA	I/O	**TWI Serial Data** SDA is the bidirectional TWI data line.	P1.7
SS#	I	**SPI Slave Select Input** When in Slave mode, SS# enables the slave mode.	P1.4

Table 2. Product Name Signal Description (Continued)

Signal Name	Type	Description	Alternate Function
T1:0	I/O	**Timer 1:0 External Clock Inputs** When timer 1:0 operates as a counter, a falling edge on the T1:0 pin increments the count.	–
T2	I/O	**Timer 2 Clock Input/Output** For the timer 2 capture mode, T2 is the external clock input. For the Timer 2 clock-out mode, T2 is the clock output.	P1.0
T2EX	I	**Timer 2 External Input** In timer 2 capture mode, a falling edge initiates a capture of the timer 2 registers. In auto-reload mode, a falling edge causes the timer 2 register to be reloaded. In the up-down counter mode, this signal determines the count direction: 1 = up, 0 = down.	P1.1
TXD	O	**Transmit Serial Data** TXD outputs the shift clock in serial I/O mode 0 and transmits data in serial I/O modes 1, 2 and 3.	P3.1
VDD	PWR	**Digital Supply Voltage** Connect this pin to +5V or +3V supply voltage.	–
VPP	I	**Programming Supply Voltage** The programming supply voltage is applied to this input for programming the on-chip EPROM/OTPROM.	–
VSS	GND	**Circuit Ground** Connect this pin to ground.	–
VSS1	GND	**Secondary Ground 1** This ground is provided to reduce ground bounce and improve power supply bypassing. Connection of this pin to ground is recommended. However, when using the TSC80251G2D as a pin-for-pin replacement for a 8xC51 product, VSS1 can be unconnected without loss of compatibility. Not available on DIP package.	–
VSS2	GND	**Secondary Ground 2** This ground is provided to reduce ground bounce and improve power supply bypassing. Connection of this pin to ground is recommended. However, when using the TSC80251G2D as a pin-for-pin replacement for a 8xC51 product, VSS2 can be unconnected without loss of compatibility. Not available on DIP package.	–
WAIT#	I	**Real-time Synchronous Wait States Input** The real-time WAIT# input is enabled by setting RTWE bit in WCON (S:A7h). During bus cycles, the external memory system can signal 'system ready' to the microcontroller in real time by controlling the WAIT# input signal.	P1.6
WCLK	O	**Wait Clock Output** The real-time WCLK output is enabled by setting RTWCE bit in WCON (S:A7h). When enabled, the WCLK output produces a square wave signal with a period of one half the oscillator frequency.	P1.7
WR#	O	**Write** Write signal output to external memory.	P3.6
XTAL1	I	**Input to the on-chip inverting oscillator amplifier** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, its output is connected to this pin. XTAL1 is the clock source for internal timing.	–

Table 11. Configuration Byte 0
UCONFIG0

7	6	5	4	3	2	1	0
-	WSA1#	WSA0#	XALE#	RD1	RD0	PAGE#	SRC

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** Set this bit when writing to UCONFIG0.
6	WSA1#	**Wait State A bits** Select the number of wait states for RD#, WR# and PSEN# signals for external memory accesses (all regions except 01:). WSA1# WSA0# Number of Wait States 0 0 3 0 1 2 1 0 1 1 1 0
5	WSA0#	
4	XALE#	**Extend ALE bit** Clear to extend the duration of the ALE pulse from T_{OSC} to $3 \cdot T_{OSC}$. Set to minimize the duration of the ALE pulse to $1 \cdot T_{OSC}$.
3	RD1	**Memory Signal Select bits** Specify a 18-bit, 17-bit or 16-bit external address bus and the usage of RD#, WR# and PSEN# signals (see Table 13).
2	RD0	
1	PAGE#	**Page Mode Select bit**(1) Clear to select the faster Page mode with A15:8/D7:0 on Port 2 and A7:0 on Port 0. Set to select the non-Page mode(2) with A15:8 on Port 2 and A7:0/D7:0 on Port 0.
0	SRC	**Source Mode/Binary Mode Select bit** Clear to select the binary mode. Set to select the source mode.

Notes: 1. UCONFIG0 is fetched twice so it can be properly read both in Page or Non-Page modes. If P2.1 is cleared during the first data fetch, a Page mode configuration is used, otherwise the subsequent fetches are performed in Non-Page mode.
2. This selection provides compatibility with the standard 80C51 hardware which is multiplexing the address LSB and the data on Port 0.

Table 22. Summary of Compare Instructions

CompareCMP <dest>, <src>dest opnd - src opnd						
			Binary Mode		Source Mode	
Mnemonic	**<dest>, <src>(2)**	**Comments**	**Bytes**	**States**	**Bytes**	**States**
CMP	Rmd, Rms	Register with register	3	2	2	1
	WRjd, WRjs	Word register with word register	3	3	2	2
	DRkd, DRks	Dword register with dword register	3	5	2	4
	Rm, #data	Register with immediate data	4	3	3	2
	WRj, #data16	Word register with immediate 16-bit data	5	4	4	3
	DRk, #0data16	Dword register with zero-extended 16-bit immediate data	5	6	4	5
	DRk, #1data16	Dword register with one-extended 16-bit immediate data	5	6	4	5
	Rm, dir8	Direct address (on-chip RAM or SFR) with byte register	4	3(1)	3	2(1)
	WRj, dir8	Direct address (on-chip RAM or SFR) with word register	4	4	3	3
	Rm, dir16	Direct address (64K) with byte register	5	3(2)	4	2(2)
	WRj, dir16	Direct address (64K) with word register	5	4(3)	4	3(3)
	Rm, at WRj	Indirect address (64K) with byte register	4	3(2)	3	2(2)
	Rm, at DRk	Indirect address (16M) with byte register	4	4(2)	3	3(2)

Notes:
1. If this instruction addresses an I/O Port (Px, x = 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.
2. If this instruction addresses external memory location, add N+2 to the number of states (N: number of wait states).
3. If this instruction addresses external memory location, add 2(N+2) to the number of states (N: number of wait states).

Notes: 1. Logical instructions that affect a bit are in Table 27.
2. A shaded cell denotes an instruction in the C51 Architecture.
3. If this instruction addresses an I/O Port (Px, x = 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.
4. If this instruction addresses an I/O Port (Px, x = 0-3), add 2 to the number of states. Add 3 if it addresses a Peripheral SFR.
5. If this instruction addresses external memory location, add N+2 to the number of states (N: number of wait states).
6. If this instruction addresses external memory location, add 2(N+2) to the number of states (N: number of wait states).

Table 23. Summary of Logical Instructions (2/2)

Shift Left LogicalSLL <dest><dest>$_0 \leftarrow 0$
<dest>$_{n+1} \leftarrow$ <dest>$_n$, n = 0..msb-1
(CY) $\leftarrow$ <dest>$_{msb}$
Shift Right ArithmeticSRA <dest><dest>$_{msb} \leftarrow$ <dest>$_{msb}$
<dest>$_{n-1} \leftarrow$ <dest>$_n$, n = msb..1
(CY) $\leftarrow$ <dest>$_0$
Shift Right LogicalSRL <dest><dest>$_{msb} \leftarrow 0$
<dest>$_{n-1} \leftarrow$ <dest>$_n$, n = msb..1
(CY) $\leftarrow$ <dest>$_0$
SwapSWAP $AA_{3:0}$ $A_{7:4}$

Mnemonic	<dest>, <src>(1)	Comments	Binary Mode		Source Mode	
			Bytes	States	Bytes	States
SLL	Rm	Shift byte register left through the MSB	3	2	2	1
	WRj	Shift word register left through the MSB	3	2	2	1
SRA	Rm	Shift byte register right	3	2	2	1
	WRj	Shift word register right	3	2	2	1
SRL	Rm	Shift byte register left	3	2	2	1
	WRj	Shift word register left	3	2	2	1
SWAP	A	Swap nibbles within ACC	1	2	1	2

Note: 1. A shaded cell denotes an instruction in the C51 Architecture.

Move[1] MOV <dest>, <src> dest opnd ← src opnd						
			Binary Mode		Source Mode	
Mnemonic	<dest>, <src>[1]	Comments	Bytes	States	Bytes	States
MOV	Rmd, Rms	Byte register to byte register	3	2	2	1
MOV	WRjd, WRjs	Word register to word register	3	2	2	1
MOV	DRkd, DRks	Dword register to dword register	3	3	2	2
MOV	Rm, #data	Immediate 8-bit data to byte register	4	3	3	2
MOV	WRj, #data16	Immediate 16-bit data to word register	5	3	4	2
MOV	DRk, #0data16	zero-ext 16bit immediate data to dword register	5	5	4	4
MOV	DRk, #1data16	one-ext 16bit immediate data to dword register	5	5	4	4
MOV	Rm, dir8	Direct address (on-chip RAM or SFR) to byte register	4	3[3]	3	2[3]
MOV	WRj, dir8	Direct address (on-chip RAM or SFR) to word register	4	4	3	3
MOV	DRk, dir8	Direct address (on-chip RAM or SFR) to dword register	4	6	3	5
MOV	Rm, dir16	Direct address (64K) to byte register	5	3[4]	4	2[4]
MOV	WRj, dir16	Direct address (64K) to word register	5	4[5]	4	3[5]
MOV	DRk, dir16	Direct address (64K) to dword register	5	6[6]	4	5[6]
MOV	Rm, at WRj	Indirect address (64K) to byte register	4	3[4]	3	2[4]
MOV	Rm, at DRk	Indirect address (16M) to byte register	4	4[4]	3	3[4]
MOV	WRjd, at WRjs	Indirect address (64K) to word register	4	4[5]	3	3[5]
MOV	WRj, at DRk	Indirect address (16M) to word register	4	5[5]	3	4[5]
MOV	dir8, Rm	Byte register to direct address (on-chip RAM or SFR)	4	4[3]	3	3[3]
MOV	dir8, WRj	Word register to direct address (on-chip RAM or SFR)	4	5	3	4
MOV	dir8, DRk	Dword register to direct address (on-chip RAM or SFR)	4	7	3	6
MOV	dir16, Rm	Byte register to direct address (64K)	5	4[4]	4	3[4]
MOV	dir16, WRj	Word register to direct address (64K)	5	5[5]	4	4[5]
MOV	dir16, DRk	Dword register to direct address (64K)	5	7[6]	4	6[6]
MOV	at WRj, Rm	Byte register to indirect address (64K)	4	4[4]	3	3[4]
MOV	at DRk, Rm	Byte register to indirect address (16M)	4	5[4]	3	4[4]
MOV	at WRjd, WRjs	Word register to indirect address (64K)	4	5[5]	3	4[5]
MOV	at DRk, WRj	Word register to indirect address (16M)	4	6[5]	3	5[5]
MOV	Rm, at WRj +dis16	Indirect with 16-bit displacement (64K) to byte register	5	6[4]	4	5[4]
MOV	WRj, at WRj +dis16	Indirect with 16-bit displacement (64K) to word register	5	7[5]	4	6[5]
MOV	Rm, at DRk +dis24	Indirect with 16-bit displacement (16M) to byte register	5	7[4]	4	6[4]

Table 32. Summary of Call and Return Instructions

Absolute callACALL <src>(PC) ← (PC) +2; push $(PC)_{15:0}$;
$(PC)_{10:0}$ ← src opnd
Extended callECALL <src>(PC) ← (PC) + size (instr); push $(PC)_{23:0}$;
$(PC)_{23:0}$ ← src opnd
Long callLCALL <src>(PC) ← (PC) + size (instr); push $(PC)_{15:0}$;
$(PC)_{15:0}$ ← src opnd
Return from subroutineRETpop $(PC)_{15:0}$
Extended return from subroutineERETpop $(PC)_{23:0}$
Return from interruptRETIIF [INTR = 0] THEN pop $(PC)_{15:0}$
IF [INTR = 1] THEN pop $(PC)_{23:0}$; pop (PSW1)
Trap interruptTRAP(PC) ← (PC) + size (instr);
IF [INTR = 0] THEN push $(PC)_{15:0}$
IF [INTR = 1] THEN push (PSW1); push $(PC)_{23:0}$

Mnemonic	<dest>, <src>(1)	Comments	Binary Mode		Source Mode	
			Bytes	States	Bytes	States
ACALL	addr11	Absolute subroutine call	2	9(2)(3)	2	9(2)(3)
ECALL	at DRk	Extended subroutine call (indirect)	3	14(2)(3)	2	13(2)(3)
	addr24	Extended subroutine call	5	14(2)(3)	4	13(2)(3)
LCALL	at WRj	Long subroutine call (indirect)	3	10(2)(3)	2	9(2)(3)
	addr16	Long subroutine call	3	9(2)(3)	3	9(2)(3)
RET		Return from subroutine	1	7(2)	1	7(2)
ERET		Extended subroutine return	3	9(2)	2	8(2)
RETI		Return from interrupt	1	7(2)(4)	1	7(2)(4)
TRAP		Jump to the trap interrupt vector	2	12(4)	1	11(4)

Notes:
1. A shaded cell denotes an instruction in the C51 Architecture.
2. In internal execution only, add 1 to the number of states if the destination/return address is internal and odd.
3. Add 2 to the number of states if the destination address is external.
4. Add 5 to the number of states if INTR = 1.

AC Characteristics - Commercial & Industrial

AC Characteristics - External Bus Cycles

Definition of Symbols

Table 38. External Bus Cycles Timing Symbol Definitions

Signals	
A	Address
D	Data In
L	ALE
Q	Data Out
R	RD#/PSEN#
W	WR#

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid
Z	Floating

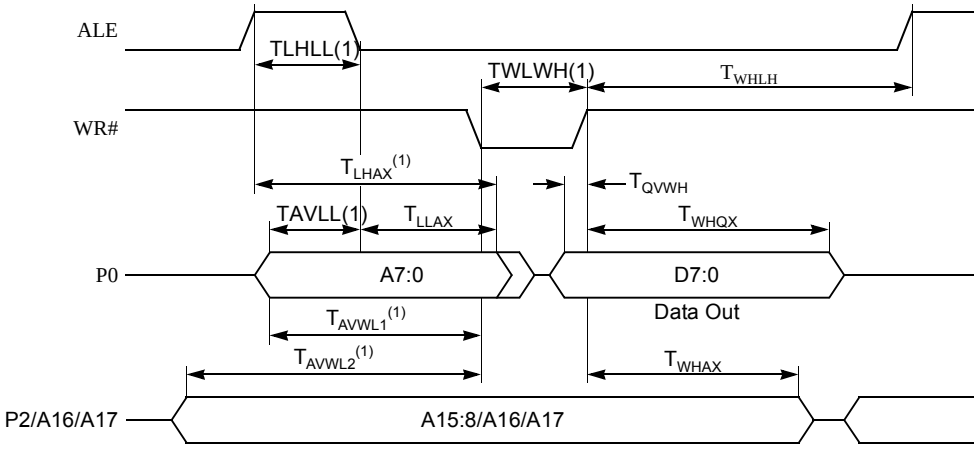
Timings

Test conditions: capacitive load on all pins = 50 pF.

Table 39 and Table 40 list the AC timing parameters for the TSC80251G2D derivatives with no wait states. External wait states can be added by extending PSEN#/RD#/WR# and or by extending ALE. In these tables, Note 2 marks parameters affected by one ALE wait state, and Note 3 marks parameters affected by PSEN#/RD#/WR# wait states.

Figure 8 to Figure 13 show the bus cycles with the timing parameters.

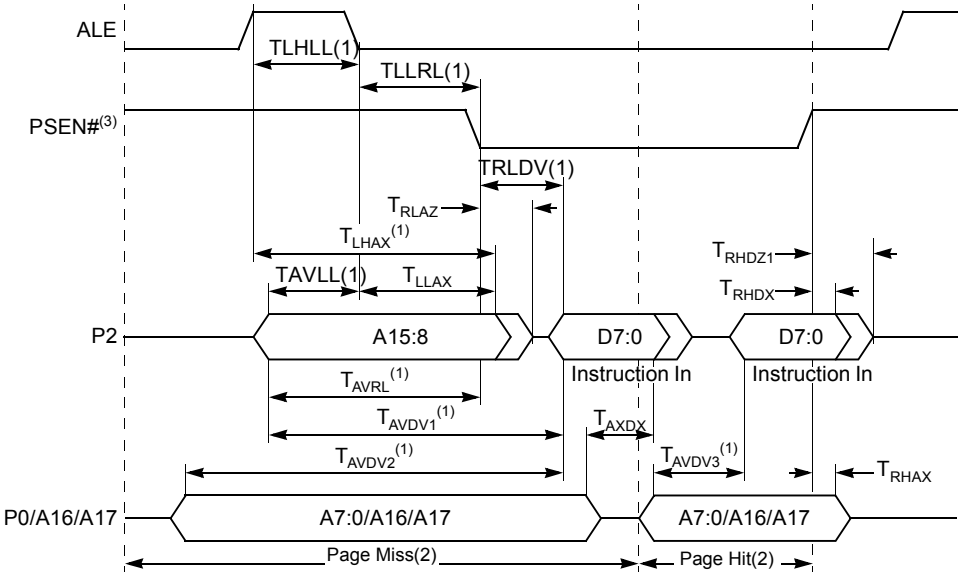
Figure 10. External Bus Cycle: Data Write (Non-Page Mode)



Note: 1. The value of this parameter depends on wait states. See Table 39 and Table 40.

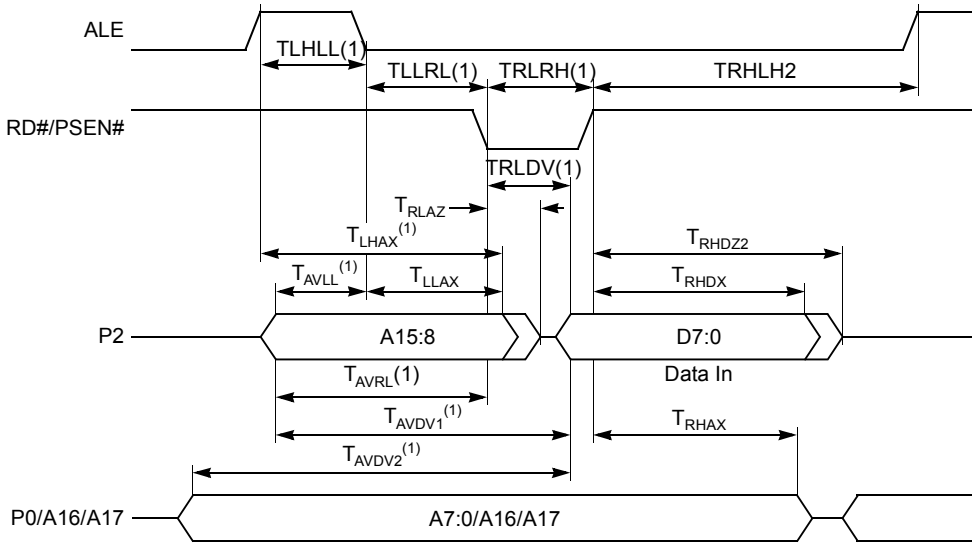
Waveforms in Page Mode

Figure 11. External Bus Cycle: Code Fetch (Page Mode)



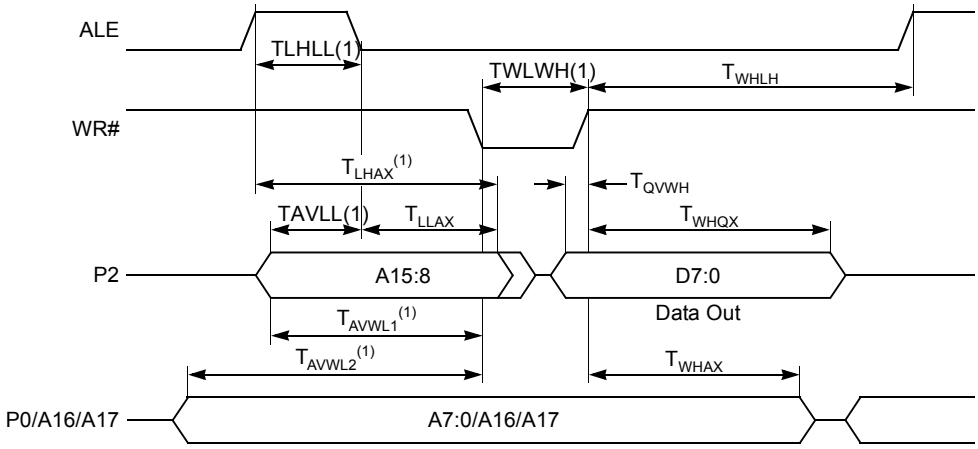
Note: 1. The value of this parameter depends on wait states. See Table 39 and Table 40.
2. A page hit (i.e., a code fetch to the same 256-byte “page” as the previous code fetch) requires one state ($2 \cdot T_{OSC}$);
a page miss requires two states ($4 \cdot T_{OSC}$).
3. During a sequence of page hits, PSEN# remains low until the end of the last page-hit cycle.

Figure 12. External Bus Cycle: Data Read (Page Mode)



Note: 1. The value of this parameter depends on wait states. See Table 39 and Table 40.

Figure 13. External Bus Cycle: Data Write (Page Mode)



Note: 1. The value of this parameter depends on wait states. See Table 39 and Table 40.

AC Characteristics - Real-Time Synchronous Wait State

Definition of Symbols

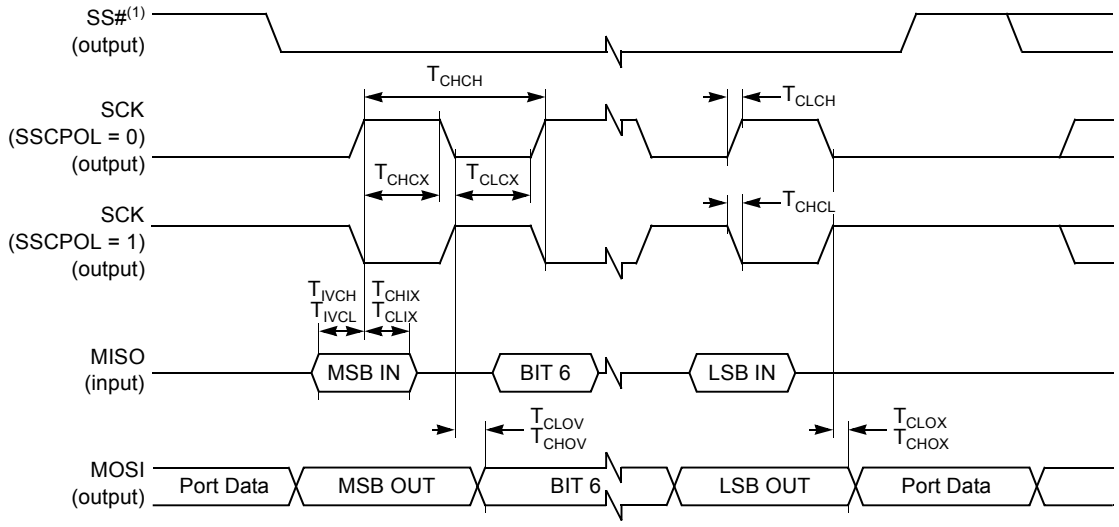
Table 41. Real-Time Synchronous Wait Timing Symbol Definitions

Signals	
C	WCLK
R	RD#/PSEN#
W	WR#
Y	WAIT#

Conditions	
L	Low
V	Valid
X	No Longer Valid

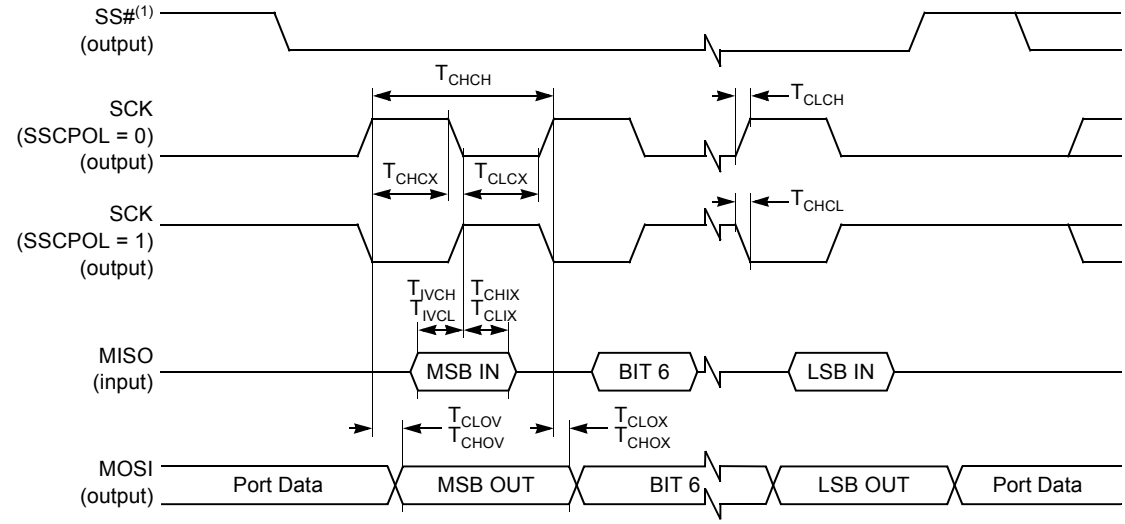
Waveforms

Figure 19. SPI Master Waveforms (SSCPHA = 0)



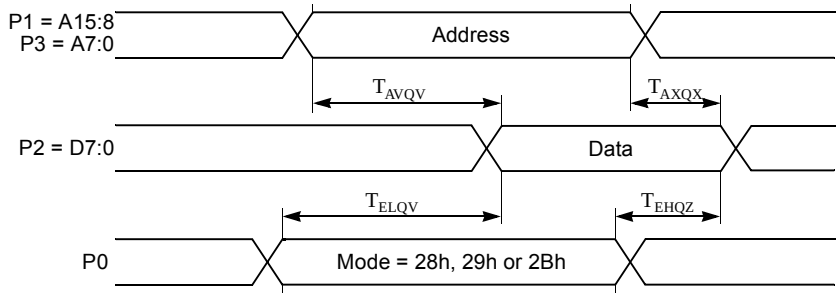
Note: 1. SS# handled by software.

Figure 20. SPI Master Waveforms (SSCPHA = 1)



Note: 1. Not Defined but normally MSB of character just received.

Figure 24. EPROM Verifying Waveforms



AC Characteristics - External Clock Drive and Logic Level References

Definition of Symbols

Table 53. External Clock Timing Symbol Definitions

Signals	
C	Clock

Conditions	
H	High
L	Low
X	No Longer Valid

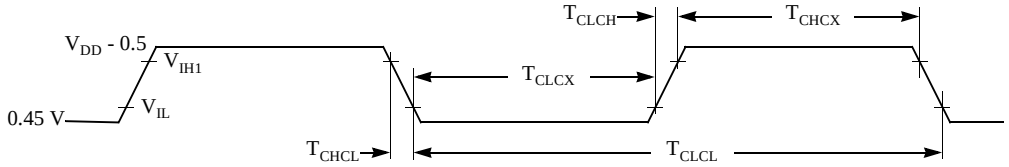
Timings

Table 54. External Clock AC Timings; V_{DD} = 4.5 to 5.5 V, T_A = -40 to +85°C

Symbol	Parameter	Min	Max	Unit
F_{OSC}	Oscillator Frequency		24	MHz
T_{CHCX}	High Time	10		ns
T_{CLCX}	Low Time	10		ns
T_{CLCH}	Rise Time	3		ns
T_{CHCL}	Fall Time	3		ns

Waveforms

Figure 25. External Clock Waveform



Notes: 1. During AC testing, all inputs are driven at V_{DD} -0.5 V for a logic 1 and 0.45 V for a logic 0.
2. Timing measurements are made on all outputs at V_{IH} min for a logic 1 and V_{IL} max for a logic 0.

DC Characteristics

High Speed Versions - Commercial, Industrial, and Automotive

Table 55. DC Characteristics; V_{DD} = 4.5 to 5.5 V, T_A = -40 to +85°C

Symbol	Parameter	Min	Typical[4]	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (except EA#, SCL, SDA)	-0.5		$0.2 \cdot V_{DD}$ - 0.1	V	
V_{IL1}[5]	Input Low Voltage (SCL, SDA)	-0.5		$0.3 \cdot V_{DD}$	V	
V_{IL2}	Input Low Voltage (EA#)	0		$0.2 \cdot V_{DD}$ - 0.3	V	
V_{IH}	Input high Voltage (except XTAL1, RST, SCL, SDA)	$0.2 \cdot V_{DD}$ + 0.9		V_{DD} + 0.5	V	
V_{IH1}[5]	Input high Voltage (XTAL1, RST, SCL, SDA)	$0.7 \cdot V_{DD}$		V_{DD} + 0.5	V	
V_{OL}	Output Low Voltage (Ports 1, 2, 3)			0.3 0.45 1.0	V	I_{OL} = 100 µA[1][2] I_{OL} = 1.6 mA[1][2] I_{OL} = 3.5 mA[1][2]
V_{OL1}	Output Low Voltage (Ports 0, ALE, PSEN#, Port 2 in Page Mode during External Address)			0.3 0.45 1.0	V	I_{OL} = 200 µA[1][2] I_{OL} = 3.2 mA[1][2] I_{OL} = 7.0 mA[1][2]
V_{OH}	Output high Voltage (Ports 1, 2, 3, ALE, PSEN#)	V_{DD} - 0.3 V_{DD} - 0.7 V_{DD} - 1.5			V	I_{OH} = -10 µA[3] I_{OH} = -30 µA[3] I_{OH} = -60 µA[3]
V_{OH1}	Output high Voltage (Port 0, Port 2 in Page Mode during External Address)	V_{DD} - 0.3 V_{DD} - 0.7 V_{DD} - 1.5			V	I_{OH} = -200 µA I_{OH} = -3.2 mA I_{OH} = -7.0 mA
V_{RET}	V_{DD} data retention limit			1.8	V	
I_{IL0}	Logical 0 Input Current (Ports 1, 2, 3)			- 50	µA	V_{IN} = 0.45 V
I_{IL1}	Logical 1 Input Current (NMI)			+ 50	µA	V_{IN} = V_{DD}
I_{LI}	Input Leakage Current (Port 0)			± 10	µA	0.45 V < V_{IN} < V_{DD}
I_{TL}	Logical 1-to-0 Transition Current (Ports 1, 2, 3 - AWAIT#)			- 650	µA	V_{IN} = 2.0 V
R_{RST}	RST Pull-Down Resistor	40	110	225	kΩ	
C_{IO}	Pin Capacitance		10		pF	T_A = 25°C
I_{DD}	Operating Current		20 25 35	25 30 40	mA	F_{OSC} = 12 MHz F_{OSC} = 16 MHz F_{OSC} = 24 MHz
I_{DL}	Idle Mode Current		5 6.5 9.5	8 10 14	mA	F_{OSC} = 12 MHz F_{OSC} = 16 MHz F_{OSC} = 24 MHz
I_{PD}	Power-Down Current		2	20	µA	V_{RET} < V_{DD} < 5.5 V
V_{PP}	Programming supply voltage	12.5		13	V	T_A = 0 to +40°C
I_{PP}	Programming supply current			75	mA	T_A = 0 to +40°C

Low Voltage Versions - Commercial & Industrial

Table 56. DC Characteristics; V_{DD} = 2.7 to 5.5 V, T_A = -40 to +85°C

Symbol	Parameter	Min	Typical[4]	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (except EA#, SCL, SDA)	-0.5		$0.2 \cdot V_{DD}$ - 0.1	V	
V_{IL1}[5]	Input Low Voltage (SCL, SDA)	-0.5		$0.3 \cdot V_{DD}$	V	
V_{IL2}	Input Low Voltage (EA#)	0		$0.2 \cdot V_{DD}$ - 0.3	V	
V_{IH}	Input high Voltage (except XTAL1, RST, SCL, SDA)	$0.2 \cdot V_{DD}$ + 0.9		V_{DD} + 0.5	V	
V_{IH1}[5]	Input high Voltage (XTAL1, RST, SCL, SDA)	$0.7 \cdot V_{DD}$		V_{DD} + 0.5	V	
V_{OL}	Output Low Voltage (Ports 1, 2, 3)			0.45	V	I_{OL} = 0.8 mA[1][2]
V_{OL1}	Output Low Voltage (Ports 0, ALE, PSEN#, Port 2 in Page Mode during External Address)			0.45	V	I_{OL} = 1.6 mA[1][2]
V_{OH}	Output high Voltage (Ports 1, 2, 3, ALE, PSEN#)	$0.9 \cdot V_{DD}$			V	I_{OH} = -10 µA[3]
V_{OH1}	Output high Voltage (Port 0, Port 2 in Page Mode during External Address)	$0.9 \cdot V_{DD}$			V	I_{OH} = -40 µA
V_{RET}	V_{DD} data retention limit			1.8	V	
I_{IL0}	Logical 0 Input Current (Ports 1, 2, 3 - AWAIT#)			- 50	µA	V_{IN} = 0.45 V
I_{IL1}	Logical 1 Input Current (NMI)			+ 50	µA	$V_{IN} = V_{DD}$
I_{LI}	Input Leakage Current (Port 0)			± 10	µA	0.45 V < V_{IN} < V_{DD}
I_{TL}	Logical 1-to-0 Transition Current (Ports 1, 2, 3)			- 650	µA	V_{IN} = 2.0 V
R_{RST}	RST Pull-Down Resistor	40	110	225	kΩ	
C_{IO}	Pin Capacitance		10		pF	T_A = 25°C
I_{DD}	Operating Current		4 8 9 11	8 11 12 14	mA	5 MHz, V_{DD} < 3.6 V 10 MHz, V_{DD} < 3.6 V 12 MHz, V_{DD} < 3.6 V 16 MHz, V_{DD} < 3.6 V
I_{DL}	Idle Mode Current		0.5 1.5 2 3	1 4 5 7	mA	5 MHz, V_{DD} < 3.6 V 10 MHz, V_{DD} < 3.6 V 12 MHz, V_{DD} < 3.6 V 16 MHz, V_{DD} < 3.6 V
I_{PD}	Power-Down Current		1	10	µA	V_{RET} < V_{DD} < 3.6 V

Notes: 1. Under steady-state (non-transient) conditions, I_{OL} must be externally limited as follows:

Maximum IOL per port pin: 10 mA

Maximum IOL per 8-bit port: Port 0 26 mA

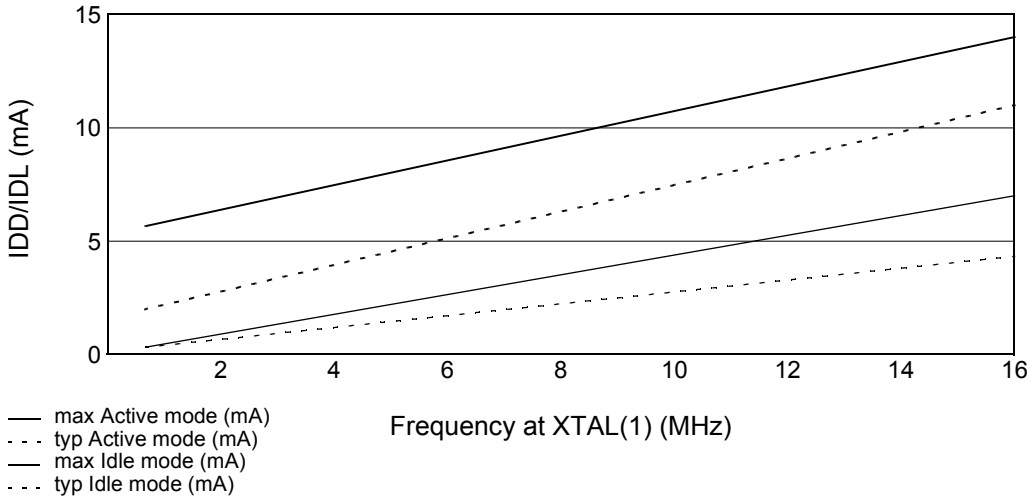
Ports 1-315 mA

Maximum Total IOL for all:Output Pins71 mA

If IOL exceeds the test conditions, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

2. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses above 0.4 V on the low-level outputs of ALE and Ports 1, 2, and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from high to low. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8 V. It may be desirable to qualify ALE or other signals with a Schmitt Trigger or CMOS-level input logic.
3. Capacitive loading on Ports 0 and 2 causes the V_{OH} on ALE and PSEN# to drop below the specification when the address lines are stabilizing.
4. Typical values are obtained using V_{DD} = 3 V and T_A = 25°C. They are not tested and there is not guarantee on these values.
5. The input threshold voltage of SCL and SDA meets the TWI specification, so an input voltage below $0.3 \cdot V_{DD}$ will be recognized as a logic 0 while an input voltage above $0.7 \cdot V_{DD}$ will be recognized as a logic 1.

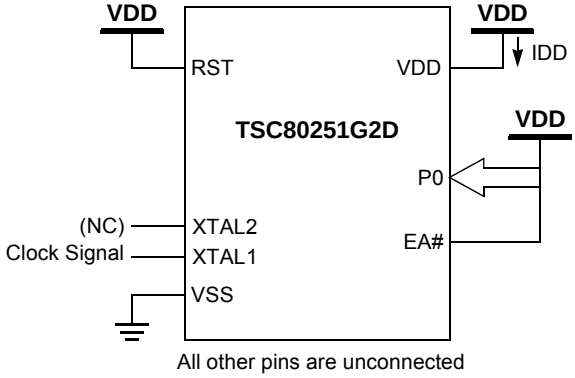
Figure 29. I_{DD}/I_{DL} Versus X_{TAL} Frequency; V_{DD} = 2.7 to 3.6 V



Note: 1.The clock prescaler is not used: $F_{OSC} = F_{XTAL}$.

I_{DD}, I_{DL} and I_{PD} Test Conditions

Figure 30. I_{DD} Test Condition, Active Mode



PLCC 44 - Mechanical Outline

Figure 35. Plastic Lead Chip Carrier

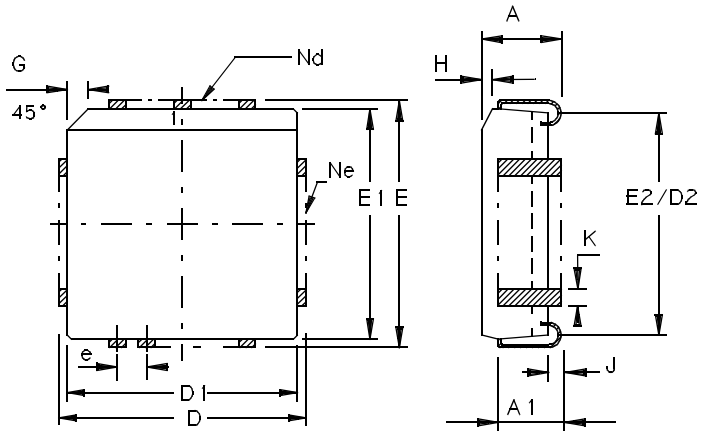


Table 59. PLCC Package Size

	MM		Inch	
	Min	**Max**	**Min**	**Max**
A	4.20	4.57	.165	.180
A1	2.29	3.04	.090	.120
D	17.40	17.65	.685	.695
D1	16.44	16.66	.647	.656
D2	14.99	16.00	.590	.630
E	17.40	17.65	.685	.695
E1	16.44	16.66	.647	.656
E2	14.99	16.00	.590	.630
e	1.27 BSC		.050 BSC	
G	1.07	1.22	.042	.048
H	1.07	1.42	.042	.056
J	0.51	-	.020	-
K	0.33	0.53	.013	.021
Nd	11		11	
Ne	11		11	

Part Number[1]	ROM	Description
Low Voltage Versions 2.7 to 5.5 V		
TSC251G2Dxxx-L16CB	32K MaskROM	16 MHz, Commercial 0° to 70°C, PLCC 44
TSC251G2Dxxx-L16CE	32K MaskROM	16 MHz, Commercial 0° to 70°C, VQFP 44
AT251G2Dxxx-SLSUL	32K MaskROM	16 MHz, Industrial & Green, PLCC 44
AT251G2Dxxx-RLTUL	32K MaskROM	16 MHz, Industrial & Green, VQFP 44

Note: 1. xxx: means ROM code, is Cxxx in case of encrypted code.

AT/TSC87251G2D OTPROM

Part Number	ROM	Description
High Speed Versions 4.5 to 5.5 V, Commercial and Industrial		
TSC87251G2D-16CB	32K OTPROM	16 MHz, Commercial 0° to 70°C, PLCC 44
TSC87251G2D-24CB	32K OTPROM	24 MHz, Commercial 0° to 70°C, PLCC 44
TSC87251G2D-24CED	32K OTPROM	24 MHz, Commercial 0° to 70°C, VQFP 44
TSC87251G2D-24IA	32K OTPROM	24 MHz, Industrial -40° to 85°C, PDIL 40
TSC87251G2D-24IB	32K OTPROM	24 MHz, Industrial -40° to 85°C, PLCC 44
AT87251G2D-SLSUM	32K OTPROM	24 MHz, Industrial & Green -40° to 85°C, PLCC 44
AT87251G2D-3CSUM	32K OTPROM	24 MHz, Industrial & Green -40° to 85°C, PDIL 40
AT87251G2D-RLTUM	32K OTPROM	24 MHz, Industrial & Green -40° to 85°C, VQFP 44
Low Voltage Versions 2.7 to 5.5 V		
TSC87251G2D-L16CB	32K OTPROM	16 MHz, Commercial 0° to 70°C, PLCC 44
TSC87251G2D-L16CED	32K OTPROM	16 MHz, Commercial 0° to 70°C, VQFP 44
AT87251G2D-SLSUL	32K OTPROM	16 MHz, Industrial & Green, 0° to 70°C, PLCC 44
AT87251G2D-RLTUL	32K OTPROM	16 MHz, Industrial & Green, 0° to 70°C, VQFP 44

Document Revision History

Changes from 4135D to 4135E

1. Added automotive qualification, and ordering information for ROM product version.

Changes from 4135E to 4135F

1. Absolute Maximum Ratings added for automotive product version.

Options (Please consult Atmel sales)

- ROM code encryption
- Tape & Reel or Dry Pack
- Known good dice
- Extended temperature range: -55°C to +125°C

Product Markings

ROMless versions

ATMEL
Part number

YYWW . Lot Number

Mask ROM versions

ATMEL
Customer Part number

Part Number
YYWW . Lot Number

OTP versions

ATMEL
Part number

YYWW . Lot Number