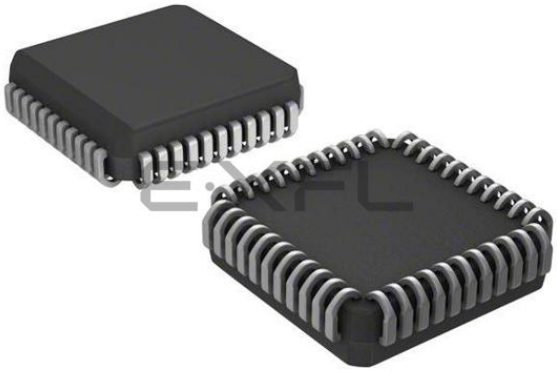


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C251
Core Size	8/16-Bit
Speed	24MHz
Connectivity	EBI/EMI, I²C, Microwire, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.6x16.6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at80251g2d-slsum

- **Typical Operating Current:11 mA at 3V**
- **Typical Power-down Current: 1 µA**
- **Temperature Ranges: Commercial (0°C to +70°C), Industrial (-40°C to +85°C), Automotive ((-40°C to +85°C) ROM only)**
- **Option: Extended Range (-55°C to +125°C)**
- **Packages: PDIL 40, PLCC 44 and VQFP 44**
- **Options: Known Good Dice and Ceramic Packages**

Description

The TSC80251G2D products are derivatives of the Atmel Microcontroller family based on the 8/16-bit C251 Architecture. This family of products is tailored to 8/16-bit microcontroller applications requiring an increased instruction throughput, a reduced operating frequency or a larger addressable memory space. The architecture can provide a significant code size reduction when compiling C programs while fully preserving the legacy of C51 assembly routines.

The TSC80251G2D derivatives are pin and software compatible with standard 80C51/Fx/Rx/Rx+ with extended on-chip data memory (1 Kbyte RAM) and up to 256 kilobytes of external code and data. Additionally, the TSC83251G2D and TSC87251G2D provide on-chip code memory: 32 kilobytes ROM and 32 kilobytes EPROM/OTPROM respectively.

They provide transparent enhancements to Intel's 8xC251Sx family with an additional Synchronous Serial Link Controller (SSLC supporting TWI, µWire and SPI protocols), a Keyboard interrupt interface, a dedicated Baud Rate Generator for UART, and Power Management features.

TSC80251G2D derivatives are optimized for speed and for low power consumption on a wide voltage range.

Note: 1. This Datasheet provides the technical description of the TSC80251G2D derivatives. For further information on the device usage, please request the TSC80251 Programmer's Guide and the TSC80251G1D Design Guide and errata sheet.

Typical Applications

- ISDN Terminals
- High-Speed Modems
- PABX (SOHO)
- Line Cards
- DVD ROM and Players
- Printers
- Plotters
- Scanners
- Banking Machines
- Barcode Readers
- Smart Cards Readers
- High-End Digital Monitors
- High-End Joysticks
- High-end TV's

Table 7. System Management SFRs

Mnemonic	Name
PCON	Power Control
POWM	Power Management

Mnemonic	Name
CKRL	Clock Reload
WCON	Synchronous Real-Time Wait State Control

Table 8. Interrupt SFRs

Mnemonic	Name
IE0	Interrupt Enable Control 0
IE1	Interrupt Enable Control 1
IPH0	Interrupt Priority Control High 0

Mnemonic	Name
IPL0	Interrupt Priority Control Low 0
IPH1	Interrupt Priority Control High 1
IPL1	Interrupt Priority Control Low 1

Table 9. Keyboard Interface SFRs

Mnemonic	Name
P1IE	Port 1 Input Interrupt Enable
P1F	Port 1 Flag

Mnemonic	Name
P1LS	Port 1 Level Selection

Table 11. Configuration Byte 0
UCONFIG0

7	6	5	4	3	2	1	0
-	WSA1#	WSA0#	XALE#	RD1	RD0	PAGE#	SRC

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** Set this bit when writing to UCONFIG0.
6	WSA1#	**Wait State A bits** Select the number of wait states for RD#, WR# and PSEN# signals for external memory accesses (all regions except 01:). WSA1# WSA0# Number of Wait States 0 0 3 0 1 2 1 0 1 1 1 0
5	WSA0#	
4	XALE#	**Extend ALE bit** Clear to extend the duration of the ALE pulse from T_{OSC} to $3 \cdot T_{OSC}$. Set to minimize the duration of the ALE pulse to $1 \cdot T_{OSC}$.
3	RD1	**Memory Signal Select bits** Specify a 18-bit, 17-bit or 16-bit external address bus and the usage of RD#, WR# and PSEN# signals (see Table 13).
2	RD0	
1	PAGE#	**Page Mode Select bit**(1) Clear to select the faster Page mode with A15:8/D7:0 on Port 2 and A7:0 on Port 0. Set to select the non-Page mode(2) with A15:8 on Port 2 and A7:0/D7:0 on Port 0.
0	SRC	**Source Mode/Binary Mode Select bit** Clear to select the binary mode. Set to select the source mode.

Notes: 1. UCONFIG0 is fetched twice so it can be properly read both in Page or Non-Page modes. If P2.1 is cleared during the first data fetch, a Page mode configuration is used, otherwise the subsequent fetches are performed in Non-Page mode.
2. This selection provides compatibility with the standard 80C51 hardware which is multiplexing the address LSB and the data on Port 0.

Configuration Byte 1

Table 13. Address Ranges and Usage of RD#, WR# and PSEN# Signals

RD1	RD0	P1.7	P3.7/RD#	PSEN#	WR#	External Memory
0	0	A17	A16	Read signal for all external memory locations	Write signal for all external memory locations	256 KB
0	1	I/O pin	A16	Read signal for all external memory locations	Write signal for all external memory locations	128 KB
1	0	I/O pin	I/O pin	Read signal for all external memory locations	Write signal for all external memory locations	64 KB
1	1	I/O pin	Read signal for regions 00: and 01:	Read signal for regions FE: and FF:	Write signal for all external memory locations	2×64 KB(1)

Notes: 1. This selection provides compatibility with the standard 80C51 hardware which has separate external memory spaces for data and code.

Table 19. Notation for Register Operands

Register	Description	C251	C51
at Ri	A memory location (00h-FFh) addressed indirectly via byte registers R0 or R1	–	3
Rn n	Byte register R0-R7 of the currently selected register bank Byte register index: n = 0-7	–	3
Rm Rmd Rms m, md, ms	Byte register R0-R15 of the currently selected register file Destination register Source register Byte register index: m, md, ms = 0-15	3	–
WRj WRjd WRjs at WRj at WRj +dis16 j, jd, js	Word register WR0, WR2, ..., WR30 of the currently selected register file Destination register Source register A memory location (00:0000h-00:FFFFh) addressed indirectly through word register WR0-WR30, is the target address for jump instructions. A memory location (00:0000h-00:FFFFh) addressed indirectly through word register (WR0-WR30) + 16-bit signed (two's complement) displacement value Word register index: j, jd, js = 0-30	3	–
DRk DRkd DRks at DRk at DRk +dis16 k, kd, ks	Dword register DR0, DR4, ..., DR28, DR56, DR60 of the currently selected register file Destination register Source register A memory location (00:0000h-FF:FFFFh) addressed indirectly through dword register DR0-DR28, DR56 and DR60, is the target address for jump instruction A memory location (00:0000h-FF:FFFFh) addressed indirectly through dword register (DR0-DR28, DR56, DR60) + 16-bit (two's complement) signed displacement value Dword register index: k, kd, ks = 0, 4, 8..., 28, 56, 60	3	–

Table 24. Summary of Multiply, Divide and Decimal-adjust Instructions

MultiplyMUL AB(B:A) ← (A)×(B)
MUL <dest>, <src>extended dest opnd ← dest opnd × src opnd

DivideDIV AB(A) ← Quotient ((A)/(B))
(B) ← Remainder ((A)/(B))

DivideDIV <dest>, <src>ext. dest opnd high ← Quotient (dest opnd/src opnd)
ext. dest opnd low ← Remainder (dest opnd/src opnd)

Decimal-adjust ACCDA AIF [[$(A)_{3:0}$ > 9] ∨ [(AC) = 1]]
for Addition (BCD) THEN $(A)_{3:0} \leftarrow (A)_{3:0}$ + 6 !affects CY;
IF [[$(A)_{7:4}$ > 9] ∨ [(CY) = 1]]
THEN $(A)_{7:4} \leftarrow (A)_{7:4}$ + 6

Mnemonic	<dest>, <src>(1)	Comments	Binary Mode		Source Mode	
			Bytes	States	Bytes	States
MUL	AB	Multiply A and B	1	5	1	5
	Rmd, Rms	Multiply byte register and byte register	3	6	2	5
	WRjd, WRjs	Multiply word register and word register	3	12	2	11
DIV	AB	Divide A and B	1	10	1	10
	Rmd, Rms	Divide byte register and byte register	3	11	2	10
	WRjd, WRjs	Divide word register and word register	3	21	2	20
DA	A	Decimal adjust ACC	1	1	1	1

Note: 1. A shaded cell denotes an instruction in the C51 Architecture.

MOV	WRj, at WRj +dis24	Indirect with 16-bit displacement (16M) to word register	5	8[5]	4	7[5]
MOV	at WRj +dis16, Rm	Byte register to indirect with 16-bit displacement (64K)	5	6[4]	4	5[4]
MOV	at WRj +dis16, WRj	Word register to indirect with 16-bit displacement (64K)	5	7[5]	4	6[5]
MOV	at DRk +dis24, Rm	Byte register to indirect with 16-bit displacement (16M)	5	7[4]	4	6[4]
MOV	at DRk +dis24, WRj	Word register to indirect with 16-bit displacement (16M)	5	8[5]	4	7[5]

Notes:
1. Instructions that move bits are in Table 27.
2. Move instructions unique to the C251 Architecture.
3. If this instruction addresses an I/O Port (Px, x = 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.
4. If this instruction addresses external memory location, add N+2 to the number of states (N: number of wait states).
5. If this instruction addresses external memory location, add 2(N+1) to the number of states (N: number of wait states).
6. If this instruction addresses external memory location, add 4(N+2) to the number of states (N: number of wait states).

Table 32. Summary of Call and Return Instructions

Absolute callACALL <src>(PC) ← (PC) +2; push $(PC)_{15:0}$;
$(PC)_{10:0}$ ← src opnd
Extended callECALL <src>(PC) ← (PC) + size (instr); push $(PC)_{23:0}$;
$(PC)_{23:0}$ ← src opnd
Long callLCALL <src>(PC) ← (PC) + size (instr); push $(PC)_{15:0}$;
$(PC)_{15:0}$ ← src opnd
Return from subroutineRETpop $(PC)_{15:0}$
Extended return from subroutineERETpop $(PC)_{23:0}$
Return from interruptRETIIF [INTR = 0] THEN pop $(PC)_{15:0}$
IF [INTR = 1] THEN pop $(PC)_{23:0}$; pop (PSW1)
Trap interruptTRAP(PC) ← (PC) + size (instr);
IF [INTR = 0] THEN push $(PC)_{15:0}$
IF [INTR = 1] THEN push (PSW1); push $(PC)_{23:0}$

Mnemonic	<dest>, <src>(1)	Comments	Binary Mode		Source Mode	
			Bytes	States	Bytes	States
ACALL	addr11	Absolute subroutine call	2	9(2)(3)	2	9(2)(3)
ECALL	at DRk	Extended subroutine call (indirect)	3	14(2)(3)	2	13(2)(3)
	addr24	Extended subroutine call	5	14(2)(3)	4	13(2)(3)
LCALL	at WRj	Long subroutine call (indirect)	3	10(2)(3)	2	9(2)(3)
	addr16	Long subroutine call	3	9(2)(3)	3	9(2)(3)
RET		Return from subroutine	1	7(2)	1	7(2)
ERET		Extended subroutine return	3	9(2)	2	8(2)
RETI		Return from interrupt	1	7(2)(4)	1	7(2)(4)
TRAP		Jump to the trap interrupt vector	2	12(4)	1	11(4)

Notes:
1. A shaded cell denotes an instruction in the C51 Architecture.
2. In internal execution only, add 1 to the number of states if the destination/return address is internal and odd.
3. Add 2 to the number of states if the destination address is external.
4. Add 5 to the number of states if INTR = 1.

Programming and Verifying Non-volatile Memory

Internal Features

The internal non-volatile memory of the TSC80251G2D derivatives contains five different areas:

- Code Memory
- Configuration Bytes
- Lock Bits
- Encryption Array
- Signature Bytes

EPROM/OTPROM Devices

All the internal non-volatile memory but the Signature Bytes of the TSC87251G2D products is made of EPROM cells. The Signature Bytes of the TSC87251G2D products are made of Mask ROM.

The TSC87251G2D products are programmed and verified in the same manner as Atmel's TSC87251G1A, using a SINGLE-PULSE algorithm, which programs at V_{PP} = 12.75V using only one 100µs pulse per byte. This results in a programming time of less than 10 seconds for the 32 kilobytes on-chip code memory.

The EPROM of the TSC87251G2D products in Window package is erasable by Ultra-Violet radiation(1) (UV). UV erasure set all the EPROM memory cells to one and allows reprogramming. The quartz window must be covered with an opaque label(2) when the device is in operation. This is not so much to protect the EPROM array from inadvertent erasure, as to protect the RAM and other on-chip logic. Allowing light to impinge on the silicon die during device operation may cause a logical malfunction.

The TSC87251G2D products in plastic packages are One Time Programmable (OTP). An EPROM cell cannot be reset by UV once programmed to zero.

Notes:
1. The recommended erasure procedure is exposure to ultra-violet light (at 2537 Å) to an integrated dose of at least 20 W-sec/cm^2. Exposing the EPROM to an ultra-violet lamp of 12000 µW/cm^2 rating for 30 minutes should be sufficient.
2. Erasure of the EPROM begins to occur when the chip is exposed to light wavelength shorter than 4000 Å. Since sunlight and fluorescent light have wavelength in this range, exposure to these light sources over an extended time (1 week in sunlight or 3 years in room-level fluorescent lighting) could cause inadvertent erasure.

Mask ROM Devices

All the internal non-volatile memory of TSC83251G2D products is made of Mask ROM cells. They can only be verified by the user, using the same algorithm as the EPROM/OTPROM devices.

ROMless Devices

The TSC80251G2D products do not include on-chip Configuration Bytes, Code Memory and Encryption Array. They only include Signature Bytes made of Mask ROM cells which can be read using the same algorithm as the EPROM/OTPROM devices.

Security Features

In some microcontroller applications, it is desirable that the user's program code be secured from unauthorized access. The TSC83251G2D and TSC87251G2D offer two kinds of protection for program code stored in the on-chip array:

- Program code in the on-chip Code Memory is encrypted when read out for verification if the Encryption Array isprogrammed.
- A three-level lock bit system restricts external access to the on-chip code memory.

Lock Bit System

The TSC87251G2D products implement 3 levels of security for User's program as described in Table 33. The TSC83251G2D products implement only the first level of security.

Level 0 is the level of an erased part and does not enable any security features.

Level 1 locks the programming of the User's internal Code Memory, the Configuration Bytes and the Encryption Array.

Level 2 locks the verifying of the User's internal Code Memory. It is always possible to verify the Configuration Bytes and the Lock Bits. It is not possible to verify the Encryption Array.

Level 3 locks the external execution.

Table 33. Lock Bits Programming

Level	Lock bits LB[2:0]	Internal Execution	External Execution	Verification	Programming	External PROM read (MOVC)
0	000	Enable	Enable	Enable(1)	Enable	Enable(2)
1	001	Enable	Enable	Enable(1)	Disable	Disable
2	01x(3)	Enable	Enable	Disable	Disable	Disable
3	1xx(3)	Enable	Disable	Disable	Disable	Disable

Notes: 1. Returns encrypted data if Encryption Array is programmed.
2. Returns non encrypted data.
3. x means don't care. Level 2 always enables level 1, and level 3 always enables levels 1 and 2.

The security level may be verified according to Table 34.

Table 34. Lock Bits Verifying

Level	Lock bits Data(1)
0	xxxxx000
1	xxxxx001
2	xxxxx01x
3	xxxxx1xx

Note: 1. x means don't care.

Encryption Array

The TSC83251G2D and TSC87251G2D products include a 128-byte Encryption Array located in non-volatile memory outside the memory address space. During verification of the on-chip code memory, the seven low-order address bits also address the Encryption Array. As the byte of the code memory is read, it is exclusive-NOR'ed (XNOR) with the key byte from the Encryption Array. If the Encryption Array is not programmed (still all 1s), the user program code is placed on the data bus in its original, unencrypted form. If the Encryption Array is programmed with key bytes, the user program code is encrypted and cannot be used without knowledge of the key byte sequence.

To preserve the secrecy of the encryption key byte sequence, the Encryption Array can not be verified.

Notes:
1. When a MOVC instruction is executed, the content of the ROM is not encrypted. In order to fully protect the user program code, the lock bit level 1 (see Table 33) must always be set when encryption is used.
2. If the encryption feature is implemented, the portion of the on-chip code memory that does not contain program code should be filled with “random” byte values to prevent the encryption key sequence from being revealed.

Signature Bytes

The TSC80251G2D derivatives contain factory-programmed Signature Bytes. These bytes are located in non-volatile memory outside the memory address space at 30h, 31h, 60h and 61h. To read the Signature Bytes, perform the procedure described in section Verify Algorithm, using the verify signature mode (see Table 37). Signature byte values are listed in Table 35.

Table 35. Signature Bytes (Electronic ID)

		Signature Address	Signature Data
Vendor	Atmel	30h	58h
Architecture	C251	31h	40h
Memory	32 kilobytes EPROM or OTPROM	60h	F7h
	32 kilobytes MaskROM or ROMless		77h
Revision	TSC80251G2D derivative	61h	FDh

Programming Algorithm

Figure 6 shows the hardware setup needed to program the TSC87251G2D EPROM/OTPROM areas:

- The chip has to be put under reset and maintained in this state until completion of the programming sequence.
- PSEN# and the other control signals (ALE and Port 0) have to be set to a high level.
- Then PSEN# has to be to forced to a low level after two clock cycles or more and it has to be maintained in this state until the completion of the programming sequence (see below).
- The voltage on the EA# pin must be set to V_{DD}.
- The programming mode is selected according to the code applied on Port 0 (see Table 36). It has to be applied until the completion of this programming operation.
- The programming address is applied on Ports 1 and 3 which are respectively the Most Significant Byte (MSB) and the Least Significant Byte (LSB) of the address.
- The programming data are applied on Port 2.
- The EPROM Programming is done by raising the voltage on the EA# pin to V_{PP}, then by generating a low level pulse on ALE/PROG# pin.
- The voltage on the EA# pin must be lowered to V_{DD} before completing the programming operation.
- It is possible to alternate programming and verifying operation (See Paragraph Verify Algorithm). Please make sure the voltage on the EA# pin has actually been lowered to V_{DD} before performing the verifying operation.

AC Characteristics - Real-Time Asynchronous Wait State

Definition of Symbols

Table 43. Real-Time Asynchronous Wait Timing Symbol Definitions

Signals	
S	PSEN#/RD#/WR#
Y	AWAIT#

Conditions	
L	Low
V	Valid
X	No Longer Valid

Timings

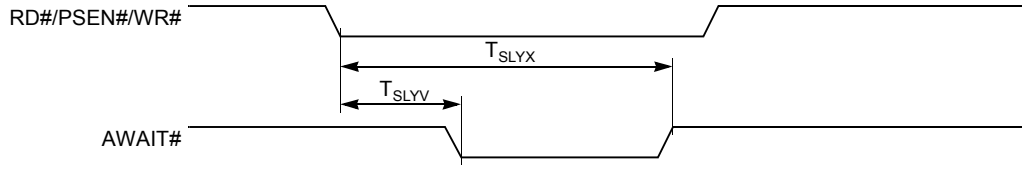
Table 44. Real-Time Asynchronous Wait AC Timings; V_{DD} = 2.7 to 5.5 V, T_A = -40 to 85°C

Symbol	Parameter	Min	Max	Unit
T_{SLYV}	PSEN#/RD#/WR# Low to Wait Set-up		T_{OSC} - 10	ns
T_{SLYX}	Wait Hold after PSEN#/RD#/WR# Low	$(2N-1)\cdot T_{OSC}$ + 10		ns(1)

Note: 1. N is the number of wait states added (N≥ 1).

Waveforms

Figure 16. Real-time Asynchronous Wait State Timings



AC Characteristics - Serial Port in Shift Register Mode

Definition of Symbols

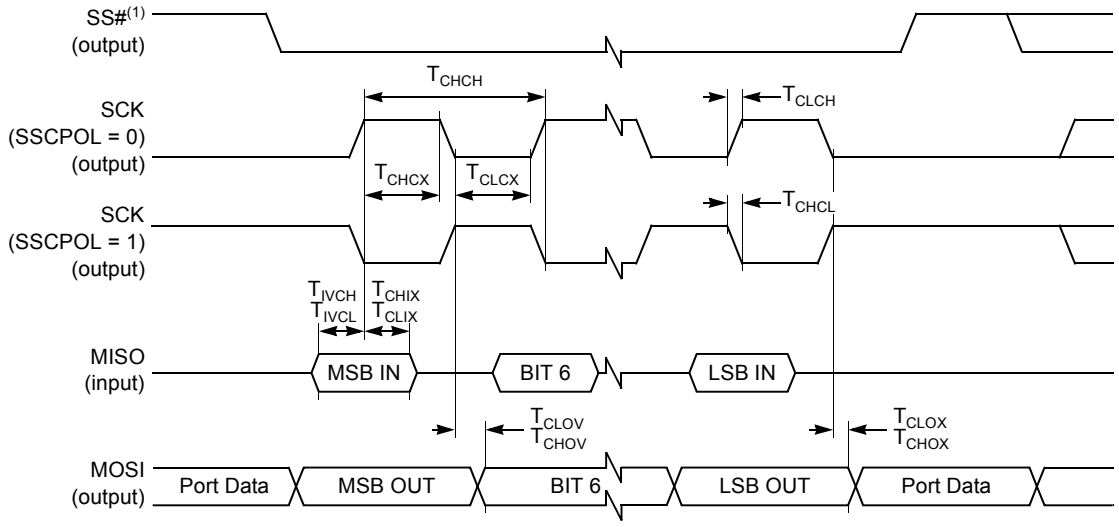
Table 45. Serial Port Timing Symbol Definitions

Signals	
D	Data In
Q	Data Out
X	Clock

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid

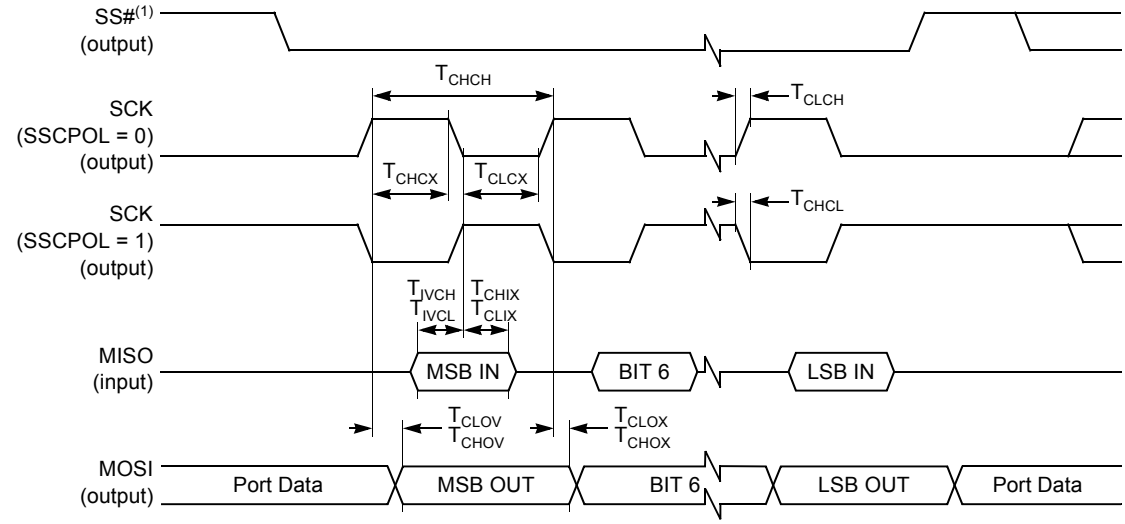
Waveforms

Figure 19. SPI Master Waveforms (SSCPHA = 0)



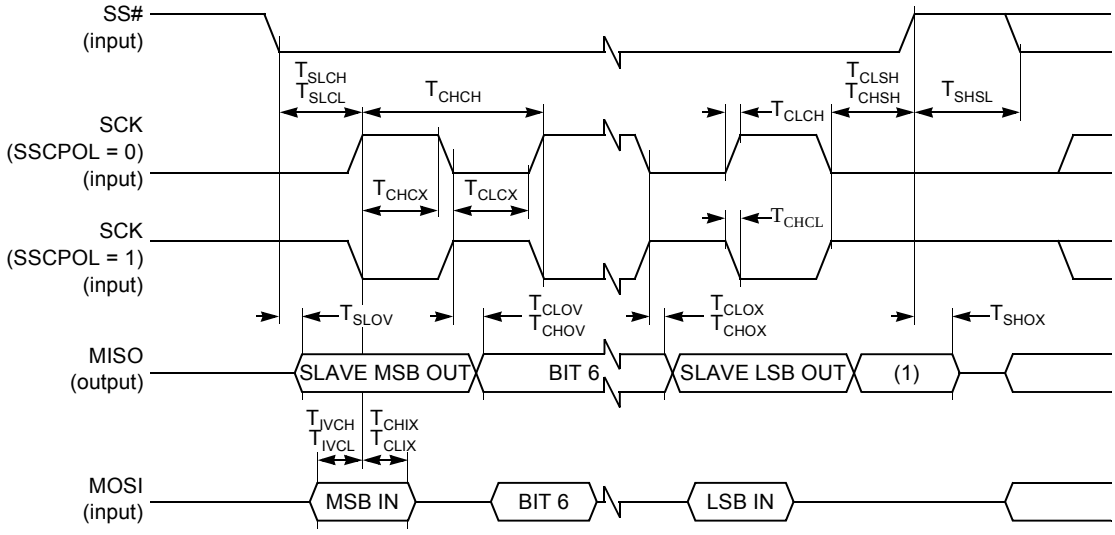
Note: 1. SS# handled by software.

Figure 20. SPI Master Waveforms (SSCPHA = 1)



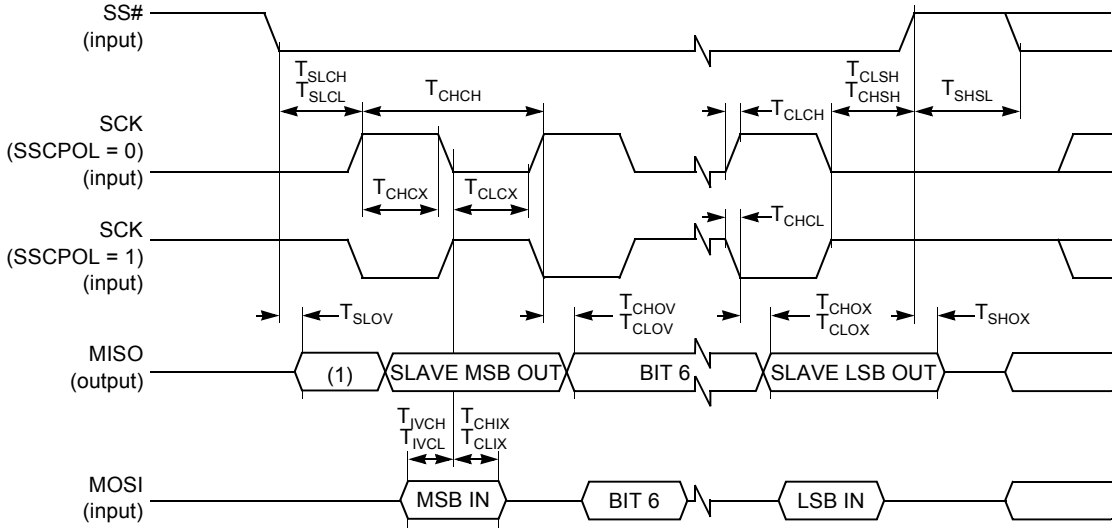
Note: 1. Not Defined but normally MSB of character just received.

Figure 21. SPI Slave Waveforms (SSCPHA = 0)



Note: 1. Not Defined but generally the LSB of the character which has just been received.

Figure 22. SPI Slave Waveforms (SSCPHA = 1)



AC Characteristics - EPROM Programming and Verifying

Definition of Symbols

Table 50. EPROM Programming and Verifying Timing Symbol Definitions

Signals	
A	Address
E	Enable: mode set on Port 0
G	Program
Q	Data Out
S	Supply (V_{PP})

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid
Z	Floating

Timings

Table 51. EPROM Programming AC timings; V_{DD} = 4.5 to 5.5 V, T_A = 0 to 40°C

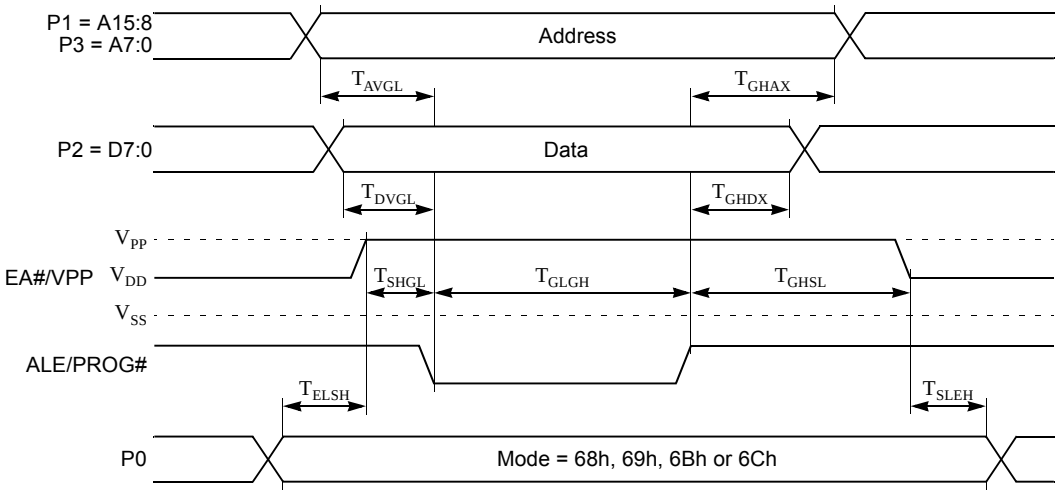
Symbol	Parameter	Min	Max	Unit
T_{OSC}	XTAL1 Period	83.5	250	ns
T_{AVGL}	Address Setup to PROG# low	48		T_{OSC}
T_{GHAX}	Address Hold after PROG# low	48		T_{OSC}
T_{DVGL}	Data Setup to PROG# low	48		T_{OSC}
T_{GHDX}	Data Hold after PROG#	48		T_{OSC}
T_{ELSH}	ENABLE High to V_{PP}	48		T_{OSC}
T_{SHGL}	V_{PP} Setup to PROG# low	10		µs
T_{GHSL}	V_{PP} Hold after PROG#	10		µs
T_{SLEH}	ENABLE Hold after V_{PP}	0		ns
T_{GLGH}	PROG# Width	90	110	µs

Table 52. EPROM Verifying AC timings; V_{DD} = 4.5 to 5.5 V, V_{DD} = 2.7 to 5.5 V, T_A = 0 to 40°C

Symbol	Parameter	Min	Max	Unit
T_{OSC}	XTAL1 Period	83.5	250	ns
T_{AVQV}	Address to Data Valid		48	T_{OSC}
T_{AXQX}	Address to Data Invalid	0		ns
T_{ELQV}	ENABLE low to Data Valid	0	48	T_{OSC}
T_{EHQZ}	Data Float after ENABLE	0	48	T_{OSC}

Waveforms

Figure 23. EPROM Programming Waveforms



Absolute Maximum Rating and Operating Conditions

Absolute Maximum Ratings

Storage Temperature ..... -65 to +150°C Voltage on any other Pin to VSS ..... -0.5 to +6.5 V I_{OL} per I/O Pin ..... 15 mA Power Dissipation ..... 1.5 W Ambient Temperature Under Bias Commercial.....0 to +70°C Industrial ..... -40 to +85°C Automotive..... -40 to +85°C V_{DD} High Speed versions..... 4.5 to 5.5 V Low Voltage versions..... 2.7 to 5.5 V	*NOTICE: Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only. Operation beyond the “operating conditions” is not recommended and extended exposure beyond the “Operating Conditions” may affect device reliability.

Packages

List of Packages

- PDIL 40
- CDIL 40 with window
- PLCC 44
- CQPJ 44 with window
- VQFP 44 (10x10)

PDIL 40 - Mechanical Outline

Figure 33. Plastic Dual In Line

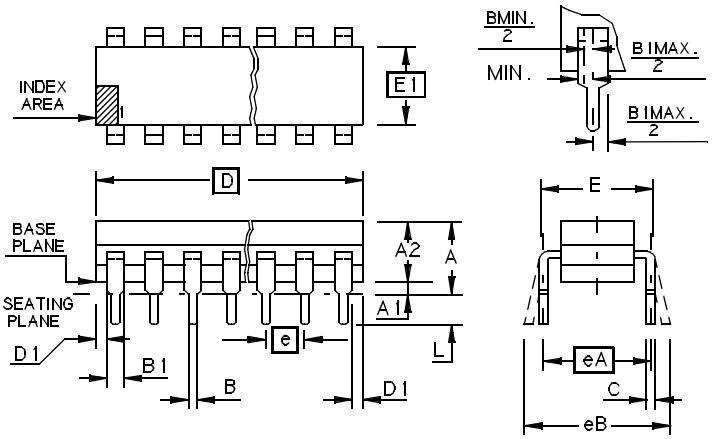


Table 57. PDIL Package Size

	MM		Inch	
	Min	**Max**	**Min**	**Max**
A	-	5.08	-	.200
A1	0.38	-	.015	-
A2	3.18	4.95	.125	.195
B	0.36	0.56	.014	.022
B1	0.76	1.78	.030	.070
C	0.20	0.38	.008	.015
D	50.29	53.21	1.980	2.095
E	15.24	15.87	.600	.625
E1	12.32	14.73	.485	.580
e	2.54 B.S.C.		.100 B.S.C.	
eA	15.24 B.S.C.		.600 B.S.C.	
eB	-	17.78	-	.700
L	2.93	3.81	.115	.150
D1	0.13	-	.005	-

CDIL 40 with Window - Mechanical Outline

Figure 34. Ceramic Dual In Line

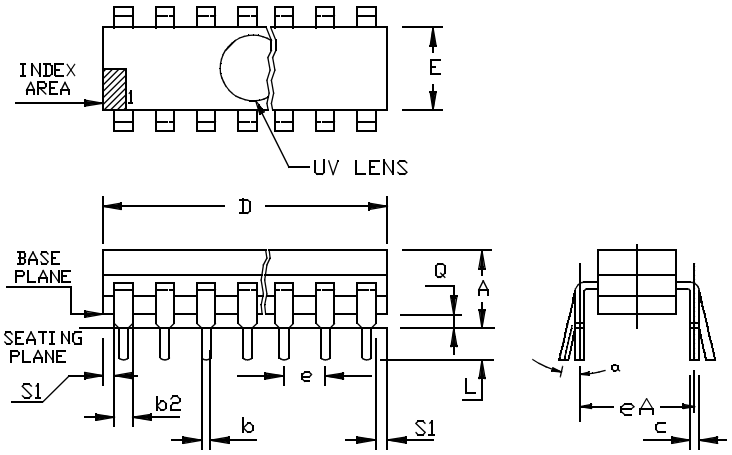


Table 58. CDIL Package Size

	MM		Inch	
	Min	**Max**	**Min**	**Max**
A	-	5.71	-	.225
b	0.36	0.58	.014	.023
b2	1.14	1.65	.045	.065
c	0.20	0.38	.008	.015
D	-	53.47	-	2.105
E	13.06	15.37	.514	.605
e	2.54 B.S.C.		.100 B.S.C.	
eA	15.24 B.S.C.		.600 B.S.C.	
L	3.18	5.08	.125	.200
Q	0.38	1.40	.015	.055
S1	0.13	-	.005	-
a	0 - 15		0 - 15	
N	40			

Part Number[1]	ROM	Description
Low Voltage Versions 2.7 to 5.5 V		
TSC251G2Dxxx-L16CB	32K MaskROM	16 MHz, Commercial 0° to 70°C, PLCC 44
TSC251G2Dxxx-L16CE	32K MaskROM	16 MHz, Commercial 0° to 70°C, VQFP 44
AT251G2Dxxx-SLSUL	32K MaskROM	16 MHz, Industrial & Green, PLCC 44
AT251G2Dxxx-RLTUL	32K MaskROM	16 MHz, Industrial & Green, VQFP 44

Note: 1. xxx: means ROM code, is Cxxx in case of encrypted code.

Options (Please consult Atmel sales)

- ROM code encryption
- Tape & Reel or Dry Pack
- Known good dice
- Extended temperature range: -55°C to +125°C

Product Markings

ROMless versions

ATMEL
Part number

YYWW . Lot Number

Mask ROM versions

ATMEL
Customer Part number

Part Number
YYWW . Lot Number

OTP versions

ATMEL
Part number

YYWW . Lot Number