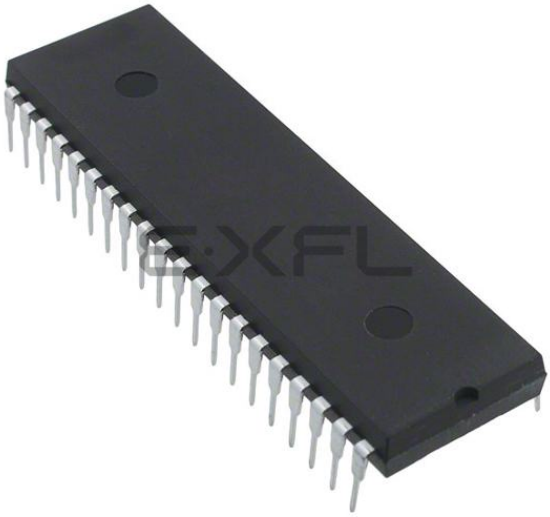

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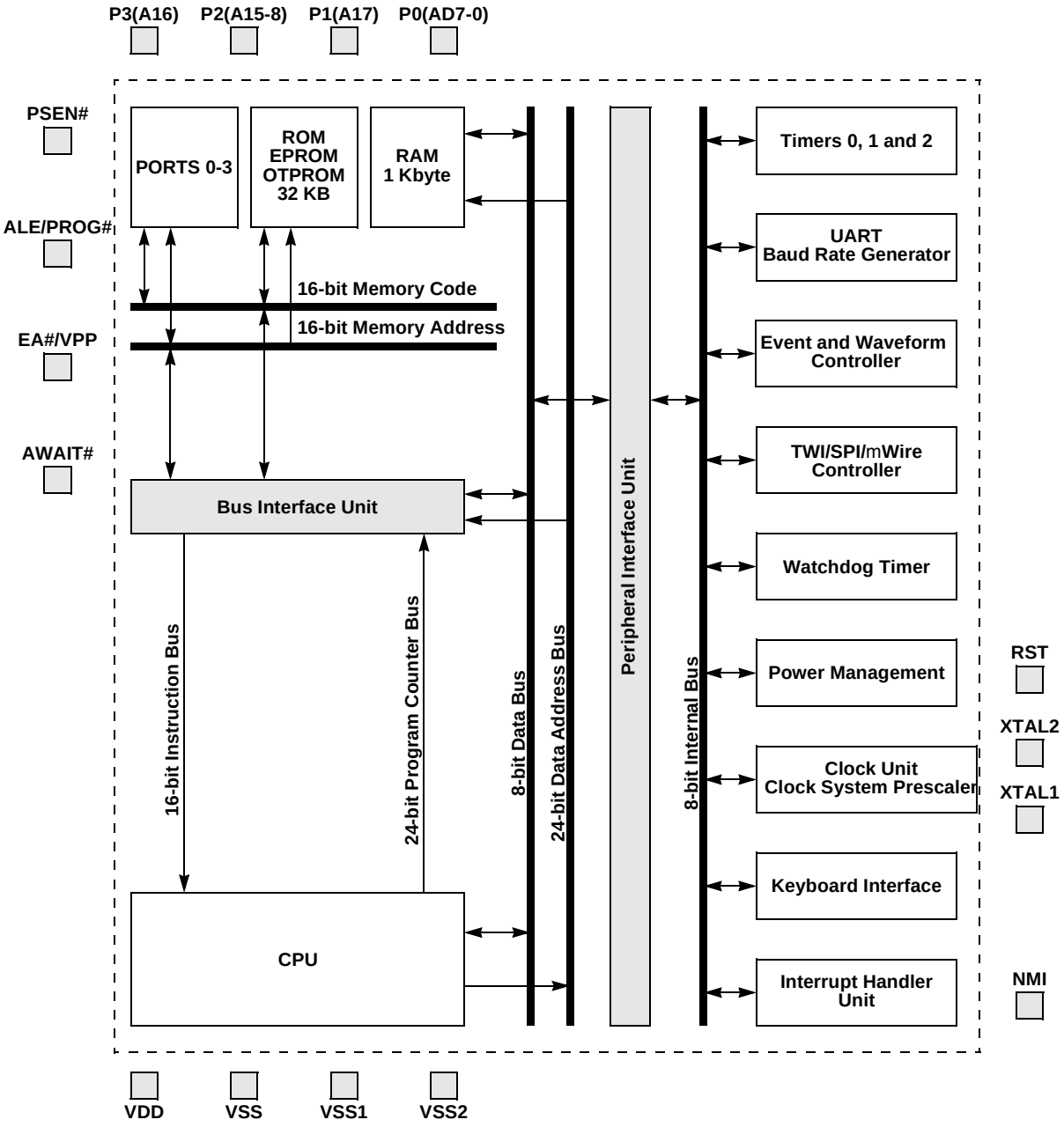
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C251
Core Size	8/16-Bit
Speed	24MHz
Connectivity	EBI/EMI, I²C, Microwire, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIL
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at87251g2d-3csum

Block Diagram



compatibility with the C51 Architecture). When PC increments beyond the end of segment FE:, it continues at the reset address FF:0000h (linearity). When PC increments beyond the end of segment 01:, it loops to the beginning of segment 00: (this prevents from its going into the reserved area).

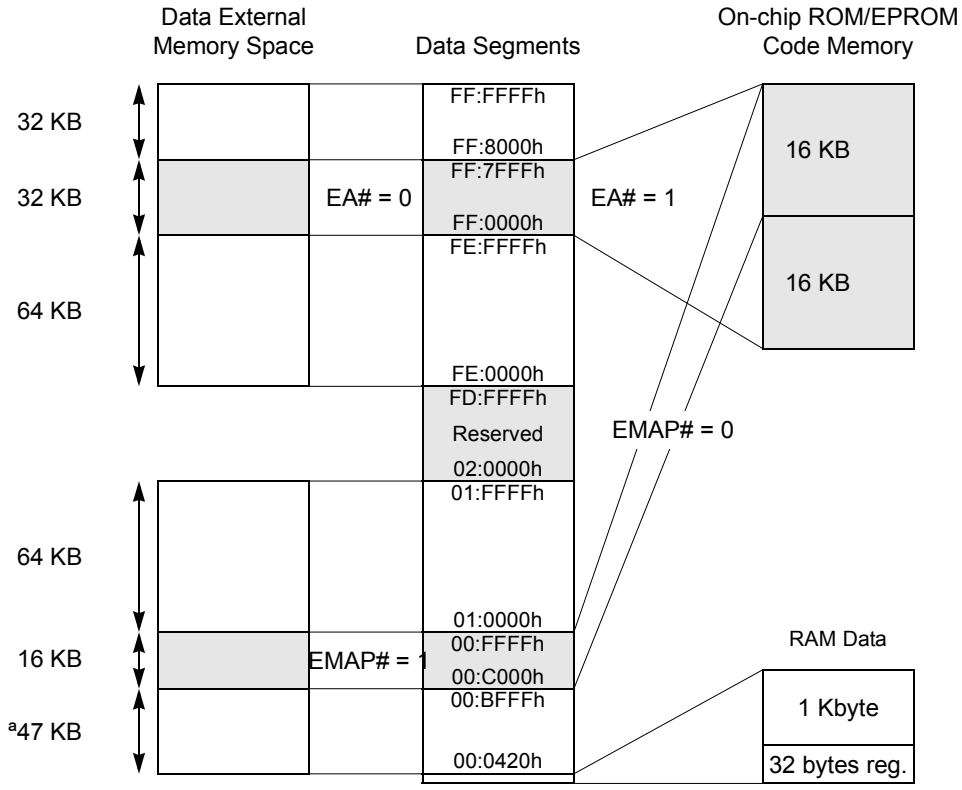
Data Memory

The TSC80251G2D derivatives implement 1 Kbyte of on-chip data RAM. Figure 5 shows the split of the internal and external data memory spaces. This memory is mapped in the data space just over the 32 bytes of registers area (see TSC80251 Programmers' Guide). Hence, the part of the on-chip RAM located from 20h to FFh is bit addressable. This on-chip RAM is not accessible through the program/code memory space.

For faster computation with the on-chip ROM/EPROM code of the TSC83251G2D/TSC87251G2D, its upper 16 KB are also mapped in the upper part of the region 00: if the On-Chip Code Memory Map configuration bit is cleared (EMAP# bit in UCONFIG1 byte, see Figure). However, if EA# is tied to a low level, the TSC80251G2D derivative is running as a ROMless product and the code is actually fetched in the corresponding external memory (i.e. the upper 16 KB of the lower 32 KB of the segment FF:). If EMAP# bit is set, the on-chip ROM is not accessible through the region 00:.

All the accesses to the portion of the data space with no on-chip memory mapped onto are redirected to the external memory.

Figure 5. Data Memory Mapping



4135F–8051–11/06

Special Function Registers

The Special Function Registers (SFRs) of the TSC80251G2D derivatives fall into the categories detailed in Table 1 to Table 9.

SFRs are placed in a reserved on-chip memory region S: which is not represented in the data memory mapping (Figure 5). The relative addresses within S: of these SFRs are provided together with their reset values in Table . They are upward compatible with the SFRs of the standard 80C51 and the Intel's 80C251Sx family. In this table, the C251 core registers are identified by Note 1 and are described in the TSC80251 Programmer's Guide. The other SFRs are described in the TSC80251G1D Design Guide. All the SFRs are bit-addressable using the C251 instruction set.

Table 1. C251 Core SFRs

Mnemonic	Name
ACC(1)	Accumulator
B(1)	B Register
PSW	Program Status Word
PSW1	Program Status Word 1
SP(1)	Stack Pointer - LSB of SPX

Mnemonic	Name
SPH(1)	Stack Pointer High - MSB of SPX
DPL(1)	Data Pointer Low byte - LSB of DPTR
DPH(1)	Data Pointer High byte - MSB of DPTR
DPXL(1)	Data Pointer Extended Low byte of DPX - Region number

Note: 1. These SFRs can also be accessed by their corresponding registers in the register file.

Table 2. I/O Port SFRs

Mnemonic	Name
P0	Port 0
P1	Port 1

Mnemonic	Name
P2	Port 2
P3	Port 3

Table 3. Timers SFRs

Mnemonic	Name
TL0	Timer/Counter 0 Low Byte
TH0	Timer/Counter 0 High Byte
TL1	Timer/Counter 1 Low Byte
TH1	Timer/Counter 1 High Byte
TL2	Timer/Counter 2 Low Byte
TH2	Timer/Counter 2 High Byte
TCON	Timer/Counter 0 and 1 Control

Mnemonic	Name
TMOD	Timer/Counter 0 and 1 Modes
T2CON	Timer/Counter 2 Control
T2MOD	Timer/Counter 2 Mode
RCAP2L	Timer/Counter 2 Reload/Capture Low Byte
RCAP2H	Timer/Counter 2 Reload/Capture High Byte
WDTRST	WatchDog Timer Reset

Table 4. Serial I/O Port SFRs

Mnemonic	Name
SCON	Serial Control
SBUF	Serial Data Buffer
SADEN	Slave Address Mask

Mnemonic	Name
SADDR	Slave Address
BRL	Baud Rate Reload
BDRCON	Baud Rate Control

Table 5. SSLC SFRs

Mnemonic	Name
SSCON	Synchronous Serial control
SSDAT	Synchronous Serial Data
SSCS	Synchronous Serial Control and Status

Mnemonic	Name
SSADR	Synchronous Serial Address
SSBR	Synchronous Serial Bit Rate

Table 6. Event Waveform Control SFRs

Mnemonic	Name
CCON	EWC-PCA Timer/Counter Control
CMOD	EWC-PCA Timer/Counter Mode
CL	EWC-PCA Timer/Counter Low Register
CH	EWC-PCA Timer/Counter High Register
CCAPM0	EWC-PCA Timer/Counter Mode 0
CCAPM1	EWC-PCA Timer/Counter Mode 1
CCAPM2	EWC-PCA Timer/Counter Mode 2
CCAPM3	EWC-PCA Timer/Counter Mode 3
CCAPM4	EWC-PCA Timer/Counter Mode 4

Mnemonic	Name
CCAP0L	EWC-PCA Compare Capture Module 0 Low Register
CCAP1L	EWC-PCA Compare Capture Module 1 Low Register
CCAP2L	EWC-PCA Compare Capture Module 2 Low Register
CCAP3L	EWC-PCA Compare Capture Module 3 Low Register
CCAP4L	EWC-PCA Compare Capture Module 4 Low Register
CCAP0H	EWC-PCA Compare Capture Module 0 High Register
CCAP1H	EWC-PCA Compare Capture Module 1 High Register
CCAP2H	EWC-PCA Compare Capture Module 2 High Register
CCAP3H	EWC-PCA Compare Capture Module 3 High Register
CCAP4H	EWC-PCA Compare Capture Module 4 High Register

Table 7. System Management SFRs

Mnemonic	Name
PCON	Power Control
POWM	Power Management

Mnemonic	Name
CKRL	Clock Reload
WCON	Synchronous Real-Time Wait State Control

Table 8. Interrupt SFRs

Mnemonic	Name
IE0	Interrupt Enable Control 0
IE1	Interrupt Enable Control 1
IPH0	Interrupt Priority Control High 0

Mnemonic	Name
IPL0	Interrupt Priority Control Low 0
IPH1	Interrupt Priority Control High 1
IPL1	Interrupt Priority Control Low 1

Table 9. Keyboard Interface SFRs

Mnemonic	Name
P1IE	Port 1 Input Interrupt Enable
P1F	Port 1 Flag

Mnemonic	Name
P1LS	Port 1 Level Selection

Configuration Byte 1

Table 13. Address Ranges and Usage of RD#, WR# and PSEN# Signals

RD1	RD0	P1.7	P3.7/RD#	PSEN#	WR#	External Memory
0	0	A17	A16	Read signal for all external memory locations	Write signal for all external memory locations	256 KB
0	1	I/O pin	A16	Read signal for all external memory locations	Write signal for all external memory locations	128 KB
1	0	I/O pin	I/O pin	Read signal for all external memory locations	Write signal for all external memory locations	64 KB
1	1	I/O pin	Read signal for regions 00: and 01:	Read signal for regions FE: and FF:	Write signal for all external memory locations	2×64 KB(1)

Notes: 1. This selection provides compatibility with the standard 80C51 hardware which has separate external memory spaces for data and code.

Table 22. Summary of Compare Instructions

CompareCMP <dest>, <src>dest opnd - src opnd						
			Binary Mode		Source Mode	
Mnemonic	**<dest>, <src>(2)**	**Comments**	**Bytes**	**States**	**Bytes**	**States**
CMP	Rmd, Rms	Register with register	3	2	2	1
	WRjd, WRjs	Word register with word register	3	3	2	2
	DRkd, DRks	Dword register with dword register	3	5	2	4
	Rm, #data	Register with immediate data	4	3	3	2
	WRj, #data16	Word register with immediate 16-bit data	5	4	4	3
	DRk, #0data16	Dword register with zero-extended 16-bit immediate data	5	6	4	5
	DRk, #1data16	Dword register with one-extended 16-bit immediate data	5	6	4	5
	Rm, dir8	Direct address (on-chip RAM or SFR) with byte register	4	3(1)	3	2(1)
	WRj, dir8	Direct address (on-chip RAM or SFR) with word register	4	4	3	3
	Rm, dir16	Direct address (64K) with byte register	5	3(2)	4	2(2)
	WRj, dir16	Direct address (64K) with word register	5	4(3)	4	3(3)
	Rm, at WRj	Indirect address (64K) with byte register	4	3(2)	3	2(2)
	Rm, at DRk	Indirect address (16M) with byte register	4	4(2)	3	3(2)

Notes:
1. If this instruction addresses an I/O Port (Px, x = 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.
2. If this instruction addresses external memory location, add N+2 to the number of states (N: number of wait states).
3. If this instruction addresses external memory location, add 2(N+2) to the number of states (N: number of wait states).

Notes: 1. Logical instructions that affect a bit are in Table 27.
2. A shaded cell denotes an instruction in the C51 Architecture.
3. If this instruction addresses an I/O Port (Px, x = 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.
4. If this instruction addresses an I/O Port (Px, x = 0-3), add 2 to the number of states. Add 3 if it addresses a Peripheral SFR.
5. If this instruction addresses external memory location, add N+2 to the number of states (N: number of wait states).
6. If this instruction addresses external memory location, add 2(N+2) to the number of states (N: number of wait states).

Table 23. Summary of Logical Instructions (2/2)

Shift Left LogicalSLL <dest><dest>$_0 \leftarrow 0$
<dest>$_{n+1} \leftarrow$ <dest>$_n$, n = 0..msb-1
(CY) $\leftarrow$ <dest>$_{msb}$
Shift Right ArithmeticSRA <dest><dest>$_{msb} \leftarrow$ <dest>$_{msb}$
<dest>$_{n-1} \leftarrow$ <dest>$_n$, n = msb..1
(CY) $\leftarrow$ <dest>$_0$
Shift Right LogicalSRL <dest><dest>$_{msb} \leftarrow 0$
<dest>$_{n-1} \leftarrow$ <dest>$_n$, n = msb..1
(CY) $\leftarrow$ <dest>$_0$
SwapSWAP $AA_{3:0}$ $A_{7:4}$

Mnemonic	<dest>, <src>(1)	Comments	Binary Mode		Source Mode	
			Bytes	States	Bytes	States
SLL	Rm	Shift byte register left through the MSB	3	2	2	1
	WRj	Shift word register left through the MSB	3	2	2	1
SRA	Rm	Shift byte register right	3	2	2	1
	WRj	Shift word register right	3	2	2	1
SRL	Rm	Shift byte register left	3	2	2	1
	WRj	Shift word register left	3	2	2	1
SWAP	A	Swap nibbles within ACC	1	2	1	2

Note: 1. A shaded cell denotes an instruction in the C51 Architecture.

Table 24. Summary of Multiply, Divide and Decimal-adjust Instructions

MultiplyMUL AB(B:A) ← (A)×(B)
MUL <dest>, <src>extended dest opnd ← dest opnd × src opnd

DivideDIV AB(A) ← Quotient ((A)/(B))
(B) ← Remainder ((A)/(B))

DivideDIV <dest>, <src>ext. dest opnd high ← Quotient (dest opnd/src opnd)
ext. dest opnd low ← Remainder (dest opnd/src opnd)

Decimal-adjust ACCDA AIF [[$(A)_{3:0}$ > 9] ∨ [(AC) = 1]]
for Addition (BCD) THEN $(A)_{3:0} \leftarrow (A)_{3:0}$ + 6 !affects CY;
IF [[$(A)_{7:4}$ > 9] ∨ [(CY) = 1]]
THEN $(A)_{7:4} \leftarrow (A)_{7:4}$ + 6

Mnemonic	<dest>, <src>(1)	Comments	Binary Mode		Source Mode	
			Bytes	States	Bytes	States
MUL	AB	Multiply A and B	1	5	1	5
	Rmd, Rms	Multiply byte register and byte register	3	6	2	5
	WRjd, WRjs	Multiply word register and word register	3	12	2	11
DIV	AB	Divide A and B	1	10	1	10
	Rmd, Rms	Divide byte register and byte register	3	11	2	10
	WRjd, WRjs	Divide word register and word register	3	21	2	20
DA	A	Decimal adjust ACC	1	1	1	1

Note: 1. A shaded cell denotes an instruction in the C51 Architecture.

MOV	WRj, at WRj +dis24	Indirect with 16-bit displacement (16M) to word register	5	8[5]	4	7[5]
MOV	at WRj +dis16, Rm	Byte register to indirect with 16-bit displacement (64K)	5	6[4]	4	5[4]
MOV	at WRj +dis16, WRj	Word register to indirect with 16-bit displacement (64K)	5	7[5]	4	6[5]
MOV	at DRk +dis24, Rm	Byte register to indirect with 16-bit displacement (16M)	5	7[4]	4	6[4]
MOV	at DRk +dis24, WRj	Word register to indirect with 16-bit displacement (16M)	5	8[5]	4	7[5]

Notes:
1. Instructions that move bits are in Table 27.
2. Move instructions unique to the C251 Architecture.
3. If this instruction addresses an I/O Port (Px, x = 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.
4. If this instruction addresses external memory location, add N+2 to the number of states (N: number of wait states).
5. If this instruction addresses external memory location, add 2(N+1) to the number of states (N: number of wait states).
6. If this instruction addresses external memory location, add 4(N+2) to the number of states (N: number of wait states).

Table 30. Summary of Conditional Jump Instructions (2/2)

Jump if bitJB <src>, rel(PC) ← (PC) + size (instr);
IF [src opnd = 1] THEN (PC) ← (PC) + rel

Jump if not bitJNB <src>, rel(PC) ← (PC) + size (instr);
IF [src opnd = 0] THEN (PC) ← (PC) + rel

Jump if bit and clearJBC <dest>, rel(PC) ← (PC) + size (instr);
IF [dest opnd = 1] THEN
dest opnd ← 0
(PC) ← (PC) + rel

Jump if accumulator is zeroJZ rel(PC) ← (PC) + size (instr);
IF [(A) = 0] THEN (PC) ← (PC) + rel

Jump if accumulator is not zeroJNZ rel(PC) ← (PC) + size (instr);
IF [(A) ≠ 0] THEN (PC) ← (PC) + rel

Compare and jump if not equalCJNE <src1>, <src2>, rel(PC) ← (PC) + size (instr);
IF [src opnd1 < src opnd2] THEN (CY) ← 1
IF [src opnd1 ≥ src opnd2] THEN (CY) ← 0
IF [src opnd1 ≠ src opnd2] THEN (PC) ← (PC) + rel

Decrement and jump if not zeroDJNZ <dest>, rel(PC) ← (PC) + size (instr); dest opnd ← dest opnd -1;
IF [φ (Z)] THEN (PC) ← (PC) + rel

Mnemonic	<dest>, <src>[1]	Comments	Binary Mode[2]		Source Mode[2]	
			Bytes	States	Bytes	States
JB	bit51, rel	Jump if direct bit is set	3	2/5[3][6]	3	2/5[3][6]
	bit, rel	Jump if direct bit of 8-bit address location is set	5	4/7[3][6]	4	3/6[3][6]
JNB	bit51, rel	Jump if direct bit is not set	3	2/5[3][6]	3	2/5[3][6]
	bit, rel	Jump if direct bit of 8-bit address location is not set	5	4/7[3][6]	4	3/6[3]
JBC	bit51, rel	Jump if direct bit is set & clear bit	3	4/7[5][6]	3	4/7[5][6]
	bit, rel	Jump if direct bit of 8-bit address location is set and clear	5	7/10[5][6]	4	6/9[5][6]
JZ	rel	Jump if ACC is zero	2	2/5[6]	2	2/5[6]
JNZ	rel	Jump if ACC is not zero	2	2/5[6]	2	2/5[6]
CJNE	A, dir8, rel	Compare direct address to ACC and jump if not equal	3	2/5[3][6]	3	2/5[3][6]
	A, #data, rel	Compare immediate to ACC and jump if not equal	3	2/5[6]	3	2/5[6]
	Rn, #data, rel	Compare immediate to register and jump if not equal	3	2/5[6]	4	3/6[6]
	at Ri, #data, rel	Compare immediate to indirect and jump if not equal	3	3/6[6]	4	4/7[6]
DJNZ	Rn, rel	Decrement register and jump if not zero	2	2/5[6]	3	3/6[6]
	dir8, rel	Decrement direct address and jump if not zero	3	3/6[4][6]	3	3/6[4][6]

Notes:
1. A shaded cell denotes an instruction in the C51 Architecture.
2. States are given as jump not-taken/taken.
3. If this instruction addresses an I/O Port (Px, x = 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.
4. If this instruction addresses an I/O Port (Px, x = 0-3), add 2 to the number of states.

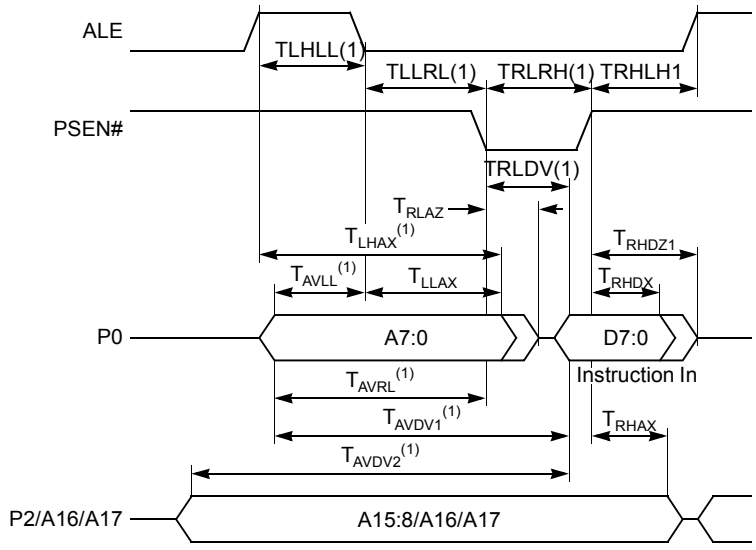
Table 40. Bus Cycles AC Timings; V_{DD} = 2.7 to 5.5 V, T_A = -40 to 85°C

Symbol	Parameter	12 MHz		16 MHz		Unit
		Min	Max	Min	Max	
T_{OSC}	$1/F_{OSC}$	83		62		ns
T_{LHLL}	ALE Pulse Width	72		52		ns(2)
T_{AVLL}	Address Valid to ALE Low	71		51		ns(2)
T_{LLAX}	Address hold after ALE Low	14		6		ns
T_{RLRH}(1)	RD#/PSEN# Pulse Width	163		121		ns(3)
T_{WLWH}	WR# Pulse Width	165		124		ns(3)
T_{LLRL}(1)	ALE Low to RD#/PSEN# Low	17		11		ns
T_{LHAX}	ALE High to Address Hold	90		57		ns(2)
T_{RLDV}(1)	RD#/PSEN# Low to Valid Data		133		92	ns(3)
T_{RHDX}(1)	Data Hold After RD#/PSEN# High	0		0		ns
T_{RHAX}(1)	Address Hold After RD#/PSEN# High	0		0		ns
T_{RLAZ}(1)	RD#/PSEN# Low to Address Float		0		0	ns
T_{RHDZ1}	Instruction Float After RD#/PSEN# High		59		48	ns
T_{RHDZ2}	Data Float After RD#/PSEN# High		225		175	ns
T_{RHLH1}	RD#/PSEN# high to ALE High (Instruction)	60		47		ns
T_{RHLH2}	RD#/PSEN# high to ALE High (Data)	226		172		ns
T_{WHLH}	WR# High to ALE High	226		172		ns
T_{AVDV1}	Address (P0) Valid to Valid Data In		289		160	ns(2)(3)
T_{AVDV2}	Address (P2) Valid to Valid Data In		296		211	ns(2)(3)
T_{AVDV3}	Address (P0) Valid to Valid Instruction In		144		98	ns(3)
T_{AXDX}	Data Hold after Address Hold	0		0		ns
T_{AVRL}(1)	Address Valid to RD# Low	111		64		ns(2)
T_{AVWL1}	Address (P0) Valid to WR# Low	111		64		ns(2)
T_{AVWL2}	Address (P2) Valid to WR# Low	158		116		ns(2)
T_{WHQX}	Data Hold after WR# High	82		66		ns
T_{QVWH}	Data Valid to WR# High	135		103		ns(3)
T_{WHAX}	WR# High to Address Hold	168		125		ns

Notes: 1. Specification for PSEN# are identical to those for RD#.
2. If a wait state is added by extending ALE, add $2 \cdot T_{OSC.}$
3. If wait states are added by extending RD#/PSEN#/WR#, add $2N \cdot T_{OSC}$ (N = 1..3).

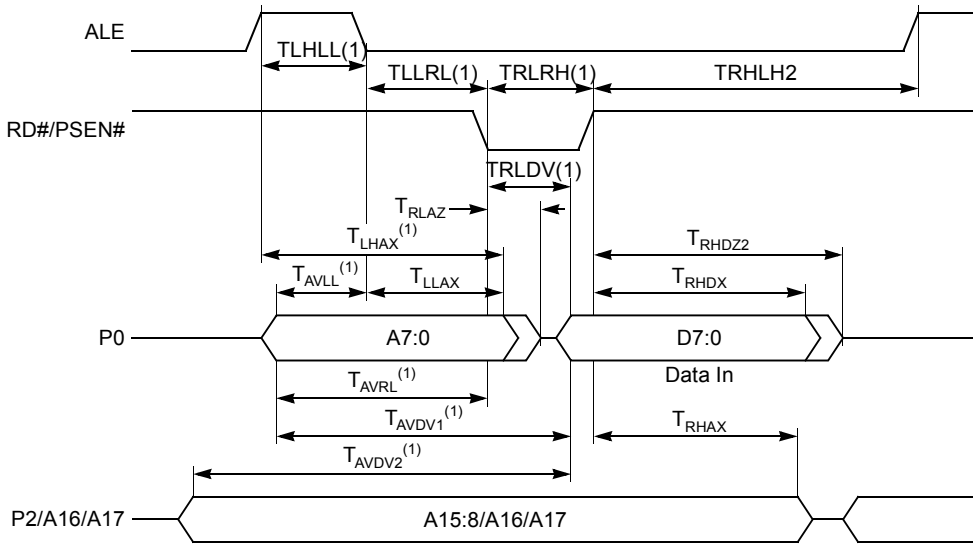
Waveforms in Non-Page Mode

Figure 8. External Bus Cycle: Code Fetch (Non-Page Mode)



Note: 1. The value of this parameter depends on wait states. See Table 39 and Table 40.

Figure 9. External Bus Cycle: Data Read (Non-Page Mode)



Note: 1. The value of this parameter depends on wait states. See Table 39 and Table 40.

AC Characteristics - Real-Time Asynchronous Wait State

Definition of Symbols

Table 43. Real-Time Asynchronous Wait Timing Symbol Definitions

Signals	
S	PSEN#/RD#/WR#
Y	AWAIT#

Conditions	
L	Low
V	Valid
X	No Longer Valid

Timings

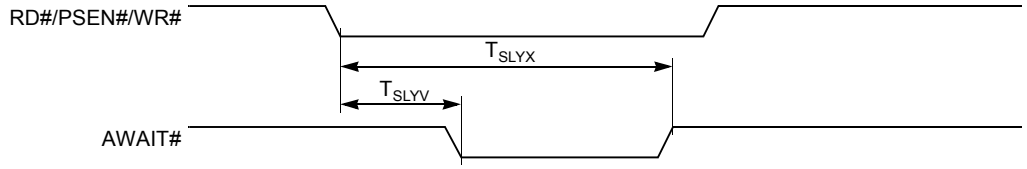
Table 44. Real-Time Asynchronous Wait AC Timings; V_{DD} = 2.7 to 5.5 V, T_A = -40 to 85°C

Symbol	Parameter	Min	Max	Unit
T_{SLYV}	PSEN#/RD#/WR# Low to Wait Set-up		T_{OSC} - 10	ns
T_{SLYX}	Wait Hold after PSEN#/RD#/WR# Low	$(2N-1)\cdot T_{OSC}$ + 10		ns(1)

Note: 1. N is the number of wait states added (N≥ 1).

Waveforms

Figure 16. Real-time Asynchronous Wait State Timings



AC Characteristics - Serial Port in Shift Register Mode

Definition of Symbols

Table 45. Serial Port Timing Symbol Definitions

Signals	
D	Data In
Q	Data Out
X	Clock

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid

DC Characteristics

High Speed Versions - Commercial, Industrial, and Automotive

Table 55. DC Characteristics; V_{DD} = 4.5 to 5.5 V, T_A = -40 to +85°C

Symbol	Parameter	Min	Typical[4]	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (except EA#, SCL, SDA)	-0.5		$0.2 \cdot V_{DD}$ - 0.1	V	
V_{IL1}[5]	Input Low Voltage (SCL, SDA)	-0.5		$0.3 \cdot V_{DD}$	V	
V_{IL2}	Input Low Voltage (EA#)	0		$0.2 \cdot V_{DD}$ - 0.3	V	
V_{IH}	Input high Voltage (except XTAL1, RST, SCL, SDA)	$0.2 \cdot V_{DD}$ + 0.9		V_{DD} + 0.5	V	
V_{IH1}[5]	Input high Voltage (XTAL1, RST, SCL, SDA)	$0.7 \cdot V_{DD}$		V_{DD} + 0.5	V	
V_{OL}	Output Low Voltage (Ports 1, 2, 3)			0.3 0.45 1.0	V	I_{OL} = 100 µA[1][2] I_{OL} = 1.6 mA[1][2] I_{OL} = 3.5 mA[1][2]
V_{OL1}	Output Low Voltage (Ports 0, ALE, PSEN#, Port 2 in Page Mode during External Address)			0.3 0.45 1.0	V	I_{OL} = 200 µA[1][2] I_{OL} = 3.2 mA[1][2] I_{OL} = 7.0 mA[1][2]
V_{OH}	Output high Voltage (Ports 1, 2, 3, ALE, PSEN#)	V_{DD} - 0.3 V_{DD} - 0.7 V_{DD} - 1.5			V	I_{OH} = -10 µA[3] I_{OH} = -30 µA[3] I_{OH} = -60 µA[3]
V_{OH1}	Output high Voltage (Port 0, Port 2 in Page Mode during External Address)	V_{DD} - 0.3 V_{DD} - 0.7 V_{DD} - 1.5			V	I_{OH} = -200 µA I_{OH} = -3.2 mA I_{OH} = -7.0 mA
V_{RET}	V_{DD} data retention limit			1.8	V	
I_{IL0}	Logical 0 Input Current (Ports 1, 2, 3)			- 50	µA	V_{IN} = 0.45 V
I_{IL1}	Logical 1 Input Current (NMI)			+ 50	µA	V_{IN} = V_{DD}
I_{LI}	Input Leakage Current (Port 0)			± 10	µA	0.45 V < V_{IN} < V_{DD}
I_{TL}	Logical 1-to-0 Transition Current (Ports 1, 2, 3 - AWAIT#)			- 650	µA	V_{IN} = 2.0 V
R_{RST}	RST Pull-Down Resistor	40	110	225	kΩ	
C_{IO}	Pin Capacitance		10		pF	T_A = 25°C
I_{DD}	Operating Current		20 25 35	25 30 40	mA	F_{OSC} = 12 MHz F_{OSC} = 16 MHz F_{OSC} = 24 MHz
I_{DL}	Idle Mode Current		5 6.5 9.5	8 10 14	mA	F_{OSC} = 12 MHz F_{OSC} = 16 MHz F_{OSC} = 24 MHz
I_{PD}	Power-Down Current		2	20	µA	V_{RET} < V_{DD} < 5.5 V
V_{PP}	Programming supply voltage	12.5		13	V	T_A = 0 to +40°C
I_{PP}	Programming supply current			75	mA	T_A = 0 to +40°C

Notes: 1. Under steady-state (non-transient) conditions, I_{OL} must be externally limited as follows:

Maximum IOL per port pin: 10 mA

Maximum IOL per 8-bit port:Port 0 26 mA

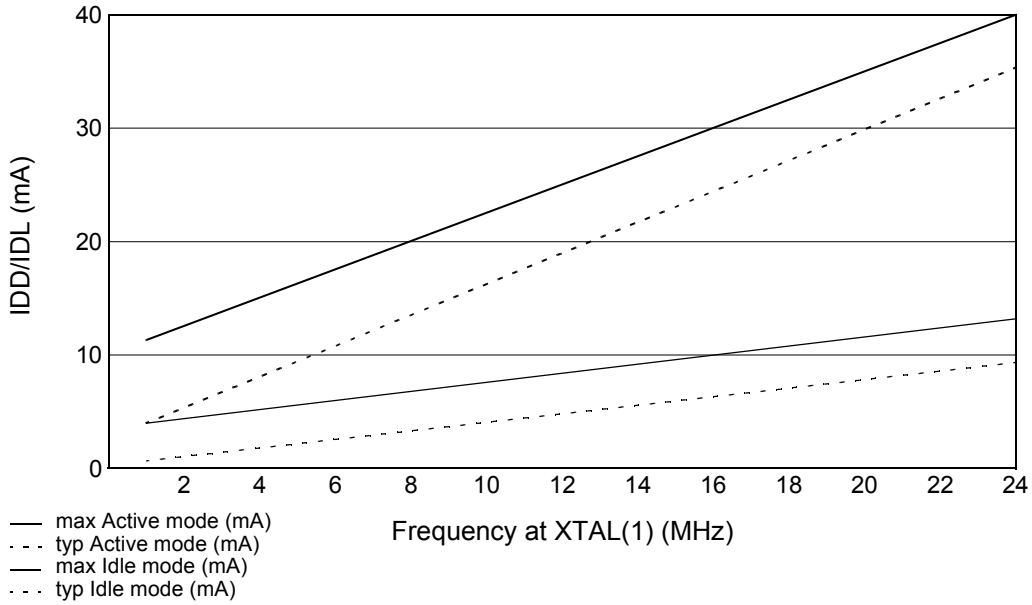
Ports 1-3 15 mA

Maximum Total IOL for all: Output Pins 71 mA

If IOL exceeds the test conditions, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

2. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses above 0.4 V on the low-level outputs of ALE and Ports 1, 2, and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from high to low. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8 V. It may be desirable to qualify ALE or other signals with a Schmitt Trigger or CMOS-level input logic.
3. Capacitive loading on Ports 0 and 2 causes the V_{OH} on ALE and PSEN# to drop below the specification when the address lines are stabilizing.
4. Typical values are obtained using V_{DD} = 5 V and T_A = 25°C. They are not tested and there is not guarantee on these values.
5. The input threshold voltage of SCL and SDA meets the TWI specification, so an input voltage below $0.3 \cdot V_{DD}$ will be recognized as a logic 0 while an input voltage above $0.7 \cdot V_{DD}$ will be recognized as a logic 1.

Figure 28. I_{DD}/I_{DL} Versus Frequency; V_{DD} = 4.5 to 5.5 V



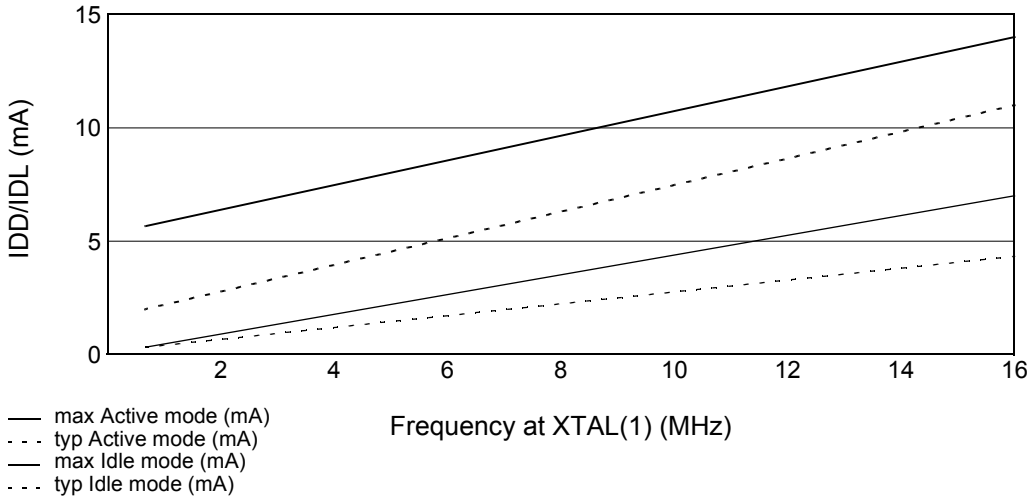
Note: 1. The clock prescaler is not used: $F_{OSC} = F_{XTAL}$.

Maximum Total IOL for all:Output Pins71 mA

If IOL exceeds the test conditions, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

2. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses above 0.4 V on the low-level outputs of ALE and Ports 1, 2, and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from high to low. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8 V. It may be desirable to qualify ALE or other signals with a Schmitt Trigger or CMOS-level input logic.
3. Capacitive loading on Ports 0 and 2 causes the V_{OH} on ALE and PSEN# to drop below the specification when the address lines are stabilizing.
4. Typical values are obtained using V_{DD} = 3 V and T_A = 25°C. They are not tested and there is not guarantee on these values.
5. The input threshold voltage of SCL and SDA meets the TWI specification, so an input voltage below $0.3 \cdot V_{DD}$ will be recognized as a logic 0 while an input voltage above $0.7 \cdot V_{DD}$ will be recognized as a logic 1.

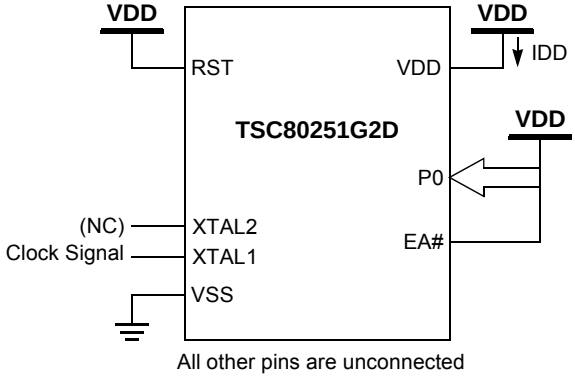
Figure 29. I_{DD}/I_{DL} Versus X_{TAL} Frequency; V_{DD} = 2.7 to 3.6 V



Note: 1.The clock prescaler is not used: $F_{OSC} = F_{XTAL}$.

I_{DD}, I_{DL} and I_{PD} Test Conditions

Figure 30. I_{DD} Test Condition, Active Mode



Packages

List of Packages

- PDIL 40
- CDIL 40 with window
- PLCC 44
- CQPJ 44 with window
- VQFP 44 (10x10)

PDIL 40 - Mechanical Outline

Figure 33. Plastic Dual In Line

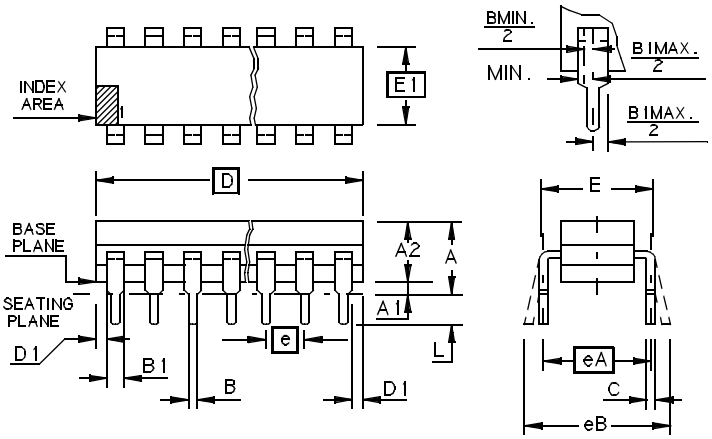


Table 57. PDIL Package Size

	MM		Inch	
	Min	**Max**	**Min**	**Max**
A	-	5.08	-	.200
A1	0.38	-	.015	-
A2	3.18	4.95	.125	.195
B	0.36	0.56	.014	.022
B1	0.76	1.78	.030	.070
C	0.20	0.38	.008	.015
D	50.29	53.21	1.980	2.095
E	15.24	15.87	.600	.625
E1	12.32	14.73	.485	.580
e	2.54 B.S.C.		.100 B.S.C.	
eA	15.24 B.S.C.		.600 B.S.C.	
eB	-	17.78	-	.700
L	2.93	3.81	.115	.150
D1	0.13	-	.005	-

CDIL 40 with Window - Mechanical Outline

Figure 34. Ceramic Dual In Line

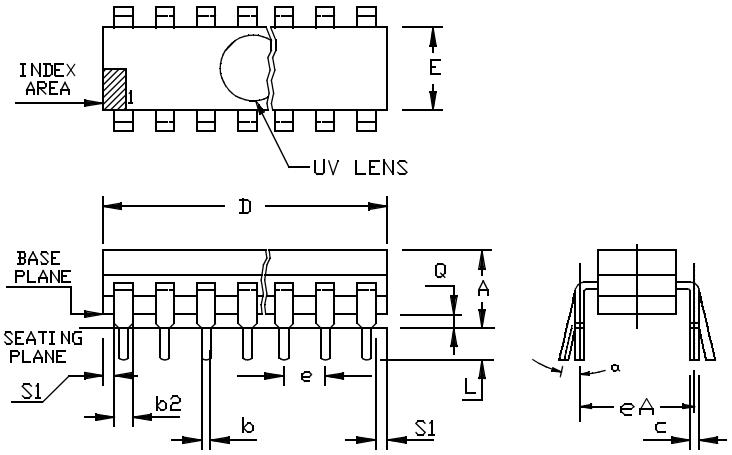


Table 58. CDIL Package Size

	MM		Inch	
	Min	**Max**	**Min**	**Max**
A	-	5.71	-	.225
b	0.36	0.58	.014	.023
b2	1.14	1.65	.045	.065
c	0.20	0.38	.008	.015
D	-	53.47	-	2.105
E	13.06	15.37	.514	.605
e	2.54 B.S.C.		.100 B.S.C.	
eA	15.24 B.S.C.		.600 B.S.C.	
L	3.18	5.08	.125	.200
Q	0.38	1.40	.015	.055
S1	0.13	-	.005	-
a	0 - 15		0 - 15	
N	40			

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