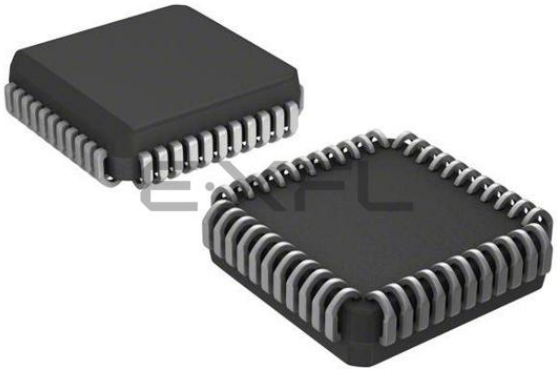

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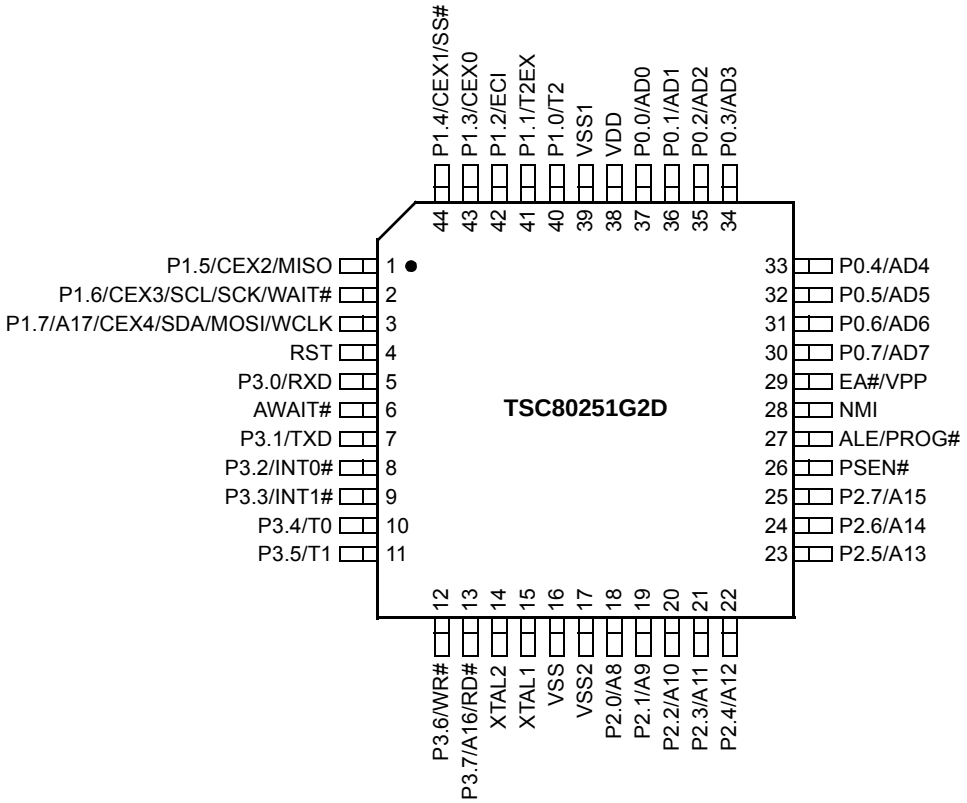
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C251
Core Size	8/16-Bit
Speed	16MHz
Connectivity	EBI/EMI, I²C, Microwire, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.6x16.6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/tsc80251g2d-16cbr

Figure 3. TSC80251G2D 44-pin VQFP Package



compatibility with the C51 Architecture). When PC increments beyond the end of segment FE:, it continues at the reset address FF:0000h (linearity). When PC increments beyond the end of segment 01:, it loops to the beginning of segment 00: (this prevents from its going into the reserved area).

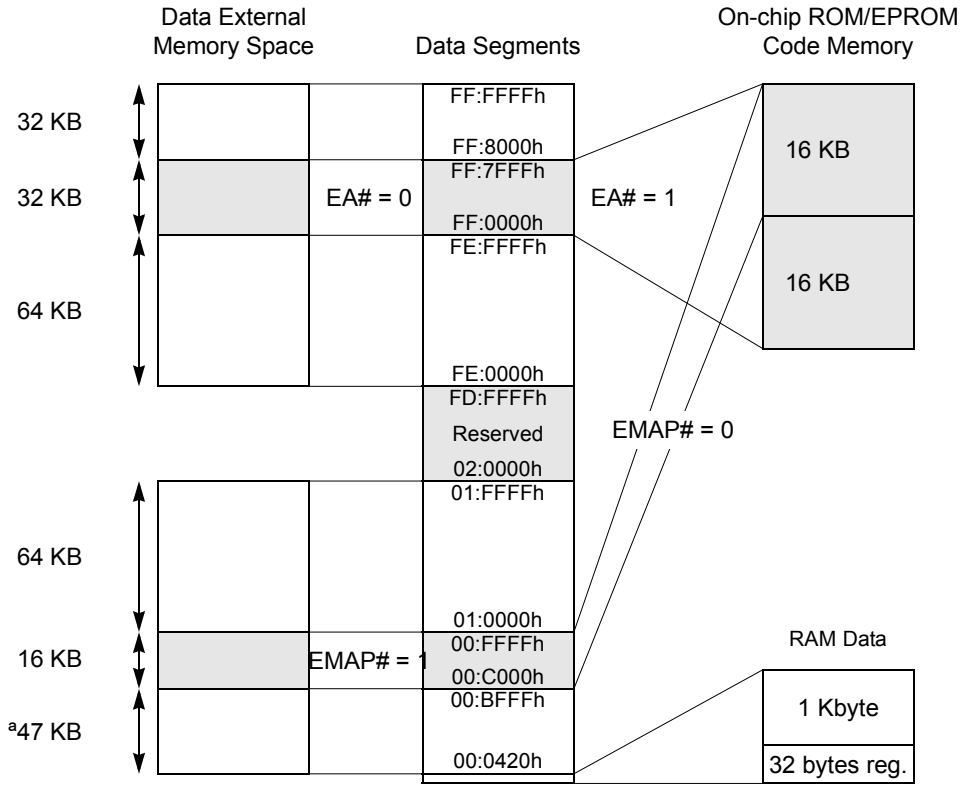
Data Memory

The TSC80251G2D derivatives implement 1 Kbyte of on-chip data RAM. Figure 5 shows the split of the internal and external data memory spaces. This memory is mapped in the data space just over the 32 bytes of registers area (see TSC80251 Programmers' Guide). Hence, the part of the on-chip RAM located from 20h to FFh is bit addressable. This on-chip RAM is not accessible through the program/code memory space.

For faster computation with the on-chip ROM/EPROM code of the TSC83251G2D/TSC87251G2D, its upper 16 KB are also mapped in the upper part of the region 00: if the On-Chip Code Memory Map configuration bit is cleared (EMAP# bit in UCONFIG1 byte, see Figure). However, if EA# is tied to a low level, the TSC80251G2D derivative is running as a ROMless product and the code is actually fetched in the corresponding external memory (i.e. the upper 16 KB of the lower 32 KB of the segment FF:). If EMAP# bit is set, the on-chip ROM is not accessible through the region 00:.

All the accesses to the portion of the data space with no on-chip memory mapped onto are redirected to the external memory.

Figure 5. Data Memory Mapping



4135F–8051–11/06

Instruction Set Summary

This section contains tables that summarize the instruction set. For each instruction there is a short description, its length in bytes, and its execution time in states (one state time is equal to two system clock cycles). There are two concurrent processes limiting the effective instruction throughput:

- Instruction Fetch
- Instruction Execution

Table 20 to Table 32 assume code executing from on-chip memory, then the CPU is fetching 16-bit at a time and this is never limiting the execution speed.

If the code is fetched from external memory, a pre-fetch queue will store instructions ahead of execution to optimize the memory bandwidth usage when slower instructions are executed. However, the effective speed may be limited depending on the average size of instructions (for the considered section of the program flow). The maximum average instruction throughput is provided by Table 14 depending on the external memory configuration (from Page Mode to Non-Page Mode and the maximum number of wait states). If the average size of instructions is not an integer, the maximum effective throughput is found by pondering the number of states for the neighbor integer values.

Table 14. Minimum Number of States per Instruction for given Average Sizes

Average size of Instructions (bytes)	Page Mode (states)	Non-page Mode (states)				
		0 Wait State	1 Wait State	2 Wait States	3 Wait States	4 Wait States
1	1	2	3	4	5	6
2	2	4	6	8	10	12
3	3	6	9	12	15	18
4	4	8	12	16	20	24
5	5	10	15	20	25	30

If the average execution time of the considered instructions is larger than the number of states given by Table 14, this larger value will prevail as the limiting factor. Otherwise, the value from Table 14 must be taken. This is providing a fair estimation of the execution speed but only the actual code execution can provide the final value.

Notation for Instruction Operands

Table 15 to Table 19 provide notation for Instruction Operands.

Table 15. Notation for Direct Addressing

Direct Address	Description	C251	C51
dir8	A direct 8-bit address. This can be a memory address (00h-7Fh) or a SFR address (80h-FFh). It is a byte (default), word or double word depending on the other operand.	3	3
dir16	A 16-bit memory address (00:0000h-00:FFFFh) used in direct addressing.	3	–

Size and Execution Time for Instruction Families

Table 20. Summary of Add and Subtract Instructions

AddADD <dest>, <src>dest opnd ← dest opnd + src opnd SubtractSUB <dest>, <src>dest opnd ← dest opnd - src opnd Add with CarryADDC <dest>, <src>(A) ← (A) + src opnd + (CY) Subtract with BorrowSUBB <dest>, <src>(A) ← (A) - src opnd - (CY)						
Mnemonic	**<dest>, <src>(1)**	**Comments**	**Binary Mode**		**Source Mode**	
			Bytes	**States**	**Bytes**	**States**
ADD	A, Rn	Register to ACC	1	1	2	2
	A, dir8	Direct address to ACC	2	1(2)	2	1(2)
	A, at Ri	Indirect address to ACC	1	2	2	3
	A, #data	Immediate data to ACC	2	1	2	1
ADD/SUB	Rmd, Rms	Byte register to/from byte register	3	2	2	1
	WRjd, WRjs	Word register to/from word register	3	3	2	2
	DRkd, DRks	Dword register to/from dword register	3	5	2	4
	Rm, #data	Immediate 8-bit data to/from byte register	4	3	3	2
	WRj, #data16	Immediate 16-bit data to/from word register	5	4	4	3
	DRk, #0data16	16-bit unsigned immediate data to/from dword register	5	6	4	5
	Rm, dir8	Direct address (on-chip RAM or SFR) to/from byte register	4	3(2)	3	2(2)
	WRj, dir8	Direct address (on-chip RAM or SFR) to/from word register	4	4	3	3
	Rm, dir16	Direct address (64K) to/from byte register	5	3(3)	4	2(3)
	WRj, dir16	Direct address (64K) to/from word register	5	4(4)	4	3(4)
	Rm, at WRj	Indirect address (64K) to/from byte register	4	3(3)	3	2(3)
	Rm, at DRk	Indirect address (16M) to/from byte register	4	4(3)	3	3(3)
ADDC/SUBB	A, Rn	Register to/from ACC with carry	1	1	2	2
	A, dir8	Direct address (on-chip RAM or SFR) to/from ACC with carry	2	1(2)	2	1(2)
	A, at Ri	Indirect address to/from ACC with carry	1	2	2	3
	A, #data	Immediate data to/from ACC with carry	2	1	2	1

Notes:
1. A shaded cell denotes an instruction in the C51 Architecture.
2. If this instruction addresses an I/O Port (Px, x = 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.
3. If this instruction addresses external memory location, add N+2 to the number of states (N: number of wait states).

Table 22. Summary of Compare Instructions

CompareCMP <dest>, <src>dest opnd - src opnd						
			Binary Mode		Source Mode	
Mnemonic	**<dest>, <src>(2)**	**Comments**	**Bytes**	**States**	**Bytes**	**States**
CMP	Rmd, Rms	Register with register	3	2	2	1
	WRjd, WRjs	Word register with word register	3	3	2	2
	DRkd, DRks	Dword register with dword register	3	5	2	4
	Rm, #data	Register with immediate data	4	3	3	2
	WRj, #data16	Word register with immediate 16-bit data	5	4	4	3
	DRk, #0data16	Dword register with zero-extended 16-bit immediate data	5	6	4	5
	DRk, #1data16	Dword register with one-extended 16-bit immediate data	5	6	4	5
	Rm, dir8	Direct address (on-chip RAM or SFR) with byte register	4	3(1)	3	2(1)
	WRj, dir8	Direct address (on-chip RAM or SFR) with word register	4	4	3	3
	Rm, dir16	Direct address (64K) with byte register	5	3(2)	4	2(2)
	WRj, dir16	Direct address (64K) with word register	5	4(3)	4	3(3)
	Rm, at WRj	Indirect address (64K) with byte register	4	3(2)	3	2(2)
	Rm, at DRk	Indirect address (16M) with byte register	4	4(2)	3	3(2)

Notes:
1. If this instruction addresses an I/O Port (Px, x = 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.
2. If this instruction addresses external memory location, add N+2 to the number of states (N: number of wait states).
3. If this instruction addresses external memory location, add 2(N+2) to the number of states (N: number of wait states).

Notes: 1. Logical instructions that affect a bit are in Table 27.
2. A shaded cell denotes an instruction in the C51 Architecture.
3. If this instruction addresses an I/O Port (Px, x = 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.
4. If this instruction addresses an I/O Port (Px, x = 0-3), add 2 to the number of states. Add 3 if it addresses a Peripheral SFR.
5. If this instruction addresses external memory location, add N+2 to the number of states (N: number of wait states).
6. If this instruction addresses external memory location, add 2(N+2) to the number of states (N: number of wait states).

Table 23. Summary of Logical Instructions (2/2)

Shift Left LogicalSLL <dest><dest>$_0 \leftarrow 0$
<dest>$_{n+1} \leftarrow$ <dest>$_n$, n = 0..msb-1
(CY) $\leftarrow$ <dest>$_{msb}$
Shift Right ArithmeticSRA <dest><dest>$_{msb} \leftarrow$ <dest>$_{msb}$
<dest>$_{n-1} \leftarrow$ <dest>$_n$, n = msb..1
(CY) $\leftarrow$ <dest>$_0$
Shift Right LogicalSRL <dest><dest>$_{msb} \leftarrow 0$
<dest>$_{n-1} \leftarrow$ <dest>$_n$, n = msb..1
(CY) $\leftarrow$ <dest>$_0$
SwapSWAP $AA_{3:0}$ $A_{7:4}$

Mnemonic	<dest>, <src>(1)	Comments	Binary Mode		Source Mode	
			Bytes	States	Bytes	States
SLL	Rm	Shift byte register left through the MSB	3	2	2	1
	WRj	Shift word register left through the MSB	3	2	2	1
SRA	Rm	Shift byte register right	3	2	2	1
	WRj	Shift word register right	3	2	2	1
SRL	Rm	Shift byte register left	3	2	2	1
	WRj	Shift word register left	3	2	2	1
SWAP	A	Swap nibbles within ACC	1	2	1	2

Note: 1. A shaded cell denotes an instruction in the C51 Architecture.

Table 27. Summary of Bit Instructions

Clear BitCLR <dest>dest opnd ← 0						
Set BitSETB <dest>dest opnd ← 1						
Complement BitCPL <dest>dest opnd ← ∅ bit						
AND Carry with BitANL CY, <src>(CY) ← (CY) ∧ src opnd						
AND Carry with Complement of BitANL CY, /<src>(CY) ← (CY) ∧ ∅ src opnd						
OR Carry with BitORL CY, <src>(CY) ← (CY) ∨ src opnd						
OR Carry with Complement of BitORL CY, /<src>(CY) ← (CY) ∨ ∅ src opnd						
Move Bit to CarryMOV CY, <src>(CY) ← src opnd						
Move Bit from CarryMOV <dest>, CYdest opnd ← (CY)						
Mnemonic	**<dest>, <src>(1)**	**Comments**	**Binary Mode**		**Source Mode**	
			Bytes	**States**	**Bytes**	**States**
CLR	CY	Clear carry	1	1	1	1
	bit51	Clear direct bit	2	2(3)	2	2(3)
	bit	Clear direct bit	4	4(3)	3	3(3)
SETB	CY	Set carry	1	1	1	1
	bit51	Set direct bit	2	2(3)	2	2(3)
	bit	Set direct bit	4	4(3)	3	3(3)
CPL	CY	Complement carry	1	1	1	1
	bit51	Complement direct bit	2	2(3)	2	2(3)
	bit	Complement direct bit	4	4(3)	3	3(3)
ANL	CY, bit51	And direct bit to carry	2	1(2)	2	1(2)
	CY, bit	And direct bit to carry	4	3(2)	3	2(2)
	CY, /bit51	And complemented direct bit to carry	2	1(2)	2	1(2)
	CY, /bit	And complemented direct bit to carry	4	3(2)	3	2(2)
ORL	CY, bit51	Or direct bit to carry	2	1(2)	2	1(2)
	CY, bit	Or direct bit to carry	4	3(2)	3	2(2)
	CY, /bit51	Or complemented direct bit to carry	2	1(2)	2	1(2)
	CY, /bit	Or complemented direct bit to carry	4	3(2)	3	2(2)
MOV	CY, bit51	Move direct bit to carry	2	1(2)	2	1(2)
	CY, bit	Move direct bit to carry	4	3(2)	3	2(2)
	bit51, CY	Move carry to direct bit	2	2(3)	2	2(3)
	bit, CY	Move carry to direct bit	4	4(3)	3	3(3)

Notes:
1. A shaded cell denotes an instruction in the C51 Architecture.
2. If this instruction addresses an I/O Port (Px, x = 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.
3. If this instruction addresses an I/O Port (Px, x = 0-3), add 2 to the number of states. Add 3 if it addresses a Peripheral SFR.

Table 28. Summary of Exchange, Push and Pop Instructions

Exchange bytesXCH A, <src>(A) ↔ src opnd Exchange DigitXCHD A, <src>$(A)_{3:0}$ ↔ src $opnd_{3:0}$ PushPUSH <src>(SP) ← (SP) +1; ((SP)) ← src opnd; (SP) ← (SP) + size (src opnd) - 1 PopPOP <dest>(SP) ← (SP) - size (dest opnd) + 1; dest opnd ← ((SP)); (SP) ← (SP) -1						
Mnemonic	**<dest>, <src>(1)**	**Comments**	**Binary Mode**		**Source Mode**	
			Bytes	**States**	**Bytes**	**States**
XCH	A, Rn	ACC and register	1	3	2	4
	A, dir8	ACC and direct address (on-chip RAM or SFR)	2	3(3)	2	3(3)
	A, at Ri	ACC and indirect address	1	4	2	5
XCHD	A, at Ri	ACC low nibble and indirect address (256 bytes)	1	4	2	5
PUSH	dir8	Push direct address onto stack	2	2(2)	2	2(2)
	#data	Push immediate data onto stack	4	4	3	3
	#data16	Push 16-bit immediate data onto stack	5	5	4	5
	Rm	Push byte register onto stack	3	4	2	3
	WRj	Push word register onto stack	3	5	2	4
	DRk	Push double word register onto stack	3	9	2	8
POP	dir8	Pop direct address (on-chip RAM or SFR) from stack	2	3(2)	2	3(2)
	Rm	Pop byte register from stack	3	3	2	2
	WRj	Pop word register from stack	3	5	2	4
	DRk	Pop double word register from stack	3	9	2	8

Notes:
1. A shaded cell denotes an instruction in the C51 Architecture.
2. If this instruction addresses an I/O Port (Px, x = 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.
3. If this instruction addresses an I/O Port (Px, x = 0-3), add 2 to the number of states. Add 3 if it addresses a Peripheral SFR.

Add 3 if it addresses a Peripheral SFR.

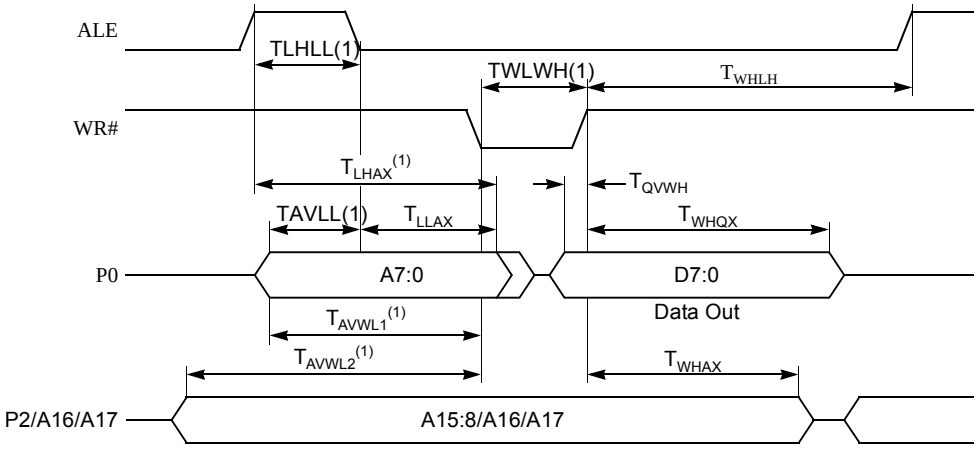
5. If this instruction addresses an I/O Port (Px, x = 0-3), add 3 to the number of states. Add 5 if it addresses a Peripheral SFR.
6. In internal execution only, add 1 to the number of states of the 'jump taken' if the destination address is internal and odd.

Table 31. Summary of Unconditional Jump Instructions

Absolute jumpAJMP <src>(PC) ← (PC) +2; $(PC)_{10:0}$ ← src opnd						
Extended jumpEJMP <src>(PC) ← (PC) + size (instr); $(PC)_{23:0}$ ← src opnd						
Long jumpLJMP <src>(PC) ← (PC) + size (instr); $(PC)_{15:0}$ ← src opnd						
Short jumpSJMP rel(PC) ← (PC) +2; (PC) ← (PC) +rel						
Jump indirectJMP at A +DPTR$(PC)_{23:16}$ ← FFh; $(PC)_{15:0}$ ← (A) + (DPTR)						
No operationNOP(PC) ← (PC) +1						
Mnemonic	**<dest>, <src>(1)**	**Comments**	**Binary Mode**		**Source Mode**	
			Bytes	**States**	**Bytes**	**States**
AJMP	addr11	Absolute jump	2	3(2)(3)	2	3(2)(3)
EJMP	addr24	Extended jump	5	6(2)(4)	4	5(2)(4)
	at DRk	Extended jump (indirect)	3	7(2)(4)	2	6(2)(4)
LJMP	at WRj	Long jump (indirect)	3	6(2)(4)	2	5(2)(4)
	addr16	Long jump (direct address)	3	5(2)(4)	3	5(2)(4)
SJMP	rel	Short jump (relative address)	2	4(2)(4)	2	4(2)(4)
JMP	at A +DPTR	Jump indirect relative to the DPTR	1	5(2)(4)	1	5(2)(4)
NOP		No operation (Jump never)	1	1	1	1

Notes:
1. A shaded cell denotes an instruction in the C51 Architecture.
2. In internal execution only, add 1 to the number of states if the destination address is internal and odd.
3. Add 2 to the number of states if the destination address is external.
4. Add 3 to the number of states if the destination address is external.

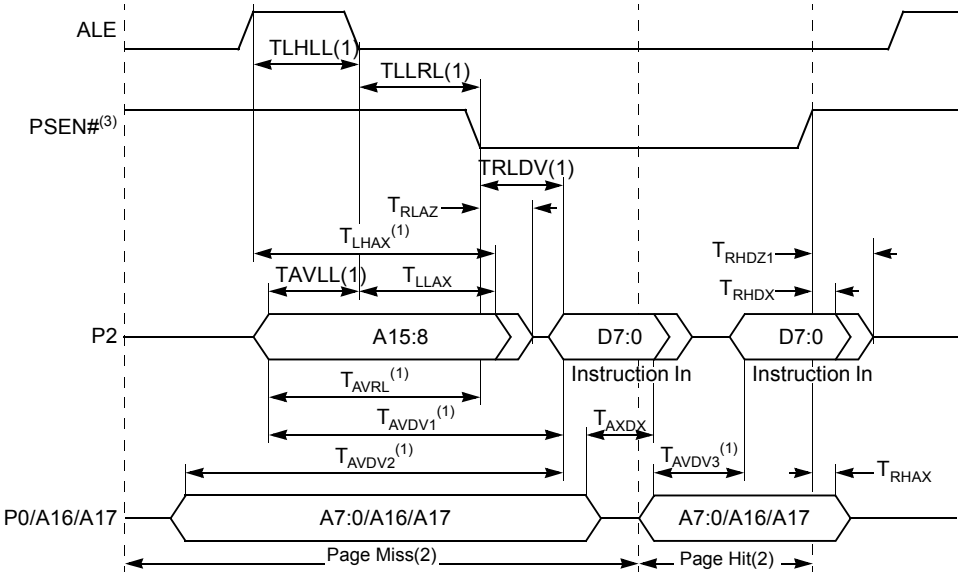
Figure 10. External Bus Cycle: Data Write (Non-Page Mode)



Note: 1. The value of this parameter depends on wait states. See Table 39 and Table 40.

Waveforms in Page Mode

Figure 11. External Bus Cycle: Code Fetch (Page Mode)



Note: 1. The value of this parameter depends on wait states. See Table 39 and Table 40.
2. A page hit (i.e., a code fetch to the same 256-byte “page” as the previous code fetch) requires one state ($2 \cdot T_{OSC}$);
a page miss requires two states ($4 \cdot T_{OSC}$).
3. During a sequence of page hits, PSEN# remains low until the end of the last page-hit cycle.

AC Characteristics - SSLC: TWI Interface

Timings

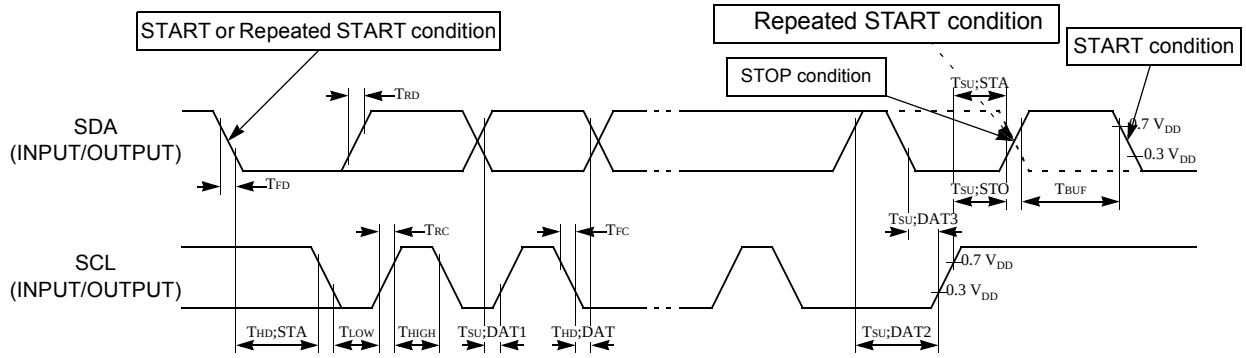
Table 47. TWI Interface AC Timing; V_{DD} = 2.7 to 5.5 V, T_A = -40 to 85°C

Symbol	Parameter	INPUT Min	INPUT Max	OUTPUT Min	OUTPUT Max
T_{HD}; STA	Start condition hold time	14·T_{CLCL}(4)		4.0 µs(1)	
T_{LOW}	SCL low time	16·T_{CLCL}(4)		4.7 µs(1)	
T_{HIGH}	SCL high time	14·T_{CLCL}(4)		4.0 µs(1)	
T_{RC}	SCL rise time	1 µs		-(2)	
T_{FC}	SCL fall time	0.3 µs		0.3 µs(3)	
T_{SU}; DAT1	Data set-up time	250 ns		20·T_{CLCL}(4)- T_{RD}	
T_{SU}; DAT2	SDA set-up time (before repeated START condition)	250 ns		1 µs(1)	
T_{SU}; DAT3	SDA set-up time (before STOP condition)	250 ns		8·T_{CLCL}(4)	
T_{HD}; DAT	Data hold time	0 ns		8·T_{CLCL}(4) - T_{FC}	
T_{SU}; STA	Repeated START set-up time	14·T_{CLCL}(4)		4.7 µs(1)	
T_{SU}; STO	STOP condition set-up time	14·T_{CLCL}(4)		4.0 µs(1)	
T_{BUF}	Bus free time	14·T_{CLCL}(4)		4.7 µs(1)	
T_{RD}	SDA rise time	1 µs		-(2)	
T_{FD}	SDA fall time	0.3 µs		0.3 µs(3)	

Notes:
1. At 100 kbit/s. At other bit-rates this value is inversely proportional to the bit-rate of 100 kbit/s.
2. Determined by the external bus-line capacitance and the external bus-line pull-up resistor, this must be < 1 µs.
3. Spikes on the SDA and SCL lines with a duration of less than 3·T_{CLCL} will be filtered out. Maximum capacitance on bus-lines SDA and SCL = 400 pF.
4. T_{CLCL} = T_{OSC} = one oscillator clock period.

Waveforms

Figure 18. TWI Waveforms



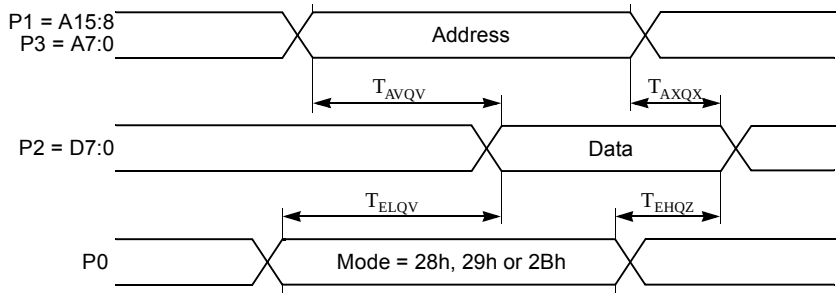
Timings

Table 49. SPI Interface AC Timing; V_{DD} = 2.7 to 5.5 V, T_A = -40 to 85°C

Symbol	Parameter	Min	Max	Unit
Slave Mode(1)				
T_{CHCH}	Clock Period	8		T_{OSC}
T_{CHCX}	Clock High Time	3.2		T_{OSC}
T_{CLCX}	Clock Low Time	3.2		T_{OSC}
T_{SLCH}, T_{SLCL}	SS# Low to Clock edge	200		ns
T_{IVCL}, T_{IVCH}	Input Data Valid to Clock Edge	100		ns
T_{CLIX}, T_{CHIX}	Input Data Hold after Clock Edge	100		ns
$T_{CLOV,}$ T_{CHOV}	Output Data Valid after Clock Edge		100	ns
T_{CLOX}, T_{CHOX}	Output Data Hold Time after Clock Edge	0		ns
T_{CLSH}, T_{CHSH}	SS# High after Clock Edge	0		ns
T_{IVCL}, T_{IVCH}	Input Data Valid to Clock Edge	100		ns
T_{CLIX}, T_{CHIX}	Input Data Hold after Clock Edge	100		ns
T_{SLOV}	SS# Low to Output Data Valid		130	ns
T_{SHOX}	Output Data Hold after SS# High		130	ns
T_{SHSL}	SS# High to SS# Low	(2)		
T_{ILIH}	Input Rise Time		2	µs
T_{IHIL}	Input Fall Time		2	µs
T_{OLOH}	Output Rise time		100	ns
T_{OHOL}	Output Fall Time		100	ns
Master Mode(3)				
T_{CHCH}	Clock Period	4		T_{OSC}
T_{CHCX}	Clock High Time	1.6		T_{OSC}
T_{CLCX}	Clock Low Time	1.6		T_{OSC}
T_{IVCL}, T_{IVCH}	Input Data Valid to Clock Edge	50		ns
T_{CLIX}, T_{CHIX}	Input Data Hold after Clock Edge	50		ns
$T_{CLOV,}$ T_{CHOV}	Output Data Valid after Clock Edge		65	ns
T_{CLOX}, T_{CHOX}	Output Data Hold Time after Clock Edge	0		ns
T_{ILIH}	Input Data Rise Time		2	µs
T_{IHIL}	Input Data Fall Time		2	µs
T_{OLOH}	Output Data Rise time		50	ns
T_{OHOL}	Output Data Fall Time		50	ns

Notes: 1. Capacitive load on all pins = 200 pF in slave mode.
2. The value of this parameter depends on software.
3. Capacitive load on all pins = 100 pF in master mode.

Figure 24. EPROM Verifying Waveforms



AC Characteristics - External Clock Drive and Logic Level References

Definition of Symbols

Table 53. External Clock Timing Symbol Definitions

Signals	
C	Clock

Conditions	
H	High
L	Low
X	No Longer Valid

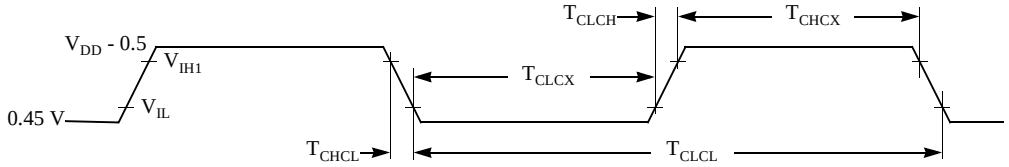
Timings

Table 54. External Clock AC Timings; V_{DD} = 4.5 to 5.5 V, T_A = -40 to +85°C

Symbol	Parameter	Min	Max	Unit
F_{OSC}	Oscillator Frequency		24	MHz
T_{CHCX}	High Time	10		ns
T_{CLCX}	Low Time	10		ns
T_{CLCH}	Rise Time	3		ns
T_{CHCL}	Fall Time	3		ns

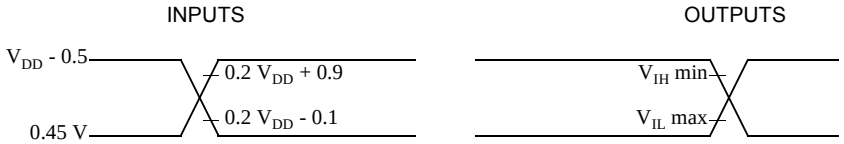
Waveforms

Figure 25. External Clock Waveform



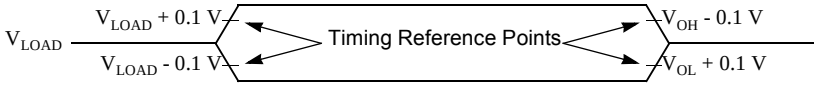
Notes: 1. During AC testing, all inputs are driven at V_{DD} -0.5 V for a logic 1 and 0.45 V for a logic 0.
2. Timing measurements are made on all outputs at V_{IH} min for a logic 1 and V_{IL} max for a logic 0.

Figure 26. AC Testing Input/Output Waveforms



Note: For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loading V_{OH}/V_{OL} level occurs with I_{OL}/I_{OH} = ±20 mA.

Figure 27. Float Waveforms



Absolute Maximum Rating and Operating Conditions

Absolute Maximum Ratings

Storage Temperature ..... -65 to +150°C Voltage on any other Pin to VSS ..... -0.5 to +6.5 V I_{OL} per I/O Pin ..... 15 mA Power Dissipation ..... 1.5 W Ambient Temperature Under Bias Commercial.....0 to +70°C Industrial ..... -40 to +85°C Automotive..... -40 to +85°C V_{DD} High Speed versions..... 4.5 to 5.5 V Low Voltage versions..... 2.7 to 5.5 V	*NOTICE: Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only. Operation beyond the “operating conditions” is not recommended and extended exposure beyond the “Operating Conditions” may affect device reliability.

Notes: 1. Under steady-state (non-transient) conditions, I_{OL} must be externally limited as follows:

Maximum IOL per port pin: 10 mA

Maximum IOL per 8-bit port:Port 0 26 mA

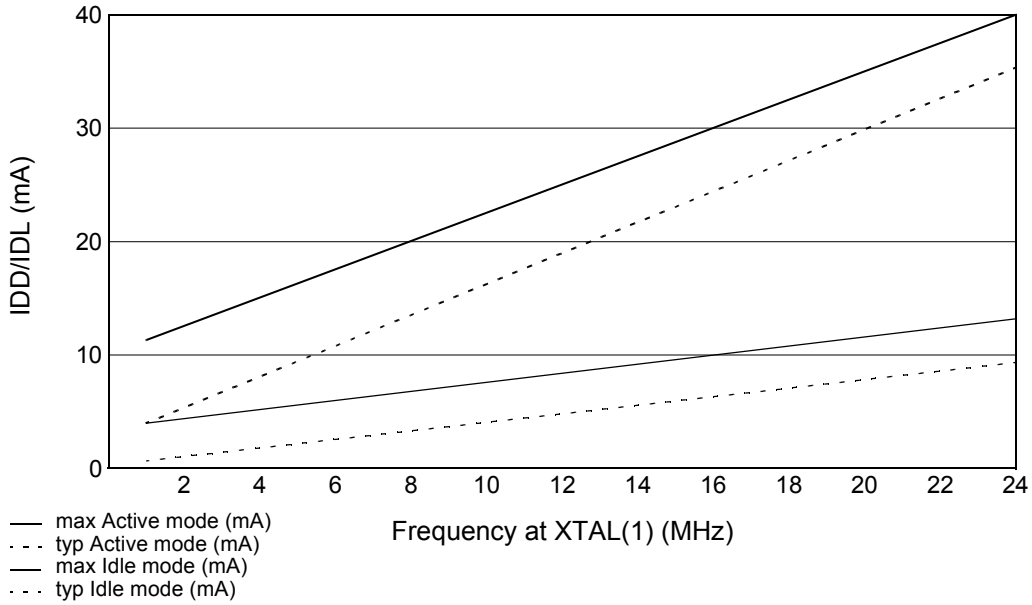
Ports 1-3 15 mA

Maximum Total IOL for all: Output Pins 71 mA

If IOL exceeds the test conditions, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

2. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses above 0.4 V on the low-level outputs of ALE and Ports 1, 2, and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from high to low. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8 V. It may be desirable to qualify ALE or other signals with a Schmitt Trigger or CMOS-level input logic.
3. Capacitive loading on Ports 0 and 2 causes the V_{OH} on ALE and PSEN# to drop below the specification when the address lines are stabilizing.
4. Typical values are obtained using V_{DD} = 5 V and T_A = 25°C. They are not tested and there is not guarantee on these values.
5. The input threshold voltage of SCL and SDA meets the TWI specification, so an input voltage below $0.3 \cdot V_{DD}$ will be recognized as a logic 0 while an input voltage above $0.7 \cdot V_{DD}$ will be recognized as a logic 1.

Figure 28. I_{DD}/I_{DL} Versus Frequency; V_{DD} = 4.5 to 5.5 V



Note: 1. The clock prescaler is not used: $F_{OSC} = F_{XTAL}$.

CDIL 40 with Window - Mechanical Outline

Figure 34. Ceramic Dual In Line

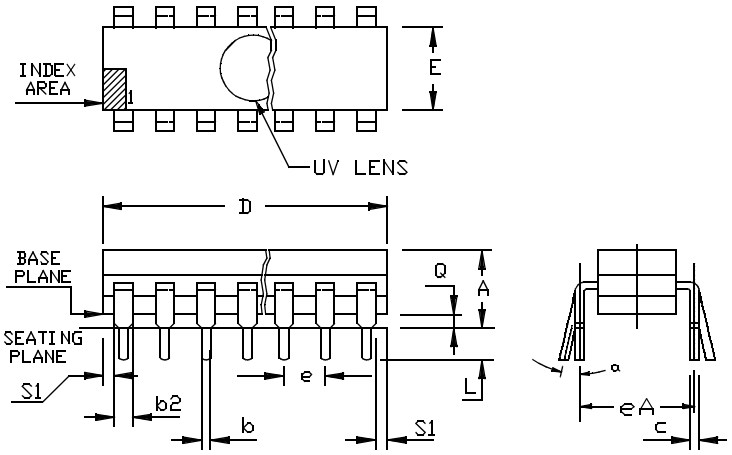


Table 58. CDIL Package Size

	MM		Inch	
	Min	**Max**	**Min**	**Max**
A	-	5.71	-	.225
b	0.36	0.58	.014	.023
b2	1.14	1.65	.045	.065
c	0.20	0.38	.008	.015
D	-	53.47	-	2.105
E	13.06	15.37	.514	.605
e	2.54 B.S.C.		.100 B.S.C.	
eA	15.24 B.S.C.		.600 B.S.C.	
L	3.18	5.08	.125	.200
Q	0.38	1.40	.015	.055
S1	0.13	-	.005	-
a	0 - 15		0 - 15	
N	40			

PLCC 44 - Mechanical Outline

Figure 35. Plastic Lead Chip Carrier

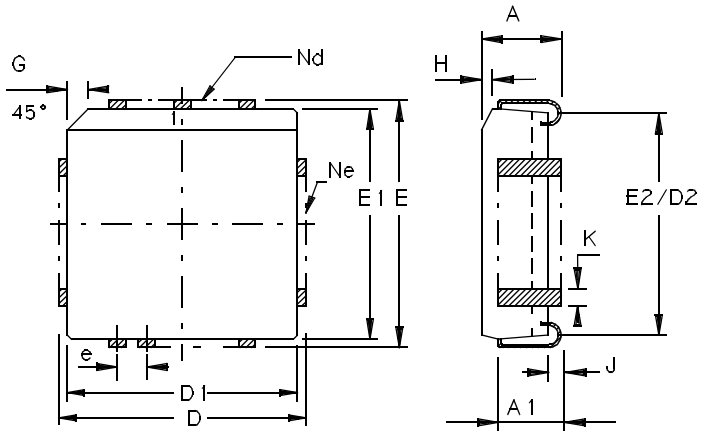


Table 59. PLCC Package Size

	MM		Inch	
	Min	**Max**	**Min**	**Max**
A	4.20	4.57	.165	.180
A1	2.29	3.04	.090	.120
D	17.40	17.65	.685	.695
D1	16.44	16.66	.647	.656
D2	14.99	16.00	.590	.630
E	17.40	17.65	.685	.695
E1	16.44	16.66	.647	.656
E2	14.99	16.00	.590	.630
e	1.27 BSC		.050 BSC	
G	1.07	1.22	.042	.048
H	1.07	1.42	.042	.056
J	0.51	-	.020	-
K	0.33	0.53	.013	.021
Nd	11		11	
Ne	11		11	

VQFP 44 (10x10) - Mechanical Outline

Figure 37. Shrink Quad Flat Pack (Plastic)

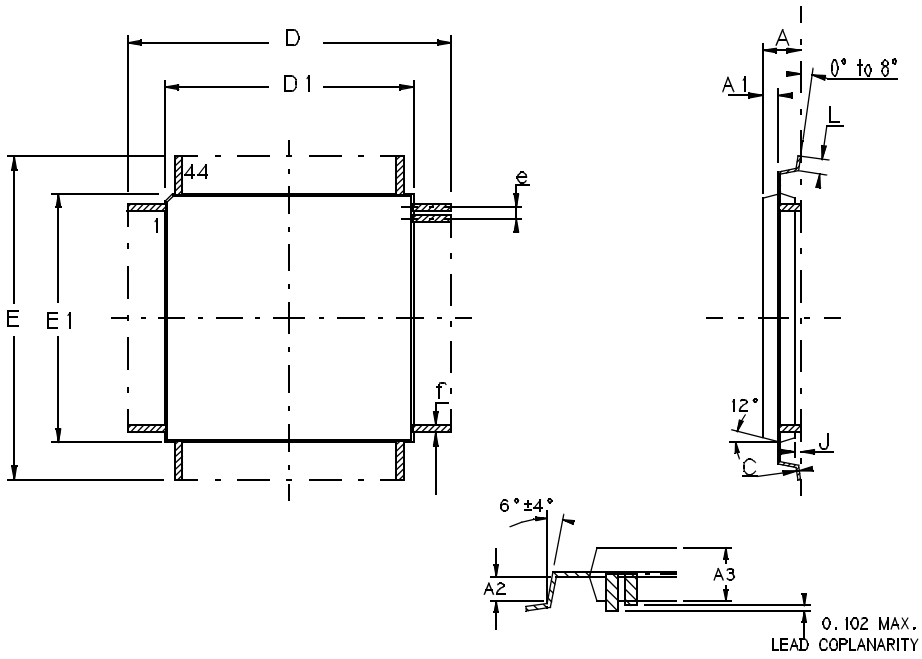


Table 61. VQFP Package Size

	MM		Inch	
	Min	**Max**	**Min**	**Max**
A	-	1.60	-	.063
A1	0.64 REF		.025 REF	
A2	0.64 REF		.025REF	
A3	1.35	1.45	.053	.057
D	11.90	12.10	.468	.476
D1	9.90	10.10	.390	.398
E	11.90	12.10	.468	.476
E1	9.90	10.10	.390	.398
J	0.05	-	.002	6
L	0.45	0.75	.018	.030
e	0.80 BSC		.0315 BSC	
f	0.35 BSC		.014 BSC	

Options (Please consult Atmel sales)

- ROM code encryption
- Tape & Reel or Dry Pack
- Known good dice
- Extended temperature range: -55°C to +125°C

Product Markings

ROMless versions

ATMEL
Part number

YYWW . Lot Number

Mask ROM versions

ATMEL
Customer Part number

Part Number
YYWW . Lot Number

OTP versions

ATMEL
Part number

YYWW . Lot Number