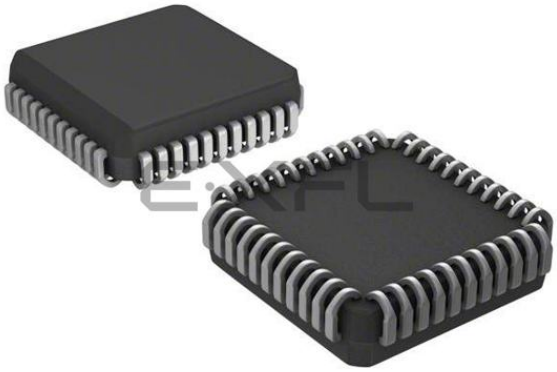


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C251
Core Size	8/16-Bit
Speed	24MHz
Connectivity	EBI/EMI, I²C, Microwire, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.6x16.6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/tsc80251g2d-24cb

Signals

Table 2. Product Name Signal Description

Signal Name	Type	Description	Alternate Function
A17	O	**18th Address Bit** Output to memory as 18th external address bit (A17) in extended bus applications, depending on the values of bits RD0 and RD1 in UCONFIG0 byte (see Table 13, Page 20).	P1.7
A16	O	**17th Address Bit** Output to memory as 17th external address bit (A16) in extended bus applications, depending on the values of bits RD0 and RD1 in UCONFIG0 byte (see Table 13, Page 20).	P3.7
A15:8(1)	O	**Address Lines** Upper address lines for the external bus.	P2.7:0
AD7:0(1)	I/O	**Address/Data Lines** Multiplexed lower address lines and data for the external memory.	P0.7:0
ALE	O	**Address Latch Enable** ALE signals the start of an external bus cycle and indicates that valid address information are available on lines A16/A17 and A7:0. An external latch can use ALE to demultiplex the address from address/data bus.	–
AWAIT#	I	**Real-time Asynchronous Wait States Input** When this pin is active (low level), the memory cycle is stretched until it becomes high. When using the Product Name as a pin-for-pin replacement for a 8xC51 product, AWAIT# can be unconnected without loss of compatibility or power consumption increase (on-chip pull-up). Not available on DIP package.	–
CEX4:0	I/O	**PCA Input/Output pins** CEXx are input signals for the PCA capture mode and output signals for the PCA compare and PWM modes.	P1.7:3
EA#	I	**External Access Enable** EA# directs program memory accesses to on-chip or off-chip code memory. For EA# = 0, all program memory accesses are off-chip. For EA# = 1, an access is on-chip ROM if the address is within the range of the on-chip ROM; otherwise the access is off-chip. The value of EA# is latched at reset. For devices without ROM on-chip, EA# must be strapped to ground.	–
ECI	O	**PCA External Clock input** ECI is the external clock input to the 16-bit PCA timer.	P1.2
MISO	I/O	**SPI Master Input Slave Output line** When SPI is in master mode, MISO receives data from the slave peripheral. When SPI is in slave mode, MISO outputs data to the master controller.	P1.5
MOSI	I/O	**SPI Master Output Slave Input line** When SPI is in master mode, MOSI outputs data to the slave peripheral. When SPI is in slave mode, MOSI receives data from the master controller.	P1.7
INT1:0#	I	**External Interrupts 0 and 1** INT1#/INT0# inputs set IE1:0 in the TCON register. If bits IT1:0 in the TCON register are set, bits IE1:0 are set by a falling edge on INT1#/INT0#. If bits IT1:0 are cleared, bits IE1:0 are set by a low level on INT1#/INT0#.	P3.3:2

Configuration Bytes

The TSC80251G2D derivatives provide user design flexibility by configuring certain operating features at device reset. These features fall into the following categories:

- external memory interface (Page mode, address bits, programmed wait states and the address range for RD#, WR#, and PSEN#)
- source mode/binary mode opcodes
- selection of bytes stored on the stack by an interrupt
- mapping of the upper portion of on-chip code memory to region 00:

Two user configuration bytes UCONFIG0 (see Table 11) and UCONFIG1 (see Table 12) provide the information.

When EA# is tied to a low level, the configuration bytes are fetched from the external address space. The TSC80251G2D derivatives reserve the top eight bytes of the memory address space (FF:FFF8h-FF:FFFFh) for an external 8-byte configuration array. Only two bytes are actually used: UCONFIG0 at FF:FFF8h and UCONFIG1 at FF:FFF9h.

For the mask ROM devices, configuration information is stored in on-chip memory (see ROM Verifying). When EA# is tied to a high level, the configuration information is retrieved from the on-chip memory instead of the external address space and there is no restriction in the usage of the external memory.

Configuration Byte 1

Table 13. Address Ranges and Usage of RD#, WR# and PSEN# Signals

RD1	RD0	P1.7	P3.7/RD#	PSEN#	WR#	External Memory
0	0	A17	A16	Read signal for all external memory locations	Write signal for all external memory locations	256 KB
0	1	I/O pin	A16	Read signal for all external memory locations	Write signal for all external memory locations	128 KB
1	0	I/O pin	I/O pin	Read signal for all external memory locations	Write signal for all external memory locations	64 KB
1	1	I/O pin	Read signal for regions 00: and 01:	Read signal for regions FE: and FF:	Write signal for all external memory locations	2×64 KB(1)

Notes: 1. This selection provides compatibility with the standard 80C51 hardware which has separate external memory spaces for data and code.

Table 22. Summary of Compare Instructions

CompareCMP <dest>, <src>dest opnd - src opnd						
			Binary Mode		Source Mode	
Mnemonic	**<dest>, <src>(2)**	**Comments**	**Bytes**	**States**	**Bytes**	**States**
CMP	Rmd, Rms	Register with register	3	2	2	1
	WRjd, WRjs	Word register with word register	3	3	2	2
	DRkd, DRks	Dword register with dword register	3	5	2	4
	Rm, #data	Register with immediate data	4	3	3	2
	WRj, #data16	Word register with immediate 16-bit data	5	4	4	3
	DRk, #0data16	Dword register with zero-extended 16-bit immediate data	5	6	4	5
	DRk, #1data16	Dword register with one-extended 16-bit immediate data	5	6	4	5
	Rm, dir8	Direct address (on-chip RAM or SFR) with byte register	4	3(1)	3	2(1)
	WRj, dir8	Direct address (on-chip RAM or SFR) with word register	4	4	3	3
	Rm, dir16	Direct address (64K) with byte register	5	3(2)	4	2(2)
	WRj, dir16	Direct address (64K) with word register	5	4(3)	4	3(3)
	Rm, at WRj	Indirect address (64K) with byte register	4	3(2)	3	2(2)
	Rm, at DRk	Indirect address (16M) with byte register	4	4(2)	3	3(2)

Notes:
1. If this instruction addresses an I/O Port (Px, x = 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.
2. If this instruction addresses external memory location, add N+2 to the number of states (N: number of wait states).
3. If this instruction addresses external memory location, add 2(N+2) to the number of states (N: number of wait states).

Table 24. Summary of Multiply, Divide and Decimal-adjust Instructions

MultiplyMUL AB(B:A) ← (A)×(B)
MUL <dest>, <src>extended dest opnd ← dest opnd × src opnd

DivideDIV AB(A) ← Quotient ((A)/(B))
(B) ← Remainder ((A)/(B))

DivideDIV <dest>, <src>ext. dest opnd high ← Quotient (dest opnd/src opnd)
ext. dest opnd low ← Remainder (dest opnd/src opnd)

Decimal-adjust ACCDA AIF [[$(A)_{3:0}$ > 9] ∨ [(AC) = 1]]
for Addition (BCD) THEN $(A)_{3:0} \leftarrow (A)_{3:0}$ + 6 !affects CY;
IF [[$(A)_{7:4}$ > 9] ∨ [(CY) = 1]]
THEN $(A)_{7:4} \leftarrow (A)_{7:4}$ + 6

Mnemonic	<dest>, <src>(1)	Comments	Binary Mode		Source Mode	
			Bytes	States	Bytes	States
MUL	AB	Multiply A and B	1	5	1	5
	Rmd, Rms	Multiply byte register and byte register	3	6	2	5
	WRjd, WRjs	Multiply word register and word register	3	12	2	11
DIV	AB	Divide A and B	1	10	1	10
	Rmd, Rms	Divide byte register and byte register	3	11	2	10
	WRjd, WRjs	Divide word register and word register	3	21	2	20
DA	A	Decimal adjust ACC	1	1	1	1

Note: 1. A shaded cell denotes an instruction in the C51 Architecture.

Table 25. Summary of Move Instructions (1/3)

Move to High wordMOVH <dest>, <src>dest $opnd_{31:16}$ ← src opnd Move with Sign extensionMOVS <dest>, <src>dest opnd ← src opnd with sign extend Move with Zero extensionMOVZ <dest>, <src>dest opnd ← src opnd with zero extend Move CodeMOVC A, <src>(A) ← src opnd Move eXtendedMOVX <dest>, <src>dest opnd ← src opnd						
Mnemonic	**<dest>, <src>(2)**	**Comments**	**Binary Mode**		**Source Mode**	
			Bytes	**States**	**Bytes**	**States**
MOVH	DRk, #data16	16-bit immediate data into upper word of dword register	5	3	4	2
MOVS	WRj, Rm	Byte register to word register with sign extension	3	2	2	1
MOVZ	WRj, Rm	Byte register to word register with zeros extension	3	2	2	1
MOVC	A, at A +DPTR	Code byte relative to DPTR to ACC	1	6(3)	1	6(3)
	A, at A +PC	Code byte relative to PC to ACC	1	6(3)	1	6(3)
MOVX	A, at Ri	Extended memory (8-bit address) to ACC(2)	1	4	1	5
	A, at DPTR	Extended memory (16-bit address) to ACC(2)	1	3(4)	1	3(4)
	at Ri, A	ACC to extended memory (8-bit address)(2)	1	4	1	4
	at DPTR, A	ACC to extended memory (16-bit address)(2)	1	4(3)	1	4(3)

Notes:
1. A shaded cell denotes an instruction in the C51 Architecture.
2. Extended memory addressed is in the region specified by DPXL (reset value = 01h).
3. If this instruction addresses external memory location, add N+1 to the number of states (N: number of wait states).
4. If this instruction addresses external memory location, add N+2 to the number of states (N: number of wait states).

Programming and Verifying Non-volatile Memory

Internal Features

The internal non-volatile memory of the TSC80251G2D derivatives contains five different areas:

- Code Memory
- Configuration Bytes
- Lock Bits
- Encryption Array
- Signature Bytes

EPROM/OTPROM Devices

All the internal non-volatile memory but the Signature Bytes of the TSC87251G2D products is made of EPROM cells. The Signature Bytes of the TSC87251G2D products are made of Mask ROM.

The TSC87251G2D products are programmed and verified in the same manner as Atmel's TSC87251G1A, using a SINGLE-PULSE algorithm, which programs at V_{PP} = 12.75V using only one 100µs pulse per byte. This results in a programming time of less than 10 seconds for the 32 kilobytes on-chip code memory.

The EPROM of the TSC87251G2D products in Window package is erasable by Ultra-Violet radiation(1) (UV). UV erasure set all the EPROM memory cells to one and allows reprogramming. The quartz window must be covered with an opaque label(2) when the device is in operation. This is not so much to protect the EPROM array from inadvertent erasure, as to protect the RAM and other on-chip logic. Allowing light to impinge on the silicon die during device operation may cause a logical malfunction.

The TSC87251G2D products in plastic packages are One Time Programmable (OTP). An EPROM cell cannot be reset by UV once programmed to zero.

Notes:
1. The recommended erasure procedure is exposure to ultra-violet light (at 2537 Å) to an integrated dose of at least 20 W-sec/cm^2. Exposing the EPROM to an ultra-violet lamp of 12000 µW/cm^2 rating for 30 minutes should be sufficient.
2. Erasure of the EPROM begins to occur when the chip is exposed to light wavelength shorter than 4000 Å. Since sunlight and fluorescent light have wavelength in this range, exposure to these light sources over an extended time (1 week in sunlight or 3 years in room-level fluorescent lighting) could cause inadvertent erasure.

Mask ROM Devices

All the internal non-volatile memory of TSC83251G2D products is made of Mask ROM cells. They can only be verified by the user, using the same algorithm as the EPROM/OTPROM devices.

ROMless Devices

The TSC80251G2D products do not include on-chip Configuration Bytes, Code Memory and Encryption Array. They only include Signature Bytes made of Mask ROM cells which can be read using the same algorithm as the EPROM/OTPROM devices.

Security Features

In some microcontroller applications, it is desirable that the user's program code be secured from unauthorized access. The TSC83251G2D and TSC87251G2D offer two kinds of protection for program code stored in the on-chip array:

- Program code in the on-chip Code Memory is encrypted when read out for verification if the Encryption Array isprogrammed.
- A three-level lock bit system restricts external access to the on-chip code memory.

AC Characteristics - Commercial & Industrial

AC Characteristics - External Bus Cycles

Definition of Symbols

Table 38. External Bus Cycles Timing Symbol Definitions

Signals	
A	Address
D	Data In
L	ALE
Q	Data Out
R	RD#/PSEN#
W	WR#

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid
Z	Floating

Timings

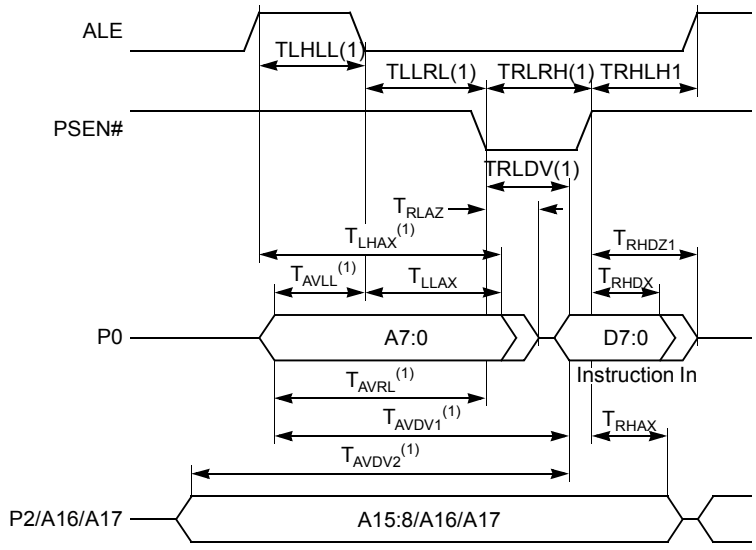
Test conditions: capacitive load on all pins = 50 pF.

Table 39 and Table 40 list the AC timing parameters for the TSC80251G2D derivatives with no wait states. External wait states can be added by extending PSEN#/RD#/WR# and or by extending ALE. In these tables, Note 2 marks parameters affected by one ALE wait state, and Note 3 marks parameters affected by PSEN#/RD#/WR# wait states.

Figure 8 to Figure 13 show the bus cycles with the timing parameters.

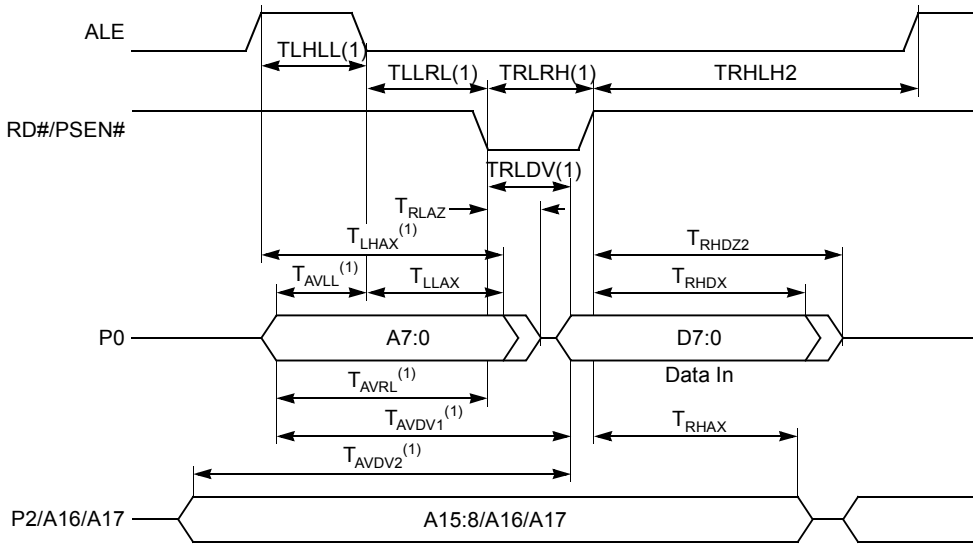
Waveforms in Non-Page Mode

Figure 8. External Bus Cycle: Code Fetch (Non-Page Mode)



Note: 1. The value of this parameter depends on wait states. See Table 39 and Table 40.

Figure 9. External Bus Cycle: Data Read (Non-Page Mode)



Note: 1. The value of this parameter depends on wait states. See Table 39 and Table 40.

Timings

Table 42. Real-Time Synchronous Wait AC Timings; V_{DD} = 2.7 to 5.5 V, T_A = -40 to 85°C

Symbol	Parameter	Min	Max	Unit
T_{CLYV}	Wait Clock Low to Wait Set-up	0	T_{OSC} - 20	ns
T_{CLYX}	Wait Hold after Wait Clock Low	2W·T_{OSC} + 5	(1+2W)·T_{OSC} - 20	ns
T_{RLYV}	PSEN#/RD# Low to Wait Set-up	0	T_{OSC} - 20	ns
T_{RLYX}	Wait Hold after PSEN#/RD# Low	2W·T_{OSC} + 5	(1+2W)·T_{OSC} - 20	ns
T_{WLYV}	WR# Low to Wait Set-up	0	T_{OSC} - 20	ns
T_{WLYX}	Wait Hold after WR# Low	2W·T_{OSC} + 5	(1+2W)·T_{OSC} - 20	ns

Waveforms

Figure 14. Real-time Synchronous Wait State: Code Fetch/Data Read

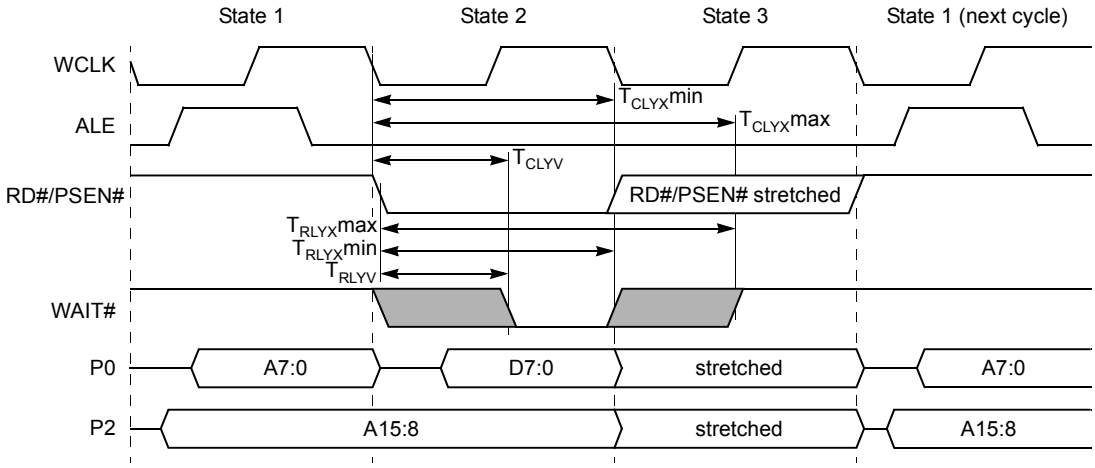
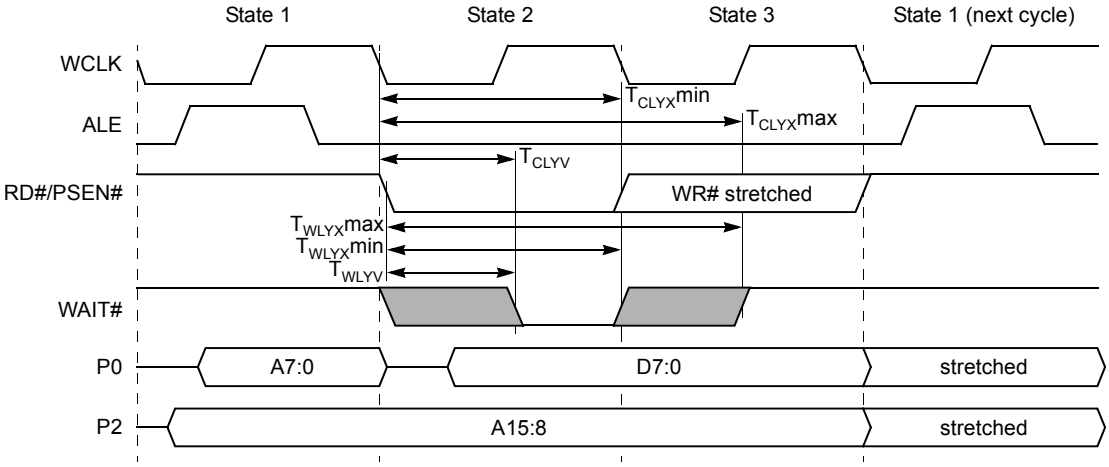


Figure 15. Real-time Synchronous Wait State: Data Write



AC Characteristics - Real-Time Asynchronous Wait State

Definition of Symbols

Table 43. Real-Time Asynchronous Wait Timing Symbol Definitions

Signals	
S	PSEN#/RD#/WR#
Y	AWAIT#

Conditions	
L	Low
V	Valid
X	No Longer Valid

Timings

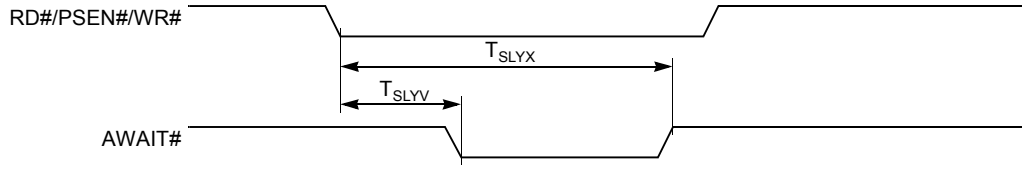
Table 44. Real-Time Asynchronous Wait AC Timings; V_{DD} = 2.7 to 5.5 V, T_A = -40 to 85°C

Symbol	Parameter	Min	Max	Unit
T_{SLYV}	PSEN#/RD#/WR# Low to Wait Set-up		T_{OSC} - 10	ns
T_{SLYX}	Wait Hold after PSEN#/RD#/WR# Low	$(2N-1)\cdot T_{OSC}$ + 10		ns(1)

Note: 1. N is the number of wait states added (N≥ 1).

Waveforms

Figure 16. Real-time Asynchronous Wait State Timings



AC Characteristics - Serial Port in Shift Register Mode

Definition of Symbols

Table 45. Serial Port Timing Symbol Definitions

Signals	
D	Data In
Q	Data Out
X	Clock

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid

Timings

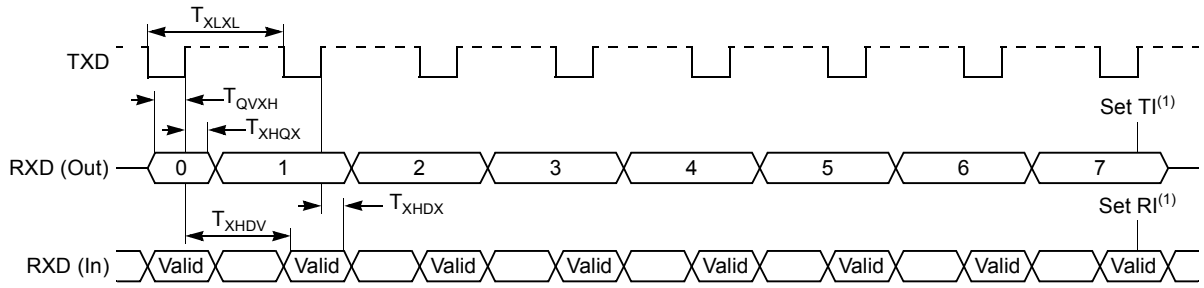
Table 46. Serial Port AC Timing -Shift Register Mode; V_{DD} = 2.7 to 5.5 V, T_A = -40 to 85°C

		12 MHz		16 MHz		24 MHz(1)		
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Unit
T_{XLXL}	Serial Port Clock Cycle Time	998		749		500		ns
T_{QVXH}	Output Data Setup to Clock Rising Edge	833		625		417		ns
T_{XHQX}	Output Data hold after Clock Rising Edge	165		124		82		ns
T_{XHDX}	Input Data Hold after Clock Rising Edge	0		0		0		ns
T_{XHDV}	Clock Rising Edge to Input Data Valid		974		732		482	ns

Note: 1. For high speed versions only.

Waveforms

Figure 17. Serial Port Waveforms - Shift Register Mode



Note: 1. TI and RI are set during S1P1 of the peripheral cycle following the shift of the eight bit.

Timings

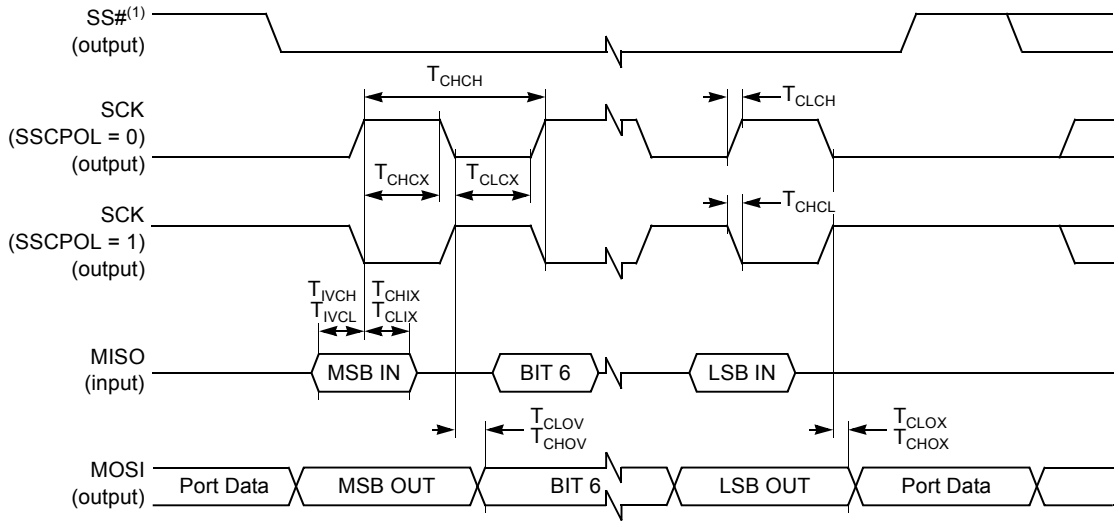
Table 49. SPI Interface AC Timing; V_{DD} = 2.7 to 5.5 V, T_A = -40 to 85°C

Symbol	Parameter	Min	Max	Unit
Slave Mode(1)				
T_{CHCH}	Clock Period	8		T_{OSC}
T_{CHCX}	Clock High Time	3.2		T_{OSC}
T_{CLCX}	Clock Low Time	3.2		T_{OSC}
T_{SLCH}, T_{SLCL}	SS# Low to Clock edge	200		ns
T_{IVCL}, T_{IVCH}	Input Data Valid to Clock Edge	100		ns
T_{CLIX}, T_{CHIX}	Input Data Hold after Clock Edge	100		ns
$T_{CLOV,}$ T_{CHOV}	Output Data Valid after Clock Edge		100	ns
T_{CLOX}, T_{CHOX}	Output Data Hold Time after Clock Edge	0		ns
T_{CLSH}, T_{CHSH}	SS# High after Clock Edge	0		ns
T_{IVCL}, T_{IVCH}	Input Data Valid to Clock Edge	100		ns
T_{CLIX}, T_{CHIX}	Input Data Hold after Clock Edge	100		ns
T_{SLOV}	SS# Low to Output Data Valid		130	ns
T_{SHOX}	Output Data Hold after SS# High		130	ns
T_{SHSL}	SS# High to SS# Low	(2)		
T_{ILIH}	Input Rise Time		2	µs
T_{IHIL}	Input Fall Time		2	µs
T_{OLOH}	Output Rise time		100	ns
T_{OHOL}	Output Fall Time		100	ns
Master Mode(3)				
T_{CHCH}	Clock Period	4		T_{OSC}
T_{CHCX}	Clock High Time	1.6		T_{OSC}
T_{CLCX}	Clock Low Time	1.6		T_{OSC}
T_{IVCL}, T_{IVCH}	Input Data Valid to Clock Edge	50		ns
T_{CLIX}, T_{CHIX}	Input Data Hold after Clock Edge	50		ns
$T_{CLOV,}$ T_{CHOV}	Output Data Valid after Clock Edge		65	ns
T_{CLOX}, T_{CHOX}	Output Data Hold Time after Clock Edge	0		ns
T_{ILIH}	Input Data Rise Time		2	µs
T_{IHIL}	Input Data Fall Time		2	µs
T_{OLOH}	Output Data Rise time		50	ns
T_{OHOL}	Output Data Fall Time		50	ns

Notes: 1. Capacitive load on all pins = 200 pF in slave mode.
2. The value of this parameter depends on software.
3. Capacitive load on all pins = 100 pF in master mode.

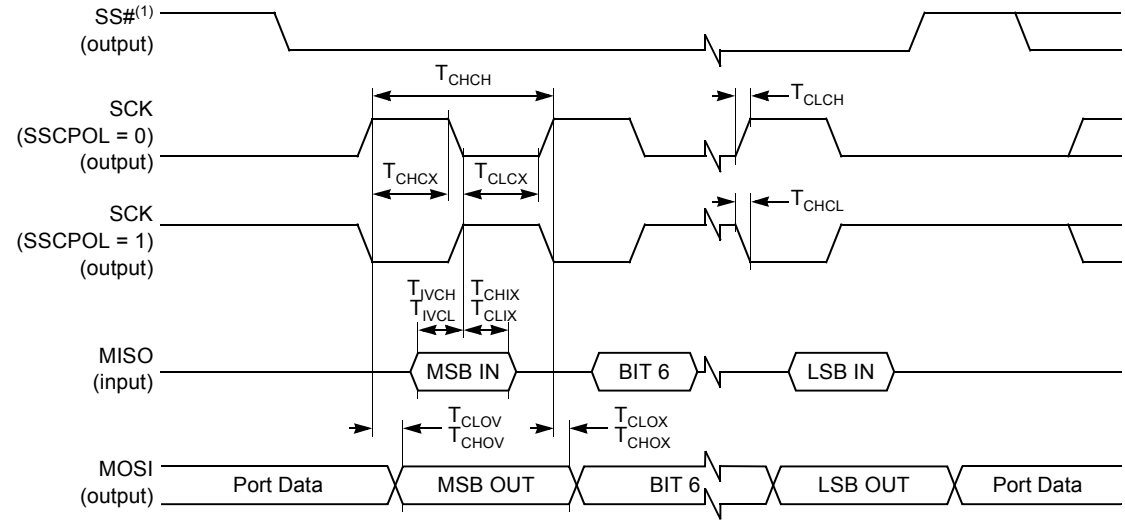
Waveforms

Figure 19. SPI Master Waveforms (SSCPHA = 0)



Note: 1. SS# handled by software.

Figure 20. SPI Master Waveforms (SSCPHA = 1)



Note: 1. Not Defined but normally MSB of character just received.

Timings

Table 51. EPROM Programming AC timings; V_{DD} = 4.5 to 5.5 V, T_A = 0 to 40°C

Symbol	Parameter	Min	Max	Unit
T_{OSC}	XTAL1 Period	83.5	250	ns
T_{AVGL}	Address Setup to PROG# low	48		T_{OSC}
T_{GHAX}	Address Hold after PROG# low	48		T_{OSC}
T_{DVGL}	Data Setup to PROG# low	48		T_{OSC}
T_{GHDX}	Data Hold after PROG#	48		T_{OSC}
T_{ELSH}	ENABLE High to V_{PP}	48		T_{OSC}
T_{SHGL}	V_{PP} Setup to PROG# low	10		µs
T_{GHSL}	V_{PP} Hold after PROG#	10		µs
T_{SLEH}	ENABLE Hold after V_{PP}	0		ns
T_{GLGH}	PROG# Width	90	110	µs

Table 52. EPROM Verifying AC timings; V_{DD} = 4.5 to 5.5 V, V_{DD} = 2.7 to 5.5 V, T_A = 0 to 40°C

Symbol	Parameter	Min	Max	Unit
T_{OSC}	XTAL1 Period	83.5	250	ns
T_{AVQV}	Address to Data Valid		48	T_{OSC}
T_{AXQX}	Address to Data Invalid	0		ns
T_{ELQV}	ENABLE low to Data Valid	0	48	T_{OSC}
T_{EHQZ}	Data Float after ENABLE	0	48	T_{OSC}

Waveforms

Figure 23. EPROM Programming Waveforms

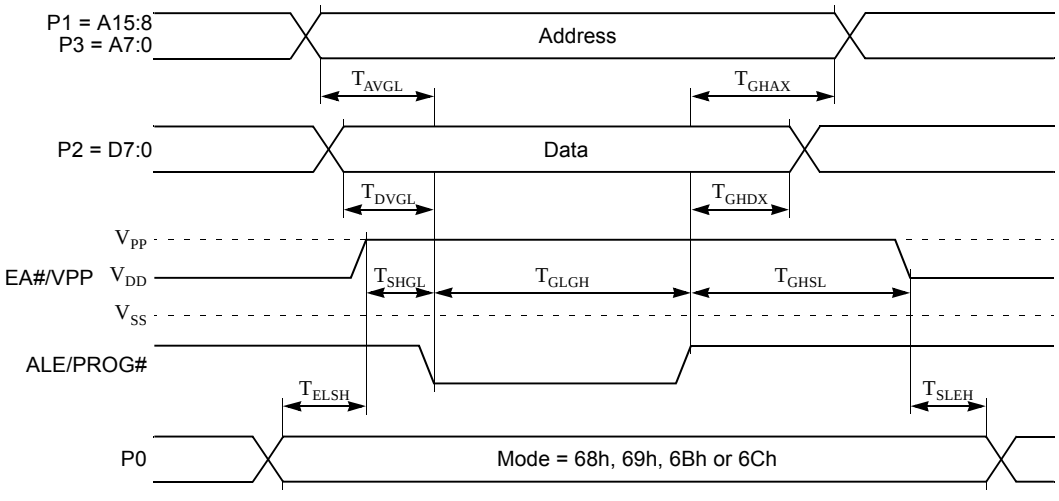
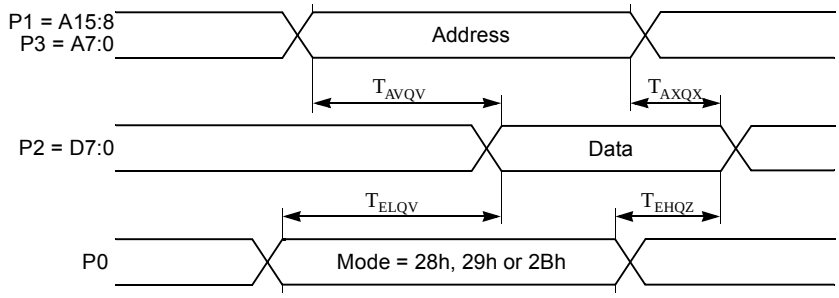


Figure 24. EPROM Verifying Waveforms



AC Characteristics - External Clock Drive and Logic Level References

Definition of Symbols

Table 53. External Clock Timing Symbol Definitions

Signals	
C	Clock

Conditions	
H	High
L	Low
X	No Longer Valid

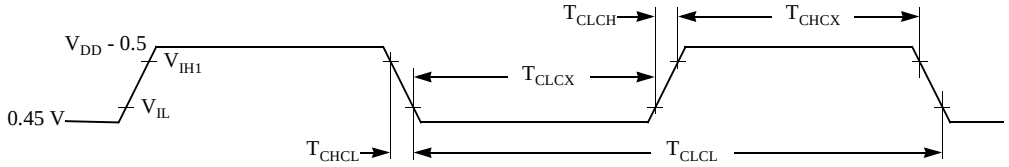
Timings

Table 54. External Clock AC Timings; V_{DD} = 4.5 to 5.5 V, T_A = -40 to +85°C

Symbol	Parameter	Min	Max	Unit
F_{OSC}	Oscillator Frequency		24	MHz
T_{CHCX}	High Time	10		ns
T_{CLCX}	Low Time	10		ns
T_{CLCH}	Rise Time	3		ns
T_{CHCL}	Fall Time	3		ns

Waveforms

Figure 25. External Clock Waveform



Notes: 1. During AC testing, all inputs are driven at V_{DD} -0.5 V for a logic 1 and 0.45 V for a logic 0.
2. Timing measurements are made on all outputs at V_{IH} min for a logic 1 and V_{IL} max for a logic 0.

Absolute Maximum Rating and Operating Conditions

Absolute Maximum Ratings

Storage Temperature ..... -65 to +150°C Voltage on any other Pin to VSS ..... -0.5 to +6.5 V I_{OL} per I/O Pin ..... 15 mA Power Dissipation ..... 1.5 W Ambient Temperature Under Bias Commercial.....0 to +70°C Industrial ..... -40 to +85°C Automotive..... -40 to +85°C V_{DD} High Speed versions..... 4.5 to 5.5 V Low Voltage versions..... 2.7 to 5.5 V	*NOTICE: Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only. Operation beyond the “operating conditions” is not recommended and extended exposure beyond the “Operating Conditions” may affect device reliability.

Figure 31. I_{DL} Test Condition, Idle Mode

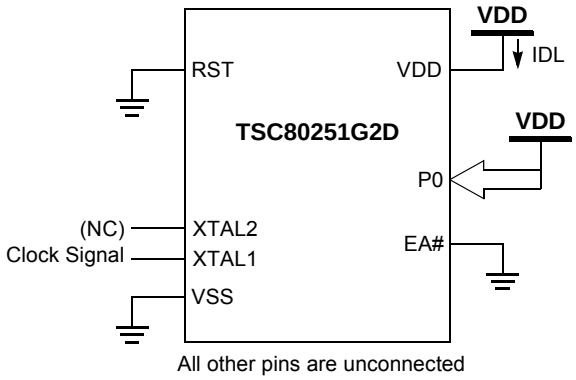
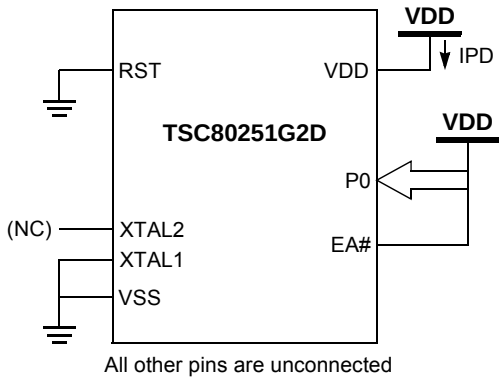


Figure 32. I_{PD} Test Condition, Power-Down Mode



CDIL 40 with Window - Mechanical Outline

Figure 34. Ceramic Dual In Line

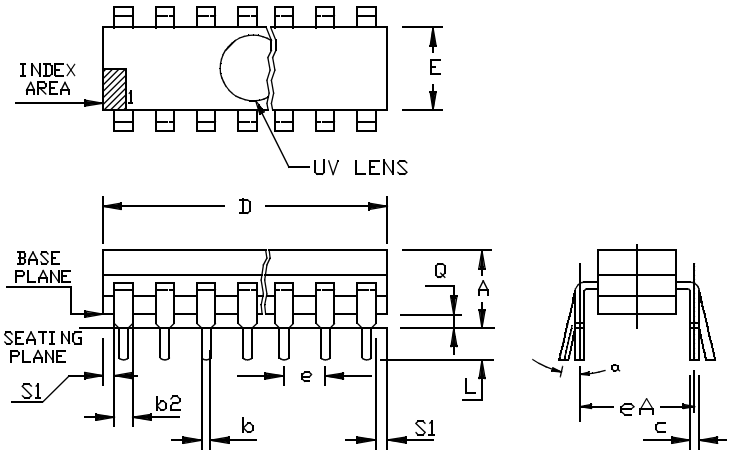


Table 58. CDIL Package Size

	MM		Inch	
	Min	**Max**	**Min**	**Max**
A	-	5.71	-	.225
b	0.36	0.58	.014	.023
b2	1.14	1.65	.045	.065
c	0.20	0.38	.008	.015
D	-	53.47	-	2.105
E	13.06	15.37	.514	.605
e	2.54 B.S.C.		.100 B.S.C.	
eA	15.24 B.S.C.		.600 B.S.C.	
L	3.18	5.08	.125	.200
Q	0.38	1.40	.015	.055
S1	0.13	-	.005	-
a	0 - 15		0 - 15	
N	40			

Options (Please consult Atmel sales)

- ROM code encryption
- Tape & Reel or Dry Pack
- Known good dice
- Extended temperature range: -55°C to +125°C

Product Markings

ROMless versions

ATMEL
Part number

YYWW . Lot Number

Mask ROM versions

ATMEL
Customer Part number

Part Number
YYWW . Lot Number

OTP versions

ATMEL
Part number

YYWW . Lot Number