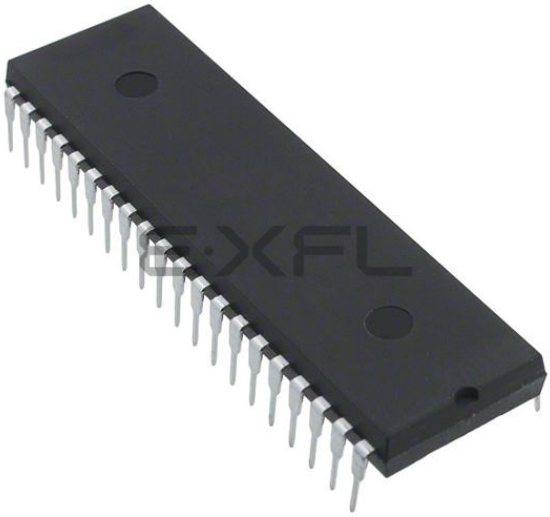

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C251
Core Size	8/16-Bit
Speed	24MHz
Connectivity	EBI/EMI, I²C, Microwire, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIL
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/tsc80251g2d-24ia

- **Typical Operating Current:11 mA at 3V**
- **Typical Power-down Current: 1 µA**
- **Temperature Ranges: Commercial (0°C to +70°C), Industrial (-40°C to +85°C), Automotive ((-40°C to +85°C) ROM only)**
- **Option: Extended Range (-55°C to +125°C)**
- **Packages: PDIL 40, PLCC 44 and VQFP 44**
- **Options: Known Good Dice and Ceramic Packages**

Description

The TSC80251G2D products are derivatives of the Atmel Microcontroller family based on the 8/16-bit C251 Architecture. This family of products is tailored to 8/16-bit microcontroller applications requiring an increased instruction throughput, a reduced operating frequency or a larger addressable memory space. The architecture can provide a significant code size reduction when compiling C programs while fully preserving the legacy of C51 assembly routines.

The TSC80251G2D derivatives are pin and software compatible with standard 80C51/Fx/Rx/Rx+ with extended on-chip data memory (1 Kbyte RAM) and up to 256 kilobytes of external code and data. Additionally, the TSC83251G2D and TSC87251G2D provide on-chip code memory: 32 kilobytes ROM and 32 kilobytes EPROM/OTPROM respectively.

They provide transparent enhancements to Intel's 8xC251Sx family with an additional Synchronous Serial Link Controller (SSLC supporting TWI, µWire and SPI protocols), a Keyboard interrupt interface, a dedicated Baud Rate Generator for UART, and Power Management features.

TSC80251G2D derivatives are optimized for speed and for low power consumption on a wide voltage range.

Note: 1. This Datasheet provides the technical description of the TSC80251G2D derivatives. For further information on the device usage, please request the TSC80251 Programmer's Guide and the TSC80251G1D Design Guide and errata sheet.

Typical Applications

- ISDN Terminals
- High-Speed Modems
- PABX (SOHO)
- Line Cards
- DVD ROM and Players
- Printers
- Plotters
- Scanners
- Banking Machines
- Barcode Readers
- Smart Cards Readers
- High-End Digital Monitors
- High-End Joysticks
- High-end TV's

Figure 3. TSC80251G2D 44-pin VQFP Package

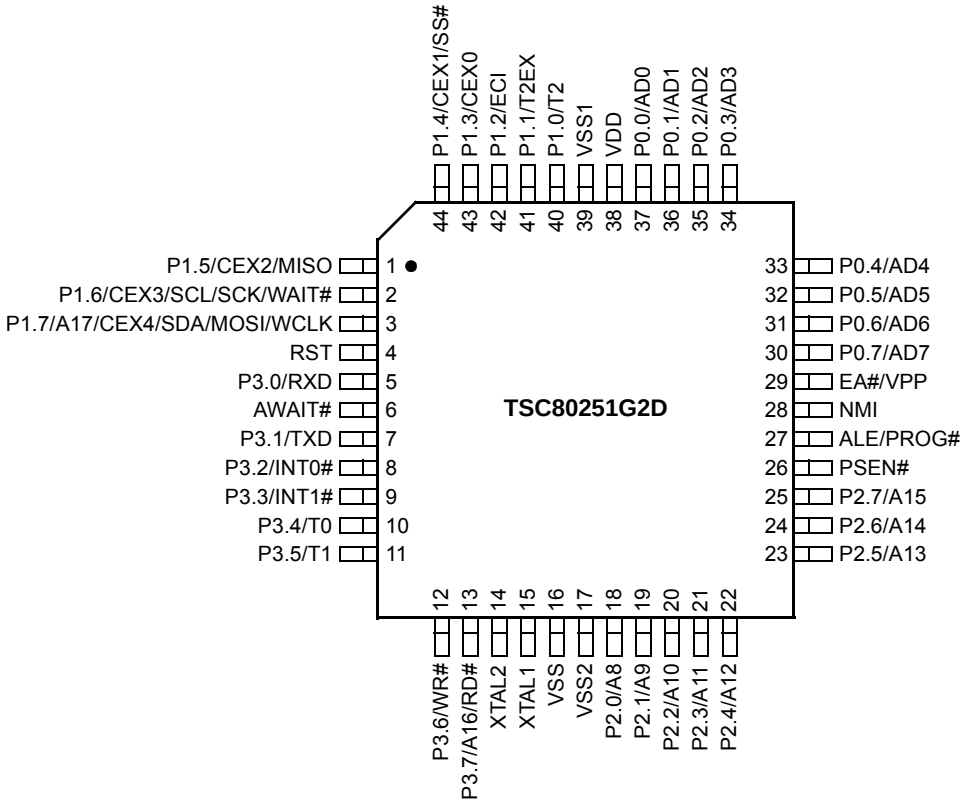


Table 2. Product Name Signal Description (Continued)

Signal Name	Type	Description	Alternate Function
NMI	I	**Non Maskable Interrupt** Holding this pin high for 24 oscillator periods triggers an interrupt. When using the Product Name as a pin-for-pin replacement for a 8xC51 product, NMI can be unconnected without loss of compatibility or power consumption increase (on-chip pull-down). Not available on DIP package.	–
P0.0:7	I/O	**Port 0** P0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. To avoid any paraitic current consumption, Floating P0 inputs must be polarized to V_{DD} or V_{SS}.	AD7:0
P1.0:7	I/O	**Port 1** P1 is an 8-bit bidirectional I/O port with internal pull-ups. P1 provides interrupt capability for a keyboard interface.	–
P2.0:7	I/O	**Port 2** P2 is an 8-bit bidirectional I/O port with internal pull-ups.	A15:8
P3.0:7	I/O	**Port 3** P3 is an 8-bit bidirectional I/O port with internal pull-ups.	–
PROG#	I	**Programming Pulse input** The programming pulse is applied to this input for programming the on-chip EPROM/OTPROM.	–
PSEN#	O	**Program Store Enable/Read signal output** PSEN# is asserted for a memory address range that depends on bits RD0 and RD1 in UCONFIG0 byte (see).	–
RD#	O	**Read or 17th Address Bit (A16)** Read signal output to external data memory depending on the values of bits RD0 and RD1 in UCONFIG0 byte (see Table 13, Page 20).	P3.7
RST	I	**Reset input to the chip** Holding this pin high for 64 oscillator periods while the oscillator is running resets the device. The Port pins are driven to their reset conditions when a voltage greater than V_{IH1} is applied, whether or not the oscillator is running. This pin has an internal pull-down resistor which allows the device to be reset by connecting a capacitor between this pin and VDD. Asserting RST when the chip is in Idle mode or Power-Down mode returns the chip to normal operation.	–
RXD	I/O	**Receive Serial Data** RXD sends and receives data in serial I/O mode 0 and receives data in serial I/O modes 1, 2 and 3.	P3.0
SCL	I/O	**TWI Serial Clock** When TWI controller is in master mode, SCL outputs the serial clock to slave peripherals. When TWI controller is in slave mode, SCL receives clock from the master controller.	P1.6
SCK	I/O	**SPI Serial Clock** When SPI is in master mode, SCK outputs clock to the slave peripheral. When SPI is in slave mode, SCK receives clock from the master controller.	P1.6
SDA	I/O	**TWI Serial Data** SDA is the bidirectional TWI data line.	P1.7
SS#	I	**SPI Slave Select Input** When in Slave mode, SS# enables the slave mode.	P1.4

Table 11. Configuration Byte 0
UCONFIG0

7	6	5	4	3	2	1	0
-	WSA1#	WSA0#	XALE#	RD1	RD0	PAGE#	SRC

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** Set this bit when writing to UCONFIG0.
6	WSA1#	**Wait State A bits** Select the number of wait states for RD#, WR# and PSEN# signals for external memory accesses (all regions except 01:). WSA1# WSA0# Number of Wait States 0 0 3 0 1 2 1 0 1 1 1 0
5	WSA0#	
4	XALE#	**Extend ALE bit** Clear to extend the duration of the ALE pulse from T_{OSC} to $3 \cdot T_{OSC}$. Set to minimize the duration of the ALE pulse to $1 \cdot T_{OSC}$.
3	RD1	**Memory Signal Select bits** Specify a 18-bit, 17-bit or 16-bit external address bus and the usage of RD#, WR# and PSEN# signals (see Table 13).
2	RD0	
1	PAGE#	**Page Mode Select bit**(1) Clear to select the faster Page mode with A15:8/D7:0 on Port 2 and A7:0 on Port 0. Set to select the non-Page mode(2) with A15:8 on Port 2 and A7:0/D7:0 on Port 0.
0	SRC	**Source Mode/Binary Mode Select bit** Clear to select the binary mode. Set to select the source mode.

Notes: 1. UCONFIG0 is fetched twice so it can be properly read both in Page or Non-Page modes. If P2.1 is cleared during the first data fetch, a Page mode configuration is used, otherwise the subsequent fetches are performed in Non-Page mode.
2. This selection provides compatibility with the standard 80C51 hardware which is multiplexing the address LSB and the data on Port 0.

Instruction Set Summary

This section contains tables that summarize the instruction set. For each instruction there is a short description, its length in bytes, and its execution time in states (one state time is equal to two system clock cycles). There are two concurrent processes limiting the effective instruction throughput:

- Instruction Fetch
- Instruction Execution

Table 20 to Table 32 assume code executing from on-chip memory, then the CPU is fetching 16-bit at a time and this is never limiting the execution speed.

If the code is fetched from external memory, a pre-fetch queue will store instructions ahead of execution to optimize the memory bandwidth usage when slower instructions are executed. However, the effective speed may be limited depending on the average size of instructions (for the considered section of the program flow). The maximum average instruction throughput is provided by Table 14 depending on the external memory configuration (from Page Mode to Non-Page Mode and the maximum number of wait states). If the average size of instructions is not an integer, the maximum effective throughput is found by pondering the number of states for the neighbor integer values.

Table 14. Minimum Number of States per Instruction for given Average Sizes

Average size of Instructions (bytes)	Page Mode (states)	Non-page Mode (states)				
		0 Wait State	1 Wait State	2 Wait States	3 Wait States	4 Wait States
1	1	2	3	4	5	6
2	2	4	6	8	10	12
3	3	6	9	12	15	18
4	4	8	12	16	20	24
5	5	10	15	20	25	30

If the average execution time of the considered instructions is larger than the number of states given by Table 14, this larger value will prevail as the limiting factor. Otherwise, the value from Table 14 must be taken. This is providing a fair estimation of the execution speed but only the actual code execution can provide the final value.

Notation for Instruction Operands

Table 15 to Table 19 provide notation for Instruction Operands.

Table 15. Notation for Direct Addressing

Direct Address	Description	C251	C51
dir8	A direct 8-bit address. This can be a memory address (00h-7Fh) or a SFR address (80h-FFh). It is a byte (default), word or double word depending on the other operand.	3	3
dir16	A 16-bit memory address (00:0000h-00:FFFFh) used in direct addressing.	3	–

Logical AND[1]ANL <dest>, <src>dest opnd ← dest opnd Λ src opnd
Logical OR[1]ORL <dest>, <src>dest opnd ← dest opnd ς src opnd
Logical Exclusive OR[1]XRL <dest>, <src>dest opnd ← dest opnd ∀ src opnd
Clear[1]CLR A(A) ← 0
Complement[1]CPL A(A) ← ∅ (A)
Rotate LeftRL $A(A)_{n+1} \leftarrow (A)_n$, n = 0..6
$(A)_0 \leftarrow (A)_7$
Rotate Left CarryRLC $A(A)_{n+1} \leftarrow (A)_n$, n = 0..6
$(CY) \leftarrow (A)_7$
$(A)_0 \leftarrow (CY)$
Rotate RightRR $A(A)_{n-1} \leftarrow (A)_n$, n = 7..1
$(A)_7 \leftarrow (A)_0$
Rotate Right CarryRRC $A(A)_{n-1} \leftarrow (A)_n$, n = 7..1
$(CY) \leftarrow (A)_0$
$(A)_7 \leftarrow (CY)$

Mnemonic	<dest>, <src>[1]	Comments	Binary Mode		Source Mode	
			Bytes	States	Bytes	States
ANL ORL XRL	A, Rn	register to ACC	1	1	2	2
	A, dir8	Direct address (on-chip RAM or SFR) to ACC	2	1[3]	2	1[3]
	A, at Ri	Indirect address to ACC	1	2	2	3
	A, #data	Immediate data to ACC	2	1	2	1
	dir8, A	ACC to direct address	2	2[4]	2	2[4]
	dir8, #data	Immediate 8-bit data to direct address	3	3[4]	3	3[4]
	Rmd, Rms	Byte register to byte register	3	2	2	1
	WRjd, WRjs	Word register to word register	3	3	2	2
	Rm, #data	Immediate 8-bit data to byte register	4	3	3	2
	WRj, #data16	Immediate 16-bit data to word register	5	4	4	3
	Rm, dir8	Direct address (on-chip RAM or SFR) to byte register	4	3[3]	3	2[3]
	WRj, dir8	Direct address (on-chip RAM or SFR) to word register	4	4	3	3
	Rm, dir16	Direct address (64K) to byte register	5	3[5]	4	2[5]
	WRj, dir16	Direct address (64K) to word register	5	4[6]	4	3[6]
	Rm, at WRj	Indirect address (64K) to byte register	4	3[5]	3	2[5]
	Rm, at DRk	Indirect address (16M) to byte register	4	4[5]	3	3[5]
CLR	A	Clear ACC	1	1	1	1
CPL	A	Complement ACC	1	1	1	1
RL	A	Rotate ACC left	1	1	1	1
RLC	A	Rotate ACC left through CY	1	1	1	1
RR	A	Rotate ACC right	1	1	1	1
RRC	A	Rotate ACC right through CY	1	1	1	1

Table 24. Summary of Multiply, Divide and Decimal-adjust Instructions

MultiplyMUL AB(B:A) ← (A)×(B)
MUL <dest>, <src>extended dest opnd ← dest opnd × src opnd

DivideDIV AB(A) ← Quotient ((A)/(B))
(B) ← Remainder ((A)/(B))

DivideDIV <dest>, <src>ext. dest opnd high ← Quotient (dest opnd/src opnd)
ext. dest opnd low ← Remainder (dest opnd/src opnd)

Decimal-adjust ACCDA AIF [[$(A)_{3:0}$ > 9] ∨ [(AC) = 1]]
for Addition (BCD) THEN $(A)_{3:0} \leftarrow (A)_{3:0}$ + 6 !affects CY;
IF [[$(A)_{7:4}$ > 9] ∨ [(CY) = 1]]
THEN $(A)_{7:4} \leftarrow (A)_{7:4}$ + 6

Mnemonic	<dest>, <src>(1)	Comments	Binary Mode		Source Mode	
			Bytes	States	Bytes	States
MUL	AB	Multiply A and B	1	5	1	5
	Rmd, Rms	Multiply byte register and byte register	3	6	2	5
	WRjd, WRjs	Multiply word register and word register	3	12	2	11
DIV	AB	Divide A and B	1	10	1	10
	Rmd, Rms	Divide byte register and byte register	3	11	2	10
	WRjd, WRjs	Divide word register and word register	3	21	2	20
DA	A	Decimal adjust ACC	1	1	1	1

Note: 1. A shaded cell denotes an instruction in the C51 Architecture.

Table 25. Summary of Move Instructions (1/3)

Move to High wordMOVH <dest>, <src>dest $opnd_{31:16}$ ← src opnd Move with Sign extensionMOVS <dest>, <src>dest opnd ← src opnd with sign extend Move with Zero extensionMOVZ <dest>, <src>dest opnd ← src opnd with zero extend Move CodeMOVC A, <src>(A) ← src opnd Move eXtendedMOVX <dest>, <src>dest opnd ← src opnd						
Mnemonic	**<dest>, <src>(2)**	**Comments**	**Binary Mode**		**Source Mode**	
			Bytes	**States**	**Bytes**	**States**
MOVH	DRk, #data16	16-bit immediate data into upper word of dword register	5	3	4	2
MOVS	WRj, Rm	Byte register to word register with sign extension	3	2	2	1
MOVZ	WRj, Rm	Byte register to word register with zeros extension	3	2	2	1
MOVC	A, at A +DPTR	Code byte relative to DPTR to ACC	1	6(3)	1	6(3)
	A, at A +PC	Code byte relative to PC to ACC	1	6(3)	1	6(3)
MOVX	A, at Ri	Extended memory (8-bit address) to ACC(2)	1	4	1	5
	A, at DPTR	Extended memory (16-bit address) to ACC(2)	1	3(4)	1	3(4)
	at Ri, A	ACC to extended memory (8-bit address)(2)	1	4	1	4
	at DPTR, A	ACC to extended memory (16-bit address)(2)	1	4(3)	1	4(3)

Notes:
1. A shaded cell denotes an instruction in the C51 Architecture.
2. Extended memory addressed is in the region specified by DPXL (reset value = 01h).
3. If this instruction addresses external memory location, add N+1 to the number of states (N: number of wait states).
4. If this instruction addresses external memory location, add N+2 to the number of states (N: number of wait states).

Table 26. Summary of Move Instructions (2/3)

Move[1] MOV <dest>, <src> dest opnd ← src opnd						
			Binary Mode		Source Mode	
Mnemonic	<dest>, <src>[2]	Comments	Bytes	States	Bytes	States
MOV	A, Rn	Register to ACC	1	1	2	2
	A, dir8	Direct address (on-chip RAM or SFR) to ACC	2	1[3]	2	1[3]
	A, at Ri	Indirect address to ACC	1	2	2	3
	A, #data	Immediate data to ACC	2	1	2	1
	Rn, A	ACC to register	1	1	2	2
	Rn, dir8	Direct address (on-chip RAM or SFR) to register	2	1[3]	3	2[3]
	Rn, #data	Immediate data to register	2	1	3	2
	dir8, A	ACC to direct address (on-chip RAM or SFR)	2	2[3]	2	2[3]
	dir8, Rn	Register to direct address (on-chip RAM or SFR)	2	2[3]	3	3[3]
	dir8, dir8	Direct address to direct address (on-chip RAM or SFR)	3	3[4]	3	3[4]
	dir8, at Ri	Indirect address to direct address (on-chip RAM or SFR)	2	3[3]	3	4[3]
	dir8, #data	Immediate data to direct address (on-chip RAM or SFR)	3	3[3]	3	3[3]
	at Ri, A	ACC to indirect address	1	3	2	4
	at Ri, dir8	Direct address (on-chip RAM or SFR) to indirect address	2	3[3]	3	4[3]
	at Ri, #data	Immediate data to indirect address	2	3	3	4
	DPTR, #data16	Load Data Pointer with a 16-bit constant	3	2	3	2

Notes:
1. Instructions that move bits are in Table 27.
2. Move instructions from the C51 Architecture.
3. If this instruction addresses an I/O Port (Px, x = 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.
4. Apply note 3 for each dir8 operand.

MOV	WRj, at WRj +dis24	Indirect with 16-bit displacement (16M) to word register	5	8[5]	4	7[5]
MOV	at WRj +dis16, Rm	Byte register to indirect with 16-bit displacement (64K)	5	6[4]	4	5[4]
MOV	at WRj +dis16, WRj	Word register to indirect with 16-bit displacement (64K)	5	7[5]	4	6[5]
MOV	at DRk +dis24, Rm	Byte register to indirect with 16-bit displacement (16M)	5	7[4]	4	6[4]
MOV	at DRk +dis24, WRj	Word register to indirect with 16-bit displacement (16M)	5	8[5]	4	7[5]

Notes:
1. Instructions that move bits are in Table 27.
2. Move instructions unique to the C251 Architecture.
3. If this instruction addresses an I/O Port (Px, x = 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.
4. If this instruction addresses external memory location, add N+2 to the number of states (N: number of wait states).
5. If this instruction addresses external memory location, add 2(N+1) to the number of states (N: number of wait states).
6. If this instruction addresses external memory location, add 4(N+2) to the number of states (N: number of wait states).

Table 39. Bus Cycles AC Timings; V_{DD} = 4.5 to 5.5 V, T_A = -40 to 85°C

Symbol	Parameter	12 MHz		16 MHz		24 MHz		Unit
		Min	Max	Min	Max	Min	Max	
T_{OSC}	$1/F_{OSC}$	83		62		41		ns
T_{LHLL}	ALE Pulse Width	78		58		38		ns(2)
T_{AVLL}	Address Valid to ALE Low	78		58		37		ns(2)
T_{LLAX}	Address hold after ALE Low	19		11		3		ns
T_{RLRH}(1)	RD#/PSEN# Pulse Width	162		121		78		ns(3)
T_{WLWH}	WR# Pulse Width	165		124		81		ns(3)
T_{LLRL}(1)	ALE Low to RD#/PSEN# Low	22		14		6		ns
T_{LHAX}	ALE High to Address Hold	99		70		40		ns(2)
T_{RLDV}(1)	RD#/PSEN# Low to Valid Data		146		104		61	ns(3)
T_{RHDX}(1)	Data Hold After RD#/PSEN# High	0		0		0		ns
T_{RHAX}(1)	Address Hold After RD#/PSEN# High	0		0		0		ns
T_{RLAZ}(1)	RD#/PSEN# Low to Address Float		0		0		0	ns
T_{RHDZ1}	Instruction Float After RD#/PSEN# High		45		40		30	ns
T_{RHDZ2}	Data Float After RD#/PSEN# High		215		165		115	ns
T_{RHLH1}	RD#/PSEN# high to ALE High (Instruction)	49		43		31		ns
T_{RHLH2}	RD#/PSEN# high to ALE High (Data)	215		169		115		ns
T_{WHLH}	WR# High to ALE High	215		169		115		ns
T_{AVDV1}	Address (P0) Valid to Valid Data In		250		175		105	ns(2)(3)
T_{AVDV2}	Address (P2) Valid to Valid Data In		306		223		140	ns(2)(3)
T_{AVDV3}	Address (P0) Valid to Valid Instruction In		150		109		68	ns(3)
T_{AXDX}	Data Hold after Address Hold	0		0		0		ns
T_{AVRL}(1)	Address Valid to RD# Low	100		70		40		ns(2)
T_{AVWL1}	Address (P0) Valid to WR# Low	100		70		40		ns(2)
T_{AVWL2}	Address (P2) Valid to WR# Low	158		115		74		ns(2)
T_{WHQX}	Data Hold after WR# High	90		69		32		ns
T_{QVWH}	Data Valid to WR# High	133		102		72		ns(3)
T_{WHAX}	WR# High to Address Hold	167		125		84		ns

Notes:
1. Specification for PSEN# are identical to those for RD#.
2. If a wait state is added by extending ALE, add $2 \cdot T_{OSC.}$
3. If wait states are added by extending RD#/PSEN#/WR#, add $2N \cdot T_{OSC}$ (N = 1..3).

AC Characteristics - SSLC: TWI Interface

Timings

Table 47. TWI Interface AC Timing; V_{DD} = 2.7 to 5.5 V, T_A = -40 to 85°C

Symbol	Parameter	INPUT Min	INPUT Max	OUTPUT Min	OUTPUT Max
T_{HD}; STA	Start condition hold time	14·T_{CLCL}(4)		4.0 µs(1)	
T_{LOW}	SCL low time	16·T_{CLCL}(4)		4.7 µs(1)	
T_{HIGH}	SCL high time	14·T_{CLCL}(4)		4.0 µs(1)	
T_{RC}	SCL rise time	1 µs		-(2)	
T_{FC}	SCL fall time	0.3 µs		0.3 µs(3)	
T_{SU}; DAT1	Data set-up time	250 ns		20·T_{CLCL}(4)- T_{RD}	
T_{SU}; DAT2	SDA set-up time (before repeated START condition)	250 ns		1 µs(1)	
T_{SU}; DAT3	SDA set-up time (before STOP condition)	250 ns		8·T_{CLCL}(4)	
T_{HD}; DAT	Data hold time	0 ns		8·T_{CLCL}(4) - T_{FC}	
T_{SU}; STA	Repeated START set-up time	14·T_{CLCL}(4)		4.7 µs(1)	
T_{SU}; STO	STOP condition set-up time	14·T_{CLCL}(4)		4.0 µs(1)	
T_{BUF}	Bus free time	14·T_{CLCL}(4)		4.7 µs(1)	
T_{RD}	SDA rise time	1 µs		-(2)	
T_{FD}	SDA fall time	0.3 µs		0.3 µs(3)	

Notes:
1. At 100 kbit/s. At other bit-rates this value is inversely proportional to the bit-rate of 100 kbit/s.
2. Determined by the external bus-line capacitance and the external bus-line pull-up resistor, this must be < 1 µs.
3. Spikes on the SDA and SCL lines with a duration of less than 3·T_{CLCL} will be filtered out. Maximum capacitance on bus-lines SDA and SCL = 400 pF.
4. T_{CLCL} = T_{OSC} = one oscillator clock period.

Waveforms

Figure 18. TWI Waveforms

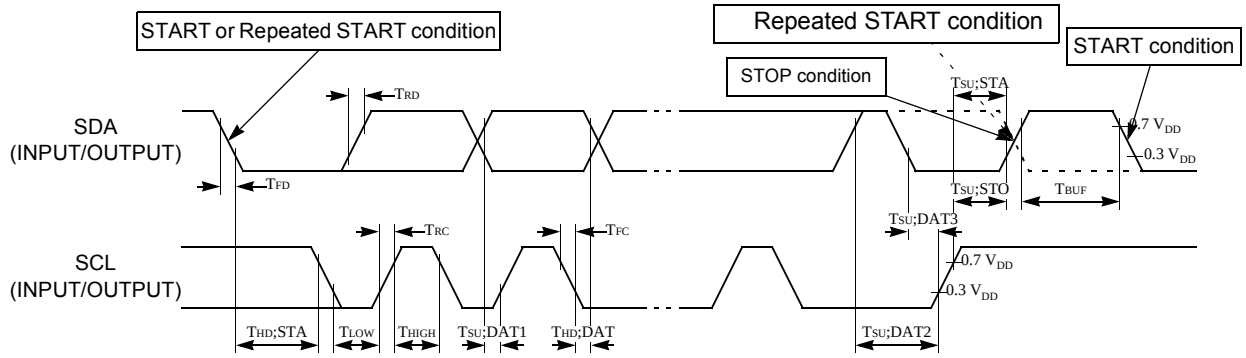
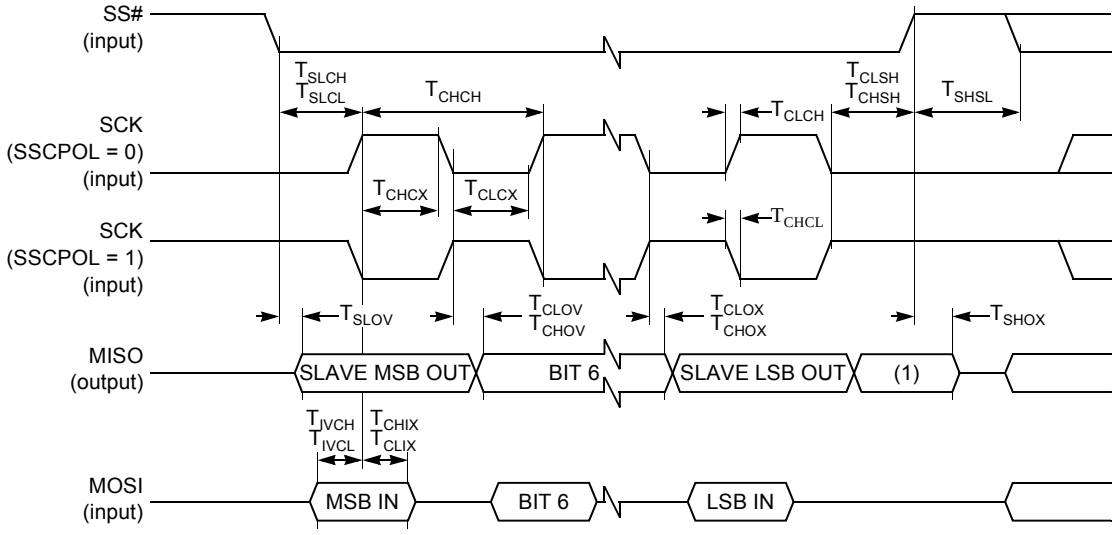
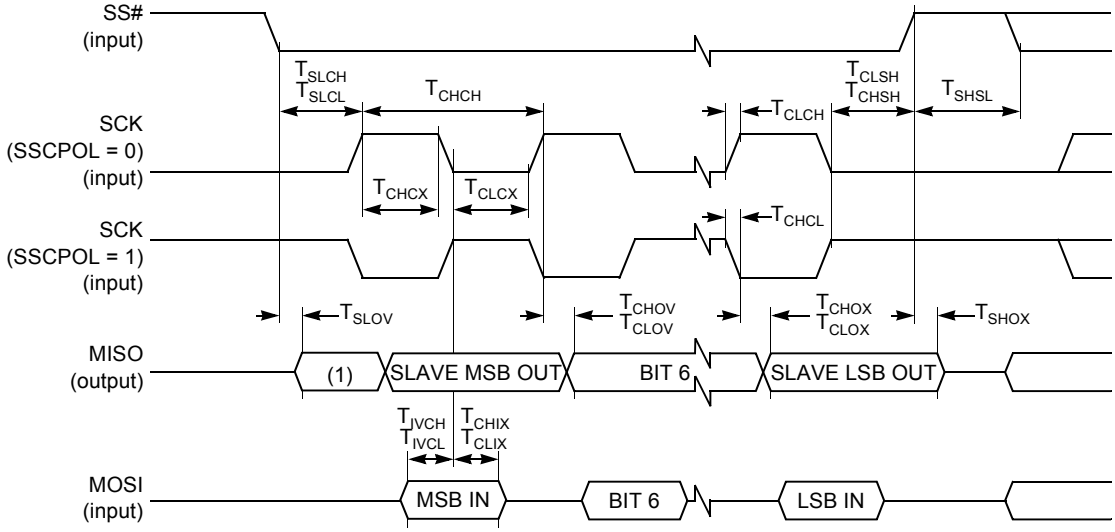


Figure 21. SPI Slave Waveforms (SSCPHA = 0)



Note: 1. Not Defined but generally the LSB of the character which has just been received.

Figure 22. SPI Slave Waveforms (SSCPHA = 1)



AC Characteristics - EPROM Programming and Verifying

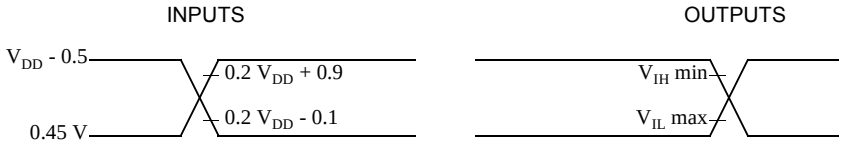
Definition of Symbols

Table 50. EPROM Programming and Verifying Timing Symbol Definitions

Signals	
A	Address
E	Enable: mode set on Port 0
G	Program
Q	Data Out
S	Supply (V_{PP})

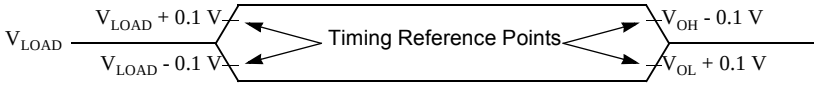
Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid
Z	Floating

Figure 26. AC Testing Input/Output Waveforms



Note: For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loading V_{OH}/V_{OL} level occurs with I_{OL}/I_{OH} = ±20 mA.

Figure 27. Float Waveforms



DC Characteristics

High Speed Versions - Commercial, Industrial, and Automotive

Table 55. DC Characteristics; V_{DD} = 4.5 to 5.5 V, T_A = -40 to +85°C

Symbol	Parameter	Min	Typical[4]	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (except EA#, SCL, SDA)	-0.5		$0.2 \cdot V_{DD}$ - 0.1	V	
V_{IL1}[5]	Input Low Voltage (SCL, SDA)	-0.5		$0.3 \cdot V_{DD}$	V	
V_{IL2}	Input Low Voltage (EA#)	0		$0.2 \cdot V_{DD}$ - 0.3	V	
V_{IH}	Input high Voltage (except XTAL1, RST, SCL, SDA)	$0.2 \cdot V_{DD}$ + 0.9		V_{DD} + 0.5	V	
V_{IH1}[5]	Input high Voltage (XTAL1, RST, SCL, SDA)	$0.7 \cdot V_{DD}$		V_{DD} + 0.5	V	
V_{OL}	Output Low Voltage (Ports 1, 2, 3)			0.3 0.45 1.0	V	I_{OL} = 100 µA[1][2] I_{OL} = 1.6 mA[1][2] I_{OL} = 3.5 mA[1][2]
V_{OL1}	Output Low Voltage (Ports 0, ALE, PSEN#, Port 2 in Page Mode during External Address)			0.3 0.45 1.0	V	I_{OL} = 200 µA[1][2] I_{OL} = 3.2 mA[1][2] I_{OL} = 7.0 mA[1][2]
V_{OH}	Output high Voltage (Ports 1, 2, 3, ALE, PSEN#)	V_{DD} - 0.3 V_{DD} - 0.7 V_{DD} - 1.5			V	I_{OH} = -10 µA[3] I_{OH} = -30 µA[3] I_{OH} = -60 µA[3]
V_{OH1}	Output high Voltage (Port 0, Port 2 in Page Mode during External Address)	V_{DD} - 0.3 V_{DD} - 0.7 V_{DD} - 1.5			V	I_{OH} = -200 µA I_{OH} = -3.2 mA I_{OH} = -7.0 mA
V_{RET}	V_{DD} data retention limit			1.8	V	
I_{IL0}	Logical 0 Input Current (Ports 1, 2, 3)			- 50	µA	V_{IN} = 0.45 V
I_{IL1}	Logical 1 Input Current (NMI)			+ 50	µA	V_{IN} = V_{DD}
I_{LI}	Input Leakage Current (Port 0)			± 10	µA	0.45 V < V_{IN} < V_{DD}
I_{TL}	Logical 1-to-0 Transition Current (Ports 1, 2, 3 - AWAIT#)			- 650	µA	V_{IN} = 2.0 V
R_{RST}	RST Pull-Down Resistor	40	110	225	kΩ	
C_{IO}	Pin Capacitance		10		pF	T_A = 25°C
I_{DD}	Operating Current		20 25 35	25 30 40	mA	F_{OSC} = 12 MHz F_{OSC} = 16 MHz F_{OSC} = 24 MHz
I_{DL}	Idle Mode Current		5 6.5 9.5	8 10 14	mA	F_{OSC} = 12 MHz F_{OSC} = 16 MHz F_{OSC} = 24 MHz
I_{PD}	Power-Down Current		2	20	µA	V_{RET} < V_{DD} < 5.5 V
V_{PP}	Programming supply voltage	12.5		13	V	T_A = 0 to +40°C
I_{PP}	Programming supply current			75	mA	T_A = 0 to +40°C

Low Voltage Versions - Commercial & Industrial

Table 56. DC Characteristics; V_{DD} = 2.7 to 5.5 V, T_A = -40 to +85°C

Symbol	Parameter	Min	Typical[4]	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (except EA#, SCL, SDA)	-0.5		$0.2 \cdot V_{DD}$ - 0.1	V	
V_{IL1}[5]	Input Low Voltage (SCL, SDA)	-0.5		$0.3 \cdot V_{DD}$	V	
V_{IL2}	Input Low Voltage (EA#)	0		$0.2 \cdot V_{DD}$ - 0.3	V	
V_{IH}	Input high Voltage (except XTAL1, RST, SCL, SDA)	$0.2 \cdot V_{DD}$ + 0.9		V_{DD} + 0.5	V	
V_{IH1}[5]	Input high Voltage (XTAL1, RST, SCL, SDA)	$0.7 \cdot V_{DD}$		V_{DD} + 0.5	V	
V_{OL}	Output Low Voltage (Ports 1, 2, 3)			0.45	V	I_{OL} = 0.8 mA[1][2]
V_{OL1}	Output Low Voltage (Ports 0, ALE, PSEN#, Port 2 in Page Mode during External Address)			0.45	V	I_{OL} = 1.6 mA[1][2]
V_{OH}	Output high Voltage (Ports 1, 2, 3, ALE, PSEN#)	$0.9 \cdot V_{DD}$			V	I_{OH} = -10 µA[3]
V_{OH1}	Output high Voltage (Port 0, Port 2 in Page Mode during External Address)	$0.9 \cdot V_{DD}$			V	I_{OH} = -40 µA
V_{RET}	V_{DD} data retention limit			1.8	V	
I_{IL0}	Logical 0 Input Current (Ports 1, 2, 3 - AWAIT#)			- 50	µA	V_{IN} = 0.45 V
I_{IL1}	Logical 1 Input Current (NMI)			+ 50	µA	$V_{IN} = V_{DD}$
I_{LI}	Input Leakage Current (Port 0)			± 10	µA	0.45 V < V_{IN} < V_{DD}
I_{TL}	Logical 1-to-0 Transition Current (Ports 1, 2, 3)			- 650	µA	V_{IN} = 2.0 V
R_{RST}	RST Pull-Down Resistor	40	110	225	kΩ	
C_{IO}	Pin Capacitance		10		pF	T_A = 25°C
I_{DD}	Operating Current		4 8 9 11	8 11 12 14	mA	5 MHz, V_{DD} < 3.6 V 10 MHz, V_{DD} < 3.6 V 12 MHz, V_{DD} < 3.6 V 16 MHz, V_{DD} < 3.6 V
I_{DL}	Idle Mode Current		0.5 1.5 2 3	1 4 5 7	mA	5 MHz, V_{DD} < 3.6 V 10 MHz, V_{DD} < 3.6 V 12 MHz, V_{DD} < 3.6 V 16 MHz, V_{DD} < 3.6 V
I_{PD}	Power-Down Current		1	10	µA	V_{RET} < V_{DD} < 3.6 V

Notes: 1. Under steady-state (non-transient) conditions, I_{OL} must be externally limited as follows:

Maximum IOL per port pin: 10 mA

Maximum IOL per 8-bit port: Port 0 26 mA

Ports 1-315 mA

Packages

List of Packages

- PDIL 40
- CDIL 40 with window
- PLCC 44
- CQPJ 44 with window
- VQFP 44 (10x10)

PDIL 40 - Mechanical Outline

Figure 33. Plastic Dual In Line

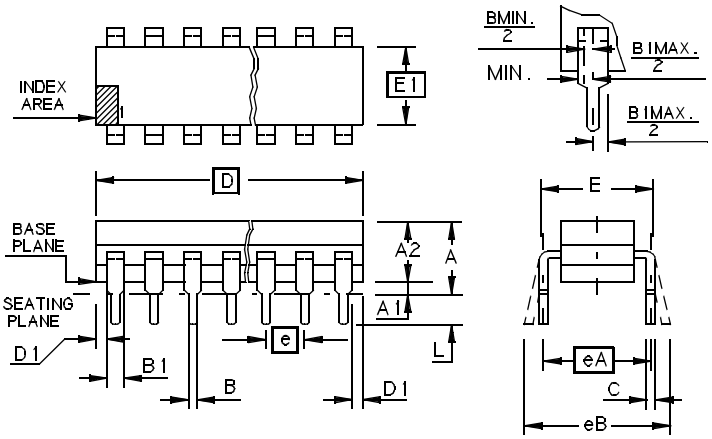


Table 57. PDIL Package Size

	MM		Inch	
	Min	**Max**	**Min**	**Max**
A	-	5.08	-	.200
A1	0.38	-	.015	-
A2	3.18	4.95	.125	.195
B	0.36	0.56	.014	.022
B1	0.76	1.78	.030	.070
C	0.20	0.38	.008	.015
D	50.29	53.21	1.980	2.095
E	15.24	15.87	.600	.625
E1	12.32	14.73	.485	.580
e	2.54 B.S.C.		.100 B.S.C.	
eA	15.24 B.S.C.		.600 B.S.C.	
eB	-	17.78	-	.700
L	2.93	3.81	.115	.150
D1	0.13	-	.005	-

PLCC 44 - Mechanical Outline

Figure 35. Plastic Lead Chip Carrier

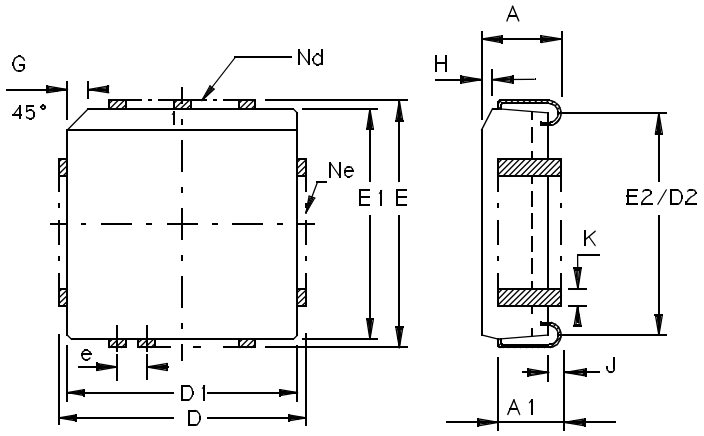


Table 59. PLCC Package Size

	MM		Inch	
	Min	**Max**	**Min**	**Max**
A	4.20	4.57	.165	.180
A1	2.29	3.04	.090	.120
D	17.40	17.65	.685	.695
D1	16.44	16.66	.647	.656
D2	14.99	16.00	.590	.630
E	17.40	17.65	.685	.695
E1	16.44	16.66	.647	.656
E2	14.99	16.00	.590	.630
e	1.27 BSC		.050 BSC	
G	1.07	1.22	.042	.048
H	1.07	1.42	.042	.056
J	0.51	-	.020	-
K	0.33	0.53	.013	.021
Nd	11		11	
Ne	11		11	

CQPJ 44 with Window - Mechanical Outline

Figure 36. Ceramic Quad Pack J

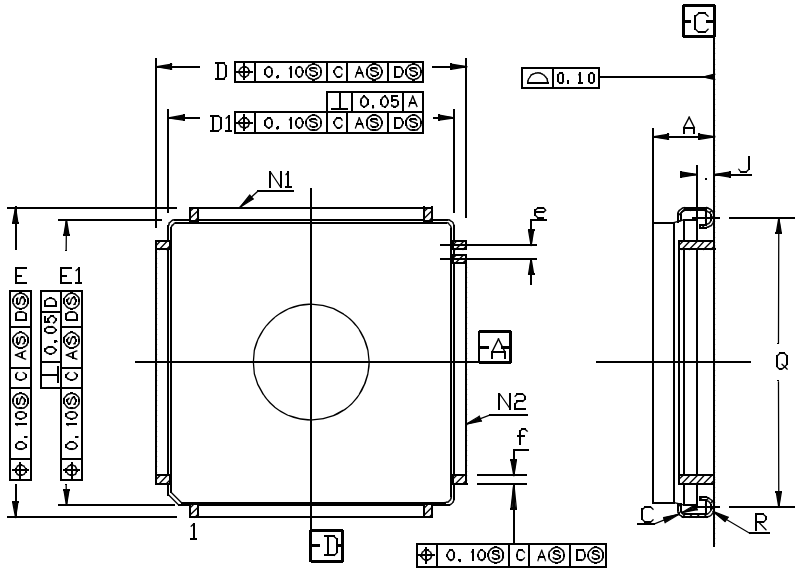


Table 60. CQPJ Package Size

	MM		Inch	
	Min	**Max**	**Min**	**Max**
A	-	4.90	-	.193
C	0.15	0.25	.006	.010
D - E	17.40	17.55	.685	.691
D1 - E1	16.36	16.66	.644	.656
e	1.27 TYP		.050 TYP	
f	0.43	0.53	.017	.021
J	0.86	1.12	.034	.044
Q	15.49	16.00	.610	.630
R	0.86 TYP		.034 TYP	
N1	11		11	
N2	11		11	

Ordering Information

AT/TSC80251G2D ROMless

Part Number	ROM	Description
High Speed Versions 4.5 to 5.5 V, Commercial and Industrial		
TSC80251G2D-16CB	ROMless	16 MHz, Commercial 0° to 70°C, PLCC 44
TSC80251G2D-24CB	ROMless	24 MHz, Commercial 0° to 70°C, PLCC 44
TSC80251G2D-24CE	ROMless	24 MHz, Commercial 0° to 70°C, VQFP 44
TSC80251G2D-24IA	ROMless	24 MHz, Industrial -40° to 85°C, PDIL 40
TSC80251G2D-24IB	ROMless	24 MHz, Industrial -40° to 85°C, PLCC 44
AT80251G2D-SLSUM	ROMless	24 MHz, Industrial & Green -40° to 85°C, PLCC 44
AT80251G2D-3CSUM	ROMless	24 MHz, Industrial & Green -40° to 85°C, PDIL 40
AT80251G2D-RLTUM	ROMless	24 MHz, Industrial & Green -40° to 85°C, VQFP 44
Low Voltage Versions 2.7 to 5.5 V		
TSC80251G2D-L16CB	ROMless	16 MHz, Commercial, PLCC 44
TSC80251G2D-L16CE	ROMless	16 MHz, Commercial, VQFP 44
AT80251G2D-SLSUL	ROMless	16 MHz, Industrial & Green, PLCC 44
AT80251G2D-RLTUL	ROMless	16 MHz, Industrial & Green, VQFP 44

AT/TSC83251G2D 32 kilobytes MaskROM

Part Number[1]	ROM	Description
High Speed Versions 4.5 to 5.5 V, Commercial and Industrial		
TSC251G2Dxxx-16CB	32K MaskROM	16 MHz, Commercial 0° to 70°C, PLCC 44
TSC251G2Dxxx-24CB	32K MaskROM	24 MHz, Commercial 0° to 70°C, PLCC 44
TSC251G2Dxxx-24CE	32K MaskROM	24 MHz, Commercial 0° to 70°C, VQFP 44
TSC251G2Dxxx-24IA	32K MaskROM	24 MHz, Industrial -40° to 85°C, PDIL 40
TSC251G2Dxxx-24IB	32K MaskROM	24 MHz, Industrial -40° to 85°C, PLCC 44
AT251G2Dxxx-SLSUM	32K MaskROM	24 MHz, Industrial & Green -40° to 85°C, PLCC 44
AT251G2Dxxx-3CSUM	32K MaskROM	24 MHz, Industrial & Green -40° to 85°C, PDIL 40
AT251G2Dxxx-RLTUM	32K MaskROM	24 MHz, Industrial & Green -40° to 85°C, VQFP 44
AT251G2Dxxx-SLSTM	32K MaskROM	24 MHz, Automotive & Green -40° to 85°C, PLCC 44