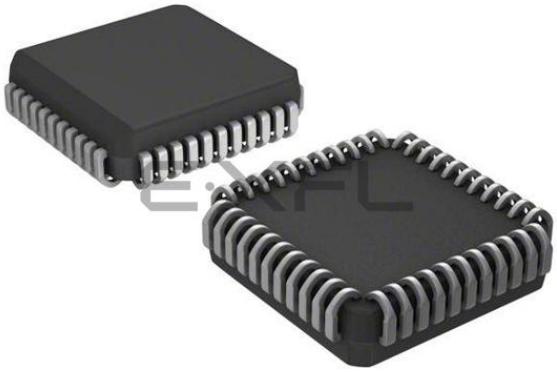

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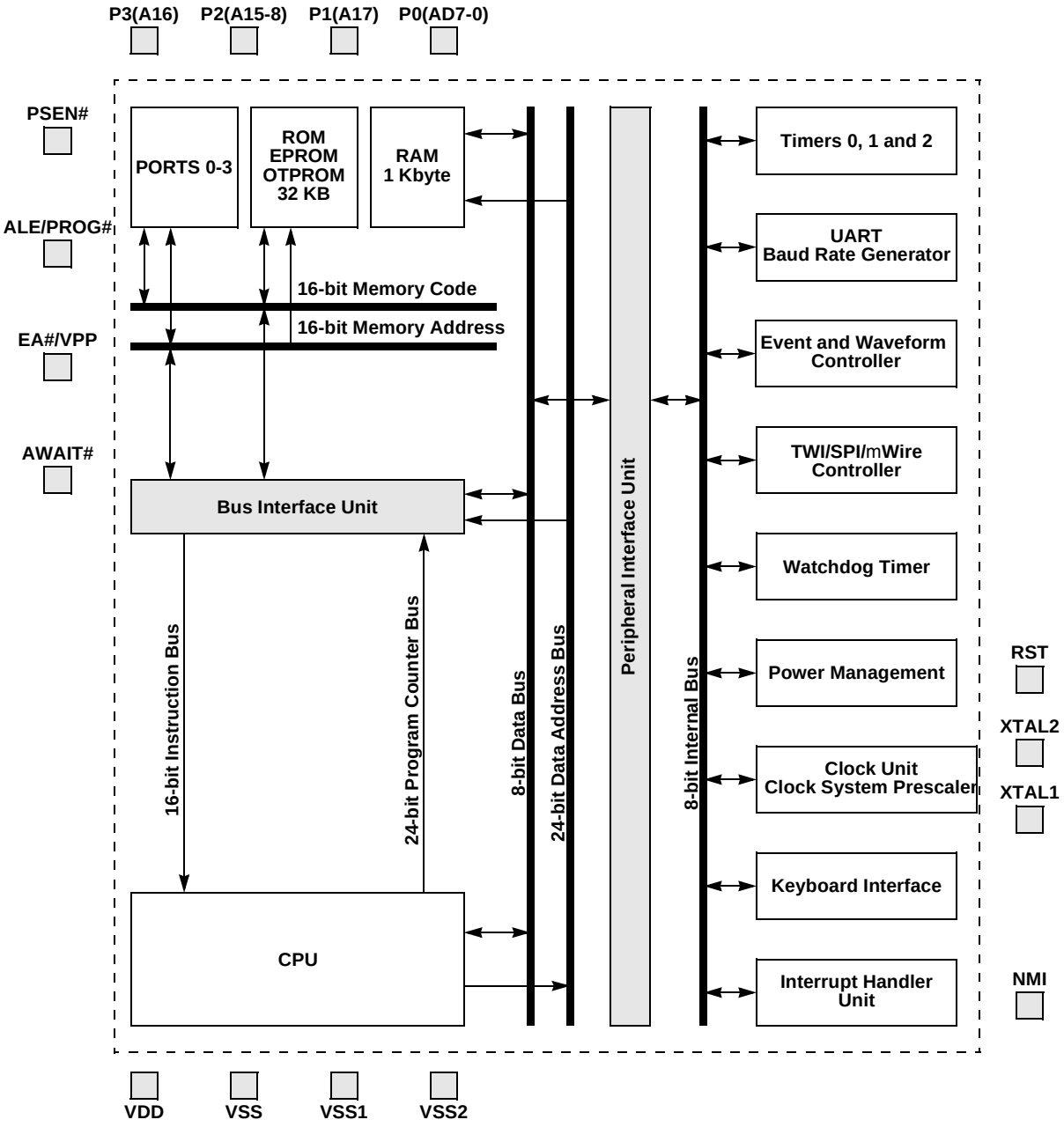
## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | C251 |
| Core Size | 8/16-Bit |
| Speed | 16MHz |
| Connectivity | EBI/EMI, I²C, Microwire, SPI, UART/USART |
| Peripherals | POR, PWM, WDT |
| Number of I/O | 32 |
| Program Memory Size | - |
| Program Memory Type | ROMless |
| EEPROM Size | - |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-LCC (J-Lead) |
| Supplier Device Package | 44-PLCC (16.6x16.6) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/tsc80251g2d-l16cb |

## Block Diagram



# Pin Description

## Pinout

**Figure 1.** TSC80251G2D 40-pin DIP package

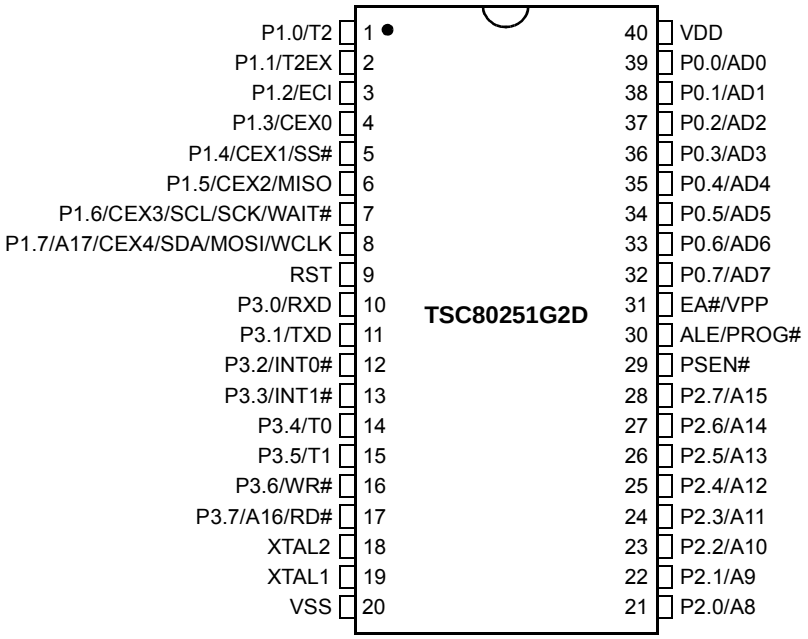



**Figure 2.** TSC80251G2D 44-pin PLCC Package

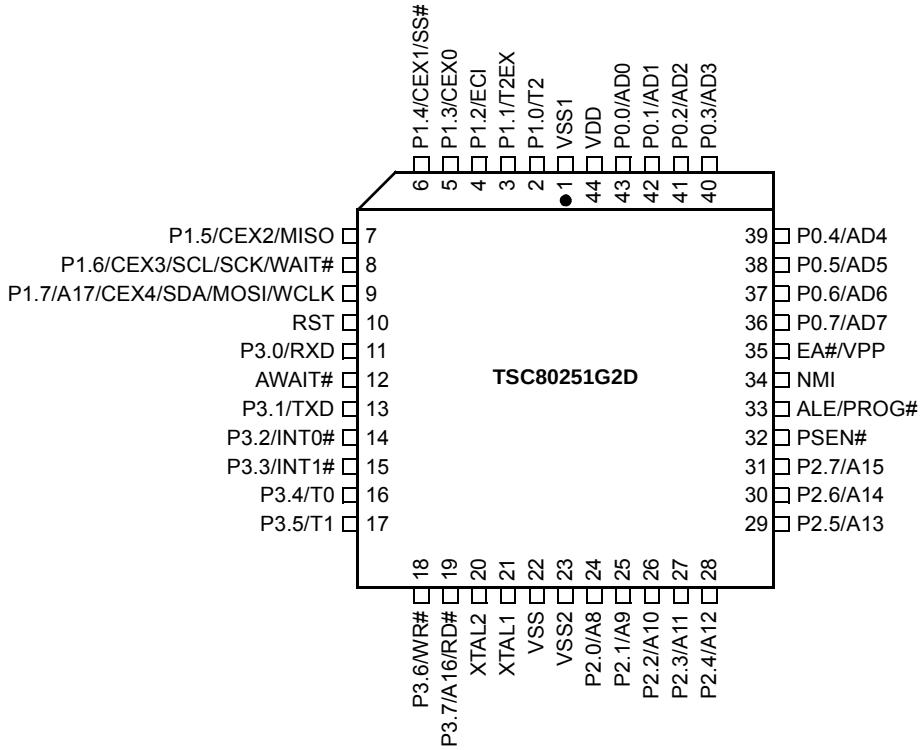


**Figure 3.** TSC80251G2D 44-pin VQFP Package

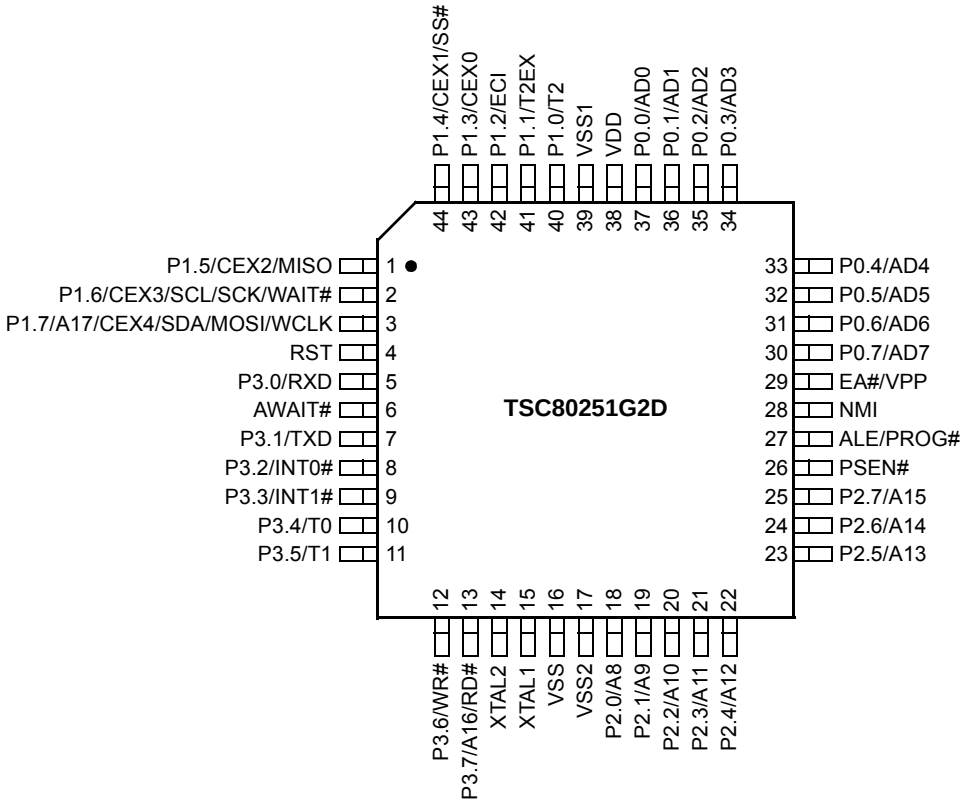


**Table 1.** TSC80251G2D Pin Assignment

| DIP | PLCC | VQFP | Name | DIP | PLCC | VQFP | Name |
|---|---|---|---|---|---|---|---|
| | 1 | 39 | VSS1 | | 23 | 17 | VSS2 |
| 1 | 2 | 40 | P1.0/T2 | 21 | 24 | 18 | P2.0/A8 |
| 2 | 3 | 41 | P1.1/T2EX | 22 | 25 | 19 | P2.1/A9 |
| 3 | 4 | 42 | P1.2/ECI | 23 | 26 | 20 | P2.2/A10 |
| 4 | 5 | 43 | P1.3/CEX0 | 24 | 27 | 21 | P2.3/A11 |
| 5 | 6 | 44 | P1.4/CEX1/SS# | 25 | 28 | 22 | P2.4/A12 |
| 6 | 7 | 1 | P1.5/CEX2/MISO | 26 | 29 | 23 | P2.5/A13 |
| 7 | 8 | 2 | P1.6/CEX3/SCL/SCK/WAIT# | 27 | 30 | 24 | P2.6/A14 |
| 8 | 9 | 3 | P1.7/A17/CEX4/SDA/MOSI/WCLK | 28 | 31 | 25 | P2.7/A15 |
| 9 | 10 | 4 | RST | 29 | 32 | 26 | PSEN# |
| 10 | 11 | 5 | P3.0/RXD | 30 | 33 | 27 | ALE/PROG# |
| | 12 | 6 | AWAIT# | | 34 | 28 | NMI |
| 11 | 13 | 7 | P3.1/TXD | 31 | 35 | 29 | EA#/VPP |
| 12 | 14 | 8 | P3.2/INT0# | 32 | 36 | 30 | P0.7/AD7 |
| 13 | 15 | 9 | P3.3/INT1# | 33 | 37 | 31 | P0.6/AD6 |
| 14 | 16 | 10 | P3.4/T0 | 34 | 38 | 32 | P0.5/AD5 |
| 15 | 17 | 11 | P3.5/T1 | 35 | 39 | 33 | P0.4/AD4 |
| 16 | 18 | 12 | P3.6/WR# | 36 | 40 | 34 | P0.3/AD3 |
| 17 | 19 | 13 | P3.7/A16/RD# | 37 | 41 | 35 | P0.2/AD2 |
| 18 | 20 | 14 | XTAL2 | 38 | 42 | 36 | P0.1/AD1 |
| 19 | 21 | 15 | XTAL1 | 39 | 43 | 37 | P0.0/AD0 |
| 20 | 22 | 16 | VSS | 40 | 44 | 38 | VDD |

## Signals

**Table 2.** Product Name Signal Description

| Signal Name | Type | Description | Alternate Function |
|---|---|---|---|
| A17 | O | **18th Address Bit**<br>Output to memory as 18th external address bit (A17) in extended bus applications, depending on the values of bits RD0 and RD1 in UCONFIG0 byte (see Table 13, Page 20). | P1.7 |
| A16 | O | **17th Address Bit**<br>Output to memory as 17th external address bit (A16) in extended bus applications, depending on the values of bits RD0 and RD1 in UCONFIG0 byte (see Table 13, Page 20). | P3.7 |
| A15:8(1) | O | **Address Lines**<br>Upper address lines for the external bus. | P2.7:0 |
| AD7:0(1) | I/O | **Address/Data Lines**<br>Multiplexed lower address lines and data for the external memory. | P0.7:0 |
| ALE | O | **Address Latch Enable**<br>ALE signals the start of an external bus cycle and indicates that valid address information are available on lines A16/A17 and A7:0. An external latch can use ALE to demultiplex the address from address/data bus. | – |
| AWAIT# | I | **Real-time Asynchronous Wait States Input**<br>When this pin is active (low level), the memory cycle is stretched until it becomes high. When using the Product Name as a pin-for-pin replacement for a 8xC51 product, AWAIT# can be unconnected without loss of compatibility or power consumption increase (on-chip pull-up).<br>Not available on DIP package. | – |
| CEX4:0 | I/O | **PCA Input/Output pins**<br>CEXx are input signals for the PCA capture mode and output signals for the PCA compare and PWM modes. | P1.7:3 |
| EA# | I | **External Access Enable**<br>EA# directs program memory accesses to on-chip or off-chip code memory.<br>For EA# = 0, all program memory accesses are off-chip.<br>For EA# = 1, an access is on-chip ROM if the address is within the range of the on-chip ROM; otherwise the access is off-chip. The value of EA# is latched at reset.<br>For devices without ROM on-chip, EA# must be strapped to ground. | – |
| ECI | O | **PCA External Clock input**<br>ECI is the external clock input to the 16-bit PCA timer. | P1.2 |
| MISO | I/O | **SPI Master Input Slave Output line**<br>When SPI is in master mode, MISO receives data from the slave peripheral. When SPI is in slave mode, MISO outputs data to the master controller. | P1.5 |
| MOSI | I/O | **SPI Master Output Slave Input line**<br>When SPI is in master mode, MOSI outputs data to the slave peripheral. When SPI is in slave mode, MOSI receives data from the master controller. | P1.7 |
| INT1:0# | I | **External Interrupts 0 and 1**<br>INT1#/INT0# inputs set IE1:0 in the TCON register. If bits IT1:0 in the TCON register are set, bits IE1:0 are set by a falling edge on INT1#/INT0#. If bits IT1:0 are cleared, bits IE1:0 are set by a low level on INT1#/INT0#. | P3.3:2 |

compatibility with the C51 Architecture). When PC increments beyond the end of segment FE:, it continues at the reset address FF:0000h (linearity). When PC increments beyond the end of segment 01:, it loops to the beginning of segment 00: (this prevents from its going into the reserved area).

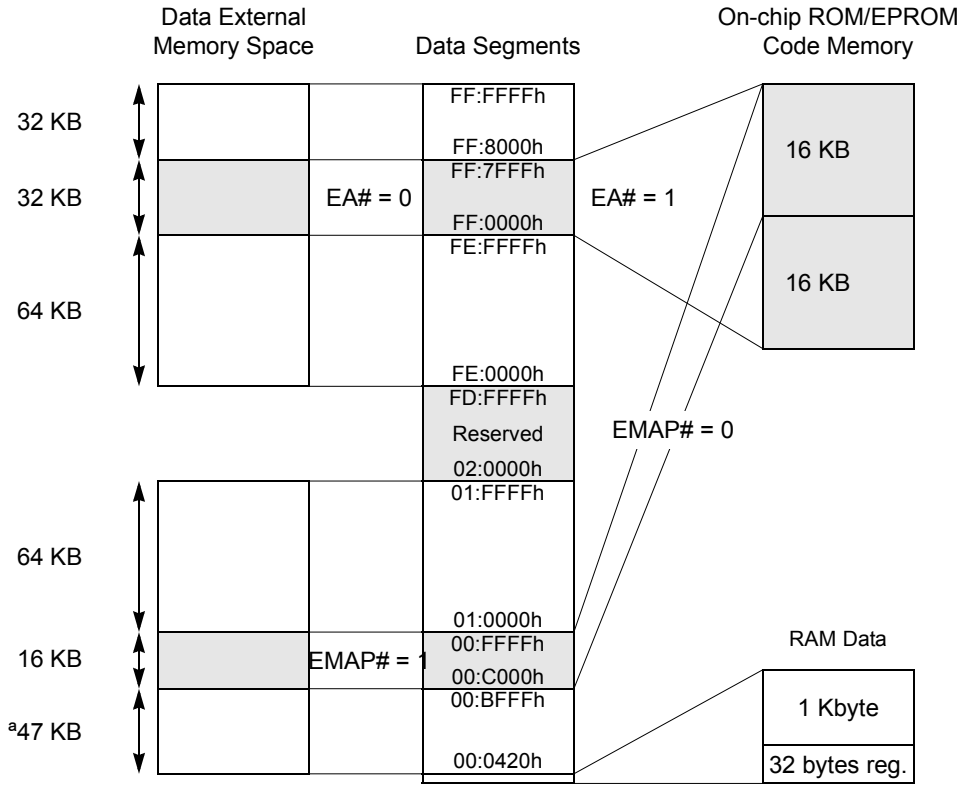
## Data Memory

The TSC80251G2D derivatives implement 1 Kbyte of on-chip data RAM. Figure 5 shows the split of the internal and external data memory spaces. This memory is mapped in the data space just over the 32 bytes of registers area (see TSC80251 Programmers' Guide). Hence, the part of the on-chip RAM located from 20h to FFh is bit addressable. This on-chip RAM is not accessible through the program/code memory space.

For faster computation with the on-chip ROM/EPROM code of the TSC83251G2D/TSC87251G2D, its upper 16 KB are also mapped in the upper part of the region 00: if the On-Chip Code Memory Map configuration bit is cleared (EMAP# bit in UCONFIG1 byte, see Figure ). However, if EA# is tied to a low level, the TSC80251G2D derivative is running as a ROMless product and the code is actually fetched in the corresponding external memory (i.e. the upper 16 KB of the lower 32 KB of the segment FF:). If EMAP# bit is set, the on-chip ROM is not accessible through the region 00:.

All the accesses to the portion of the data space with no on-chip memory mapped onto are redirected to the external memory.

**Figure 5.** Data Memory Mapping






4135F–8051–11/06

**Table 11.** Configuration Byte 0
UCONFIG0

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| - | WSA1# | WSA0# | XALE# | RD1 | RD0 | PAGE# | SRC |

| Bit Number | Bit Mnemonic | Description |
|---|---|---|
| 7 | - | **Reserved**<br>Set this bit when writing to UCONFIG0. |
| 6 | WSA1# | **Wait State A bits**<br>Select the number of wait states for RD#, WR# and PSEN# signals for external memory accesses (all regions except 01:).<br>WSA1# WSA0# Number of Wait States<br>0 0 3<br>0 1 2<br>1 0 1<br>1 1 0 |
| 5 | WSA0# | |
| 4 | XALE# | **Extend ALE bit**<br>Clear to extend the duration of the ALE pulse from $T_{OSC}$ to $3 \cdot T_{OSC}$.<br>Set to minimize the duration of the ALE pulse to $1 \cdot T_{OSC}$. |
| 3 | RD1 | **Memory Signal Select bits**<br>Specify a 18-bit, 17-bit or 16-bit external address bus and the usage of RD#, WR# and PSEN# signals (see Table 13). |
| 2 | RD0 | |
| 1 | PAGE# | **Page Mode Select bit**(1)<br>Clear to select the faster Page mode with A15:8/D7:0 on Port 2 and A7:0 on Port 0.<br>Set to select the non-Page mode(2) with A15:8 on Port 2 and A7:0/D7:0 on Port 0. |
| 0 | SRC | **Source Mode/Binary Mode Select bit**<br>Clear to select the binary mode.<br>Set to select the source mode. |

Notes: 1. UCONFIG0 is fetched twice so it can be properly read both in Page or Non-Page modes. If P2.1 is cleared during the first data fetch, a Page mode configuration is used, otherwise the subsequent fetches are performed in Non-Page mode.
2. This selection provides compatibility with the standard 80C51 hardware which is multiplexing the address LSB and the data on Port 0.

**Table 16.** Notation for Immediate Addressing

| Immediate Address | Description | C251 | C51 |
|---|---|---|---|
| #data | An 8-bit constant that is immediately addressed in an instruction | 3 | 3 |
| #data16 | A 16-bit constant that is immediately addressed in an instruction | 3 | – |
| #0data16<br>#1data16 | A 32-bit constant that is immediately addressed in an instruction. The upper word is filled with zeros (#0data16) or ones (#1data16). | 3 | – |
| #short | A constant, equal to 1, 2, or 4, that is immediately addressed in an instruction. | 3 | – |

**Table 17.** Notation for Bit Addressing

| Direct Address | Description | C251 | C51 |
|---|---|---|---|
| bit51 | A directly addressed bit (bit number = 00h-FFh) in memory or an SFR. Bits 00h-7Fh are the 128 bits in byte locations 20h-2Fh in the on-chip RAM. Bits 80h-FFh are the 128 bits in the 16 SFRs with addresses that end in 0h or 8h, S:80h, S:88h, S:90h,..., S:F0h, S:F8h. | – | 3 |
| bit | A directly addressed bit in memory locations 00:0020h-00:007Fh or in any defined SFR. | 3 | |

**Table 18.** Notation for Destination in Control Instructions

| Direct Address | Description | C251 | C51 |
|---|---|---|---|
| rel | A signed (two's complement) 8-bit relative address. The destination is -128 to +127 bytes relative to the next instruction's first byte. | 3 | 3 |
| addr11 | An 11-bit target address. The target is in the same 2-Kbyte block of memory as the next instruction's first byte. | – | 3 |
| addr16 | A 16-bit target address. The target can be anywhere within the same 64-Kbyte region as the next instruction's first byte. | – | 3 |
| addr24 | A 24-bit target address. The target can be anywhere within the 16-Mbyte address space. | 3 | – |

**Table 22.** Summary of Compare Instructions

| CompareCMP <dest>, <src>dest opnd - src opnd | | | | | | |
|---|---|---|---|---|---|---|
| | | | Binary Mode | | Source Mode | |
| **Mnemonic** | **<dest>, <src>(2)** | **Comments** | **Bytes** | **States** | **Bytes** | **States** |
| CMP | Rmd, Rms | Register with register | 3 | 2 | 2 | 1 |
| | WRjd, WRjs | Word register with word register | 3 | 3 | 2 | 2 |
| | DRkd, DRks | Dword register with dword register | 3 | 5 | 2 | 4 |
| | Rm, #data | Register with immediate data | 4 | 3 | 3 | 2 |
| | WRj, #data16 | Word register with immediate 16-bit data | 5 | 4 | 4 | 3 |
| | DRk, #0data16 | Dword register with zero-extended 16-bit immediate data | 5 | 6 | 4 | 5 |
| | DRk, #1data16 | Dword register with one-extended 16-bit immediate data | 5 | 6 | 4 | 5 |
| | Rm, dir8 | Direct address (on-chip RAM or SFR) with byte register | 4 | 3(1) | 3 | 2(1) |
| | WRj, dir8 | Direct address (on-chip RAM or SFR) with word register | 4 | 4 | 3 | 3 |
| | Rm, dir16 | Direct address (64K) with byte register | 5 | 3(2) | 4 | 2(2) |
| | WRj, dir16 | Direct address (64K) with word register | 5 | 4(3) | 4 | 3(3) |
| | Rm, at WRj | Indirect address (64K) with byte register | 4 | 3(2) | 3 | 2(2) |
| | Rm, at DRk | Indirect address (16M) with byte register | 4 | 4(2) | 3 | 3(2) |

Notes:
1. If this instruction addresses an I/O Port (Px, x = 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.
2. If this instruction addresses external memory location, add N+2 to the number of states (N: number of wait states).
3. If this instruction addresses external memory location, add 2(N+2) to the number of states (N: number of wait states).

| | | | | | | |
|---|---|---|---|---|---|---|
| MOV | WRj, at WRj +dis24 | Indirect with 16-bit displacement (16M) to word register | 5 | 8[5] | 4 | 7[5] |
| MOV | at WRj +dis16, Rm | Byte register to indirect with 16-bit displacement (64K) | 5 | 6[4] | 4 | 5[4] |
| MOV | at WRj +dis16, WRj | Word register to indirect with 16-bit displacement (64K) | 5 | 7[5] | 4 | 6[5] |
| MOV | at DRk +dis24, Rm | Byte register to indirect with 16-bit displacement (16M) | 5 | 7[4] | 4 | 6[4] |
| MOV | at DRk +dis24, WRj | Word register to indirect with 16-bit displacement (16M) | 5 | 8[5] | 4 | 7[5] |

Notes:
1. Instructions that move bits are in Table 27.
2. Move instructions unique to the C251 Architecture.
3. If this instruction addresses an I/O Port (Px, x = 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.
4. If this instruction addresses external memory location, add N+2 to the number of states (N: number of wait states).
5. If this instruction addresses external memory location, add 2(N+1) to the number of states (N: number of wait states).
6. If this instruction addresses external memory location, add 4(N+2) to the number of states (N: number of wait states).

**Table 29.** Summary of Conditional Jump Instructions (1/2)

| Jump conditional on statusJcc rel(PC) ← (PC) + size (instr);<br>IF [cc] THEN (PC) ← (PC) + rel | | | | | | |
|---|---|---|---|---|---|---|
| | | | Binary Mode | | Source Mode | |
| **Mnemonic** | **<dest>, <src>[1]** | **Comments** | **Bytes** | **States** | **Bytes** | **States** |
| JC | rel | Jump if carry | 2 | 1/4[3] | 2 | 1/4[3] |
| JNC | rel | Jump if not carry | 2 | 1/4[3] | 2 | 1/4[3] |
| JE | rel | Jump if equal | 3 | 2/5[3] | 2 | 1/4[3] |
| JNE | rel | Jump if not equal | 3 | 2/5[3] | 2 | 1/4[3] |
| JG | rel | Jump if greater than | 3 | 2/5[3] | 2 | 1/4[3] |
| JLE | rel | Jump if less than, or equal | 3 | 2/5[3] | 2 | 1/4[3] |
| JSL | rel | Jump if less than (signed) | 3 | 2/5[3] | 2 | 1/4[3] |
| JSLE | rel | Jump if less than, or equal (signed) | 3 | 2/5[3] | 2 | 1/4[3] |
| JSG | rel | Jump if greater than (signed) | 3 | 2/5[3] | 2 | 1/4[3] |
| JSGE | rel | Jump if greater than or equal (signed) | 3 | 2/5[3] | 2 | 1/4[3] |

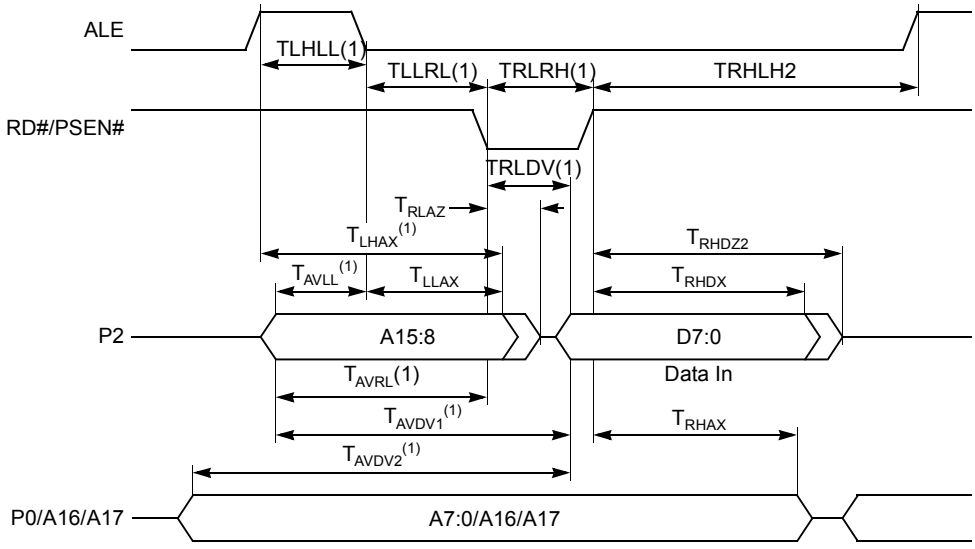
Notes:
1. A shaded cell denotes an instruction in the C51 Architecture.
2. States are given as jump not-taken/taken.
3. In internal execution only, add 1 to the number of states of the ‘jump taken’ if the destination address is internal and odd.

**Table 40.** Bus Cycles AC Timings; $V_{DD}$ = 2.7 to 5.5 V, $T_A$ = -40 to 85°C

| Symbol | Parameter | 12 MHz | | 16 MHz | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $T_{OSC}$ | $1/F_{OSC}$ | 83 | | 62 | | ns |
| $T_{LHLL}$ | ALE Pulse Width | 72 | | 52 | | ns(2) |
| $T_{AVLL}$ | Address Valid to ALE Low | 71 | | 51 | | ns(2) |
| $T_{LLAX}$ | Address hold after ALE Low | 14 | | 6 | | ns |
| $T_{RLRH}$(1) | RD#/PSEN# Pulse Width | 163 | | 121 | | ns(3) |
| $T_{WLWH}$ | WR# Pulse Width | 165 | | 124 | | ns(3) |
| $T_{LLRL}$(1) | ALE Low to RD#/PSEN# Low | 17 | | 11 | | ns |
| $T_{LHAX}$ | ALE High to Address Hold | 90 | | 57 | | ns(2) |
| $T_{RLDV}$(1) | RD#/PSEN# Low to Valid Data | | 133 | | 92 | ns(3) |
| $T_{RHDX}$(1) | Data Hold After RD#/PSEN# High | 0 | | 0 | | ns |
| $T_{RHAX}$(1) | Address Hold After RD#/PSEN# High | 0 | | 0 | | ns |
| $T_{RLAZ}$(1) | RD#/PSEN# Low to Address Float | | 0 | | 0 | ns |
| $T_{RHDZ1}$ | Instruction Float After RD#/PSEN# High | | 59 | | 48 | ns |
| $T_{RHDZ2}$ | Data Float After RD#/PSEN# High | | 225 | | 175 | ns |
| $T_{RHLH1}$ | RD#/PSEN# high to ALE High (Instruction) | 60 | | 47 | | ns |
| $T_{RHLH2}$ | RD#/PSEN# high to ALE High (Data) | 226 | | 172 | | ns |
| $T_{WHLH}$ | WR# High to ALE High | 226 | | 172 | | ns |
| $T_{AVDV1}$ | Address (P0) Valid to Valid Data In | | 289 | | 160 | ns(2)(3) |
| $T_{AVDV2}$ | Address (P2) Valid to Valid Data In | | 296 | | 211 | ns(2)(3) |
| $T_{AVDV3}$ | Address (P0) Valid to Valid Instruction In | | 144 | | 98 | ns(3) |
| $T_{AXDX}$ | Data Hold after Address Hold | 0 | | 0 | | ns |
| $T_{AVRL}$(1) | Address Valid to RD# Low | 111 | | 64 | | ns(2) |
| $T_{AVWL1}$ | Address (P0) Valid to WR# Low | 111 | | 64 | | ns(2) |
| $T_{AVWL2}$ | Address (P2) Valid to WR# Low | 158 | | 116 | | ns(2) |
| $T_{WHQX}$ | Data Hold after WR# High | 82 | | 66 | | ns |
| $T_{QVWH}$ | Data Valid to WR# High | 135 | | 103 | | ns(3) |
| $T_{WHAX}$ | WR# High to Address Hold | 168 | | 125 | | ns |

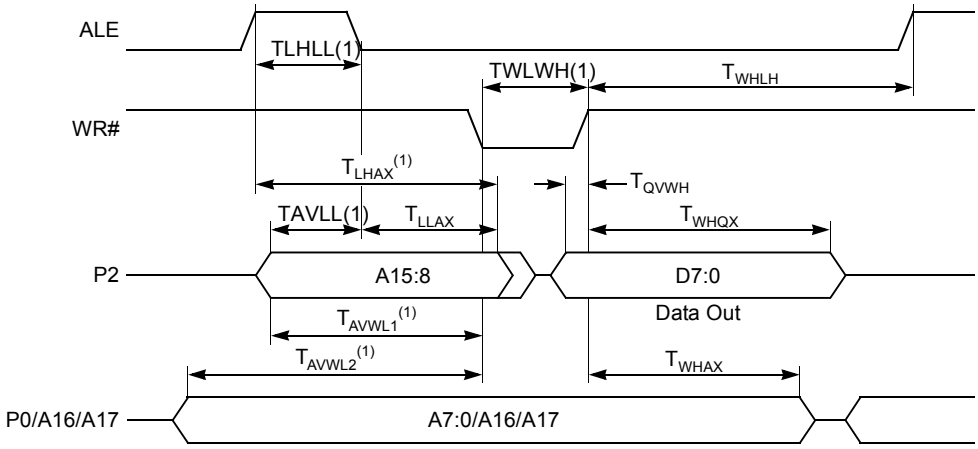
Notes: 1. Specification for PSEN# are identical to those for RD#.
2. If a wait state is added by extending ALE, add $2 \cdot T_{OSC.}$
3. If wait states are added by extending RD#/PSEN#/WR#, add $2N \cdot T_{OSC}$ (N = 1..3).

**Figure 12.** External Bus Cycle: Data Read (Page Mode)




Note: 1. The value of this parameter depends on wait states. See Table 39 and Table 40.

**Figure 13.** External Bus Cycle: Data Write (Page Mode)




Note: 1. The value of this parameter depends on wait states. See Table 39 and Table 40.

## AC Characteristics - Real-Time Synchronous Wait State

### Definition of Symbols

**Table 41.** Real-Time Synchronous Wait Timing Symbol Definitions

| Signals | |
|---|---|
| C | WCLK |
| R | RD#/PSEN# |
| W | WR# |
| Y | WAIT# |

| Conditions | |
|---|---|
| L | Low |
| V | Valid |
| X | No Longer Valid |

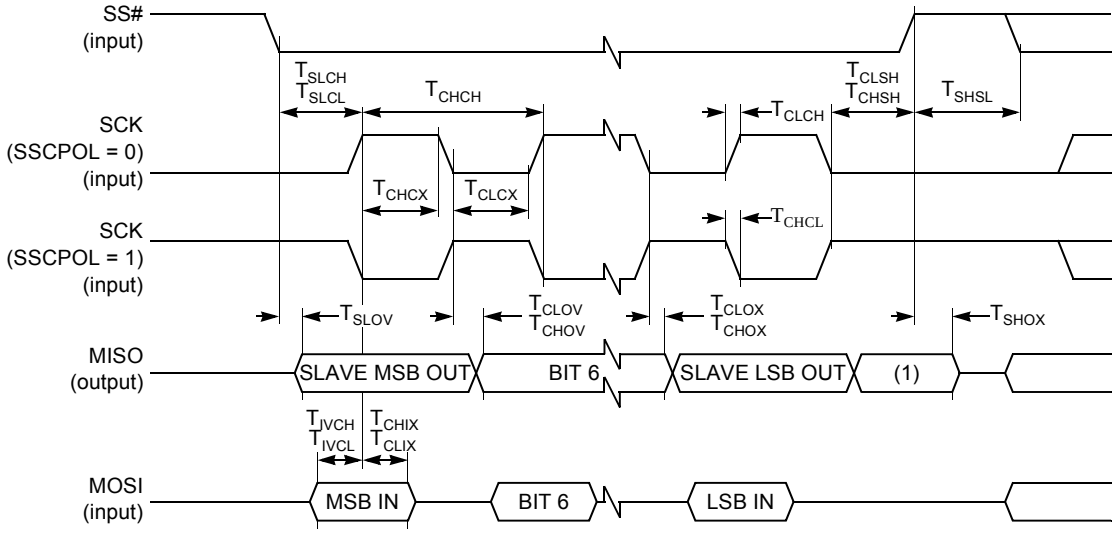
**Timings**

**Table 49.** SPI Interface AC Timing; $V_{DD}$ = 2.7 to 5.5 V, $T_A$ = -40 to 85°C

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| **Slave Mode(1)** | | | | |
| $T_{CHCH}$ | Clock Period | 8 | | $T_{OSC}$ |
| $T_{CHCX}$ | Clock High Time | 3.2 | | $T_{OSC}$ |
| $T_{CLCX}$ | Clock Low Time | 3.2 | | $T_{OSC}$ |
| $T_{SLCH}$, $T_{SLCL}$ | SS# Low to Clock edge | 200 | | ns |
| $T_{IVCL}$, $T_{IVCH}$ | Input Data Valid to Clock Edge | 100 | | ns |
| $T_{CLIX}$, $T_{CHIX}$ | Input Data Hold after Clock Edge | 100 | | ns |
| $T_{CLOV,}$ $T_{CHOV}$ | Output Data Valid after Clock Edge | | 100 | ns |
| $T_{CLOX}$, $T_{CHOX}$ | Output Data Hold Time after Clock Edge | 0 | | ns |
| $T_{CLSH}$, $T_{CHSH}$ | SS# High after Clock Edge | 0 | | ns |
| $T_{IVCL}$, $T_{IVCH}$ | Input Data Valid to Clock Edge | 100 | | ns |
| $T_{CLIX}$, $T_{CHIX}$ | Input Data Hold after Clock Edge | 100 | | ns |
| $T_{SLOV}$ | SS# Low to Output Data Valid | | 130 | ns |
| $T_{SHOX}$ | Output Data Hold after SS# High | | 130 | ns |
| $T_{SHSL}$ | SS# High to SS# Low | (2) | | |
| $T_{ILIH}$ | Input Rise Time | | 2 | µs |
| $T_{IHIL}$ | Input Fall Time | | 2 | µs |
| $T_{OLOH}$ | Output Rise time | | 100 | ns |
| $T_{OHOL}$ | Output Fall Time | | 100 | ns |
| **Master Mode(3)** | | | | |
| $T_{CHCH}$ | Clock Period | 4 | | $T_{OSC}$ |
| $T_{CHCX}$ | Clock High Time | 1.6 | | $T_{OSC}$ |
| $T_{CLCX}$ | Clock Low Time | 1.6 | | $T_{OSC}$ |
| $T_{IVCL}$, $T_{IVCH}$ | Input Data Valid to Clock Edge | 50 | | ns |
| $T_{CLIX}$, $T_{CHIX}$ | Input Data Hold after Clock Edge | 50 | | ns |
| $T_{CLOV,}$ $T_{CHOV}$ | Output Data Valid after Clock Edge | | 65 | ns |
| $T_{CLOX}$, $T_{CHOX}$ | Output Data Hold Time after Clock Edge | 0 | | ns |
| $T_{ILIH}$ | Input Data Rise Time | | 2 | µs |
| $T_{IHIL}$ | Input Data Fall Time | | 2 | µs |
| $T_{OLOH}$ | Output Data Rise time | | 50 | ns |
| $T_{OHOL}$ | Output Data Fall Time | | 50 | ns |

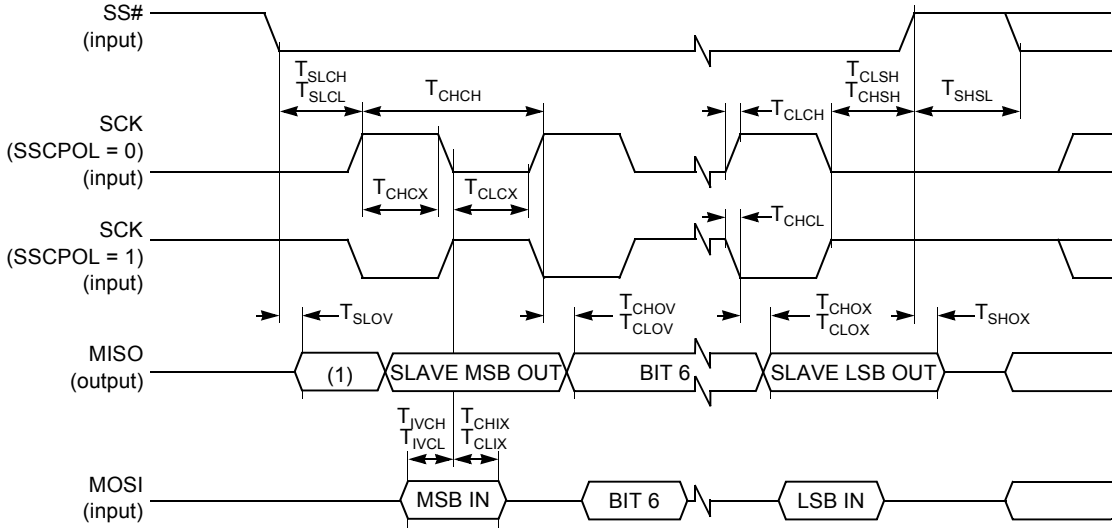
Notes: 1. Capacitive load on all pins = 200 pF in slave mode.
2. The value of this parameter depends on software.
3. Capacitive load on all pins = 100 pF in master mode.

**Figure 21.** SPI Slave Waveforms (SSCPHA = 0)




Note: 1. Not Defined but generally the LSB of the character which has just been received.

**Figure 22.** SPI Slave Waveforms (SSCPHA = 1)




## AC Characteristics - EPROM Programming and Verifying

### Definition of Symbols

**Table 50.** EPROM Programming and Verifying Timing Symbol Definitions

| Signals | |
|---|---|
| A | Address |
| E | Enable: mode set on Port 0 |
| G | Program |
| Q | Data Out |
| S | Supply ($V_{PP}$) |

| Conditions | |
|---|---|
| H | High |
| L | Low |
| V | Valid |
| X | No Longer Valid |
| Z | Floating |

## Timings

**Table 51.** EPROM Programming AC timings; $V_{DD}$ = 4.5 to 5.5 V, $T_A$ = 0 to 40°C

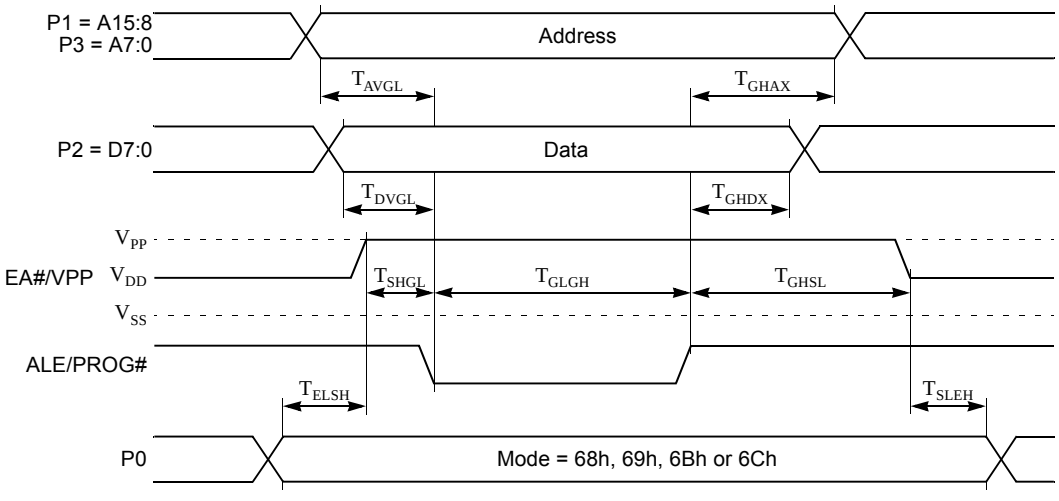
| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $T_{OSC}$ | XTAL1 Period | 83.5 | 250 | ns |
| $T_{AVGL}$ | Address Setup to PROG# low | 48 | | $T_{OSC}$ |
| $T_{GHAX}$ | Address Hold after PROG# low | 48 | | $T_{OSC}$ |
| $T_{DVGL}$ | Data Setup to PROG# low | 48 | | $T_{OSC}$ |
| $T_{GHDX}$ | Data Hold after PROG# | 48 | | $T_{OSC}$ |
| $T_{ELSH}$ | ENABLE High to $V_{PP}$ | 48 | | $T_{OSC}$ |
| $T_{SHGL}$ | $V_{PP}$ Setup to PROG# low | 10 | | µs |
| $T_{GHSL}$ | $V_{PP}$ Hold after PROG# | 10 | | µs |
| $T_{SLEH}$ | ENABLE Hold after $V_{PP}$ | 0 | | ns |
| $T_{GLGH}$ | PROG# Width | 90 | 110 | µs |

**Table 52.** EPROM Verifying AC timings; $V_{DD}$ = 4.5 to 5.5 V, $V_{DD}$ = 2.7 to 5.5 V, $T_A$ = 0 to 40°C

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $T_{OSC}$ | XTAL1 Period | 83.5 | 250 | ns |
| $T_{AVQV}$ | Address to Data Valid | | 48 | $T_{OSC}$ |
| $T_{AXQX}$ | Address to Data Invalid | 0 | | ns |
| $T_{ELQV}$ | ENABLE low to Data Valid | 0 | 48 | $T_{OSC}$ |
| $T_{EHQZ}$ | Data Float after ENABLE | 0 | 48 | $T_{OSC}$ |

## Waveforms

**Figure 23.** EPROM Programming Waveforms



Notes: 1. Under steady-state (non-transient) conditions, $I_{OL}$ must be externally limited as follows:

Maximum IOL per port pin: 10 mA

Maximum IOL per 8-bit port:Port 0 26 mA

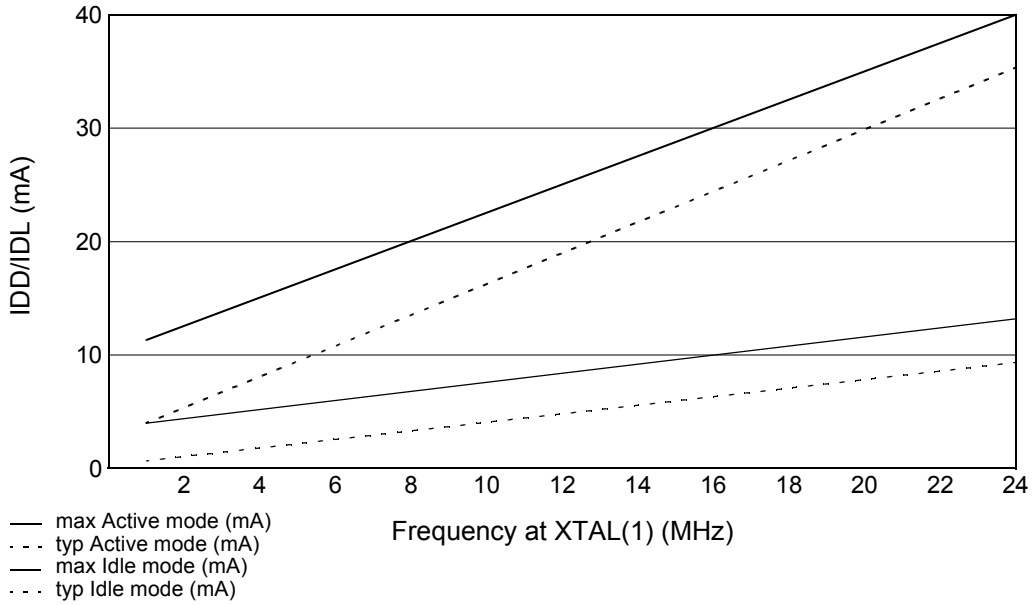
Ports 1-3 15 mA

Maximum Total IOL for all: Output Pins 71 mA

If IOL exceeds the test conditions, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

2. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses above 0.4 V on the low-level outputs of ALE and Ports 1, 2, and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from high to low. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8 V. It may be desirable to qualify ALE or other signals with a Schmitt Trigger or CMOS-level input logic.
3. Capacitive loading on Ports 0 and 2 causes the $V_{OH}$ on ALE and PSEN# to drop below the specification when the address lines are stabilizing.
4. Typical values are obtained using $V_{DD}$ = 5 V and $T_A$ = 25°C. They are not tested and there is not guarantee on these values.
5. The input threshold voltage of SCL and SDA meets the TWI specification, so an input voltage below $0.3 \cdot V_{DD}$ will be recognized as a logic 0 while an input voltage above $0.7 \cdot V_{DD}$ will be recognized as a logic 1.

**Figure 28.** $I_{DD}/I_{DL}$ Versus Frequency; $V_{DD}$ = 4.5 to 5.5 V




Note: 1. The clock prescaler is not used: $F_{OSC} = F_{XTAL}$.

**Figure 31.** $I_{DL}$ Test Condition, Idle Mode

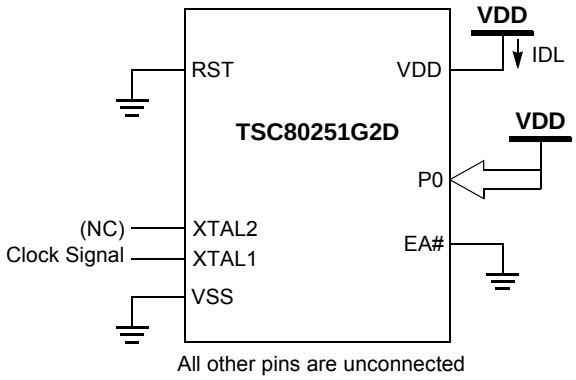
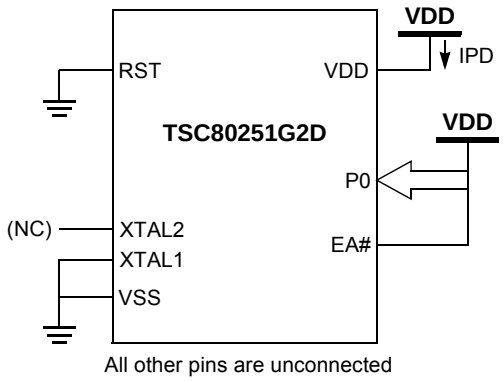



**Figure 32.** $I_{PD}$ Test Condition, Power-Down Mode



## PLCC 44 - Mechanical Outline

**Figure 35.** Plastic Lead Chip Carrier

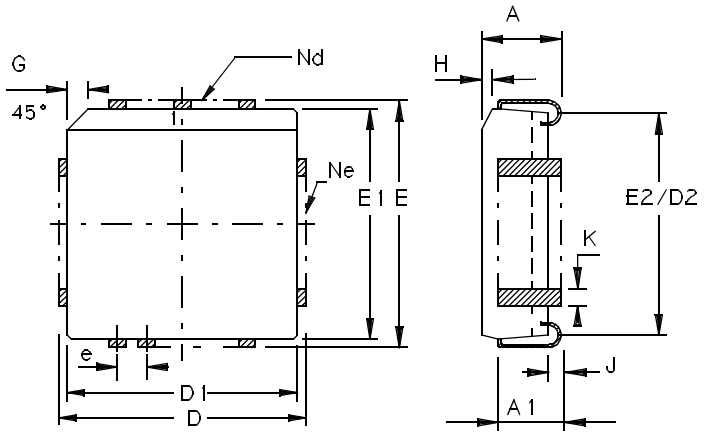



**Table 59.** PLCC Package Size

| | MM | | Inch | |
|---|---|---|---|---|
| | **Min** | **Max** | **Min** | **Max** |
| A | 4.20 | 4.57 | .165 | .180 |
| A1 | 2.29 | 3.04 | .090 | .120 |
| D | 17.40 | 17.65 | .685 | .695 |
| D1 | 16.44 | 16.66 | .647 | .656 |
| D2 | 14.99 | 16.00 | .590 | .630 |
| E | 17.40 | 17.65 | .685 | .695 |
| E1 | 16.44 | 16.66 | .647 | .656 |
| E2 | 14.99 | 16.00 | .590 | .630 |
| e | 1.27 BSC | | .050 BSC | |
| G | 1.07 | 1.22 | .042 | .048 |
| H | 1.07 | 1.42 | .042 | .056 |
| J | 0.51 | - | .020 | - |
| K | 0.33 | 0.53 | .013 | .021 |
| Nd | 11 | | 11 | |
| Ne | 11 | | 11 | |

## CQPJ 44 with Window - Mechanical Outline

**Figure 36.** Ceramic Quad Pack J

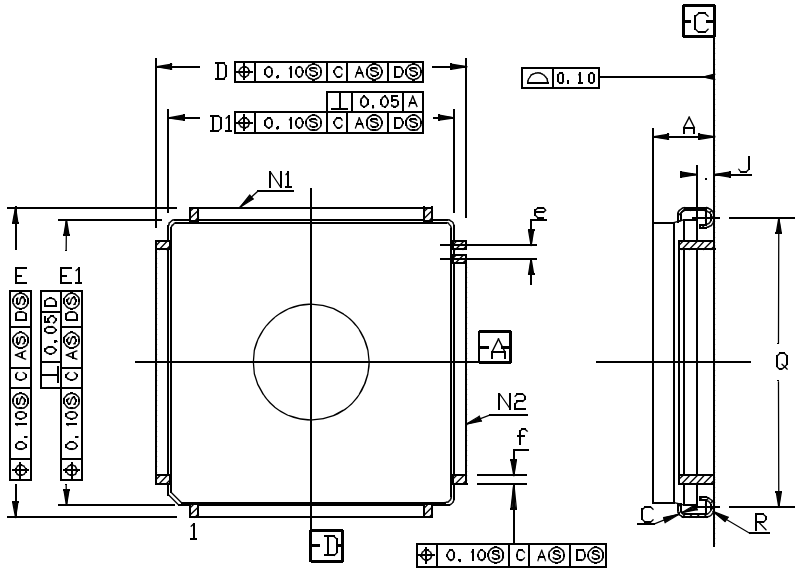



**Table 60.** CQPJ Package Size

| | MM | | Inch | |
|---|---|---|---|---|
| | **Min** | **Max** | **Min** | **Max** |
| A | - | 4.90 | - | .193 |
| C | 0.15 | 0.25 | .006 | .010 |
| D - E | 17.40 | 17.55 | .685 | .691 |
| D1 - E1 | 16.36 | 16.66 | .644 | .656 |
| e | 1.27 TYP | | .050 TYP | |
| f | 0.43 | 0.53 | .017 | .021 |
| J | 0.86 | 1.12 | .034 | .044 |
| Q | 15.49 | 16.00 | .610 | .630 |
| R | 0.86 TYP | | .034 TYP | |
| N1 | 11 | | 11 | |
| N2 | 11 | | 11 | |