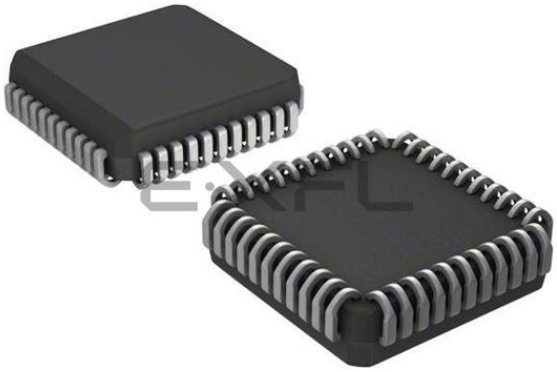

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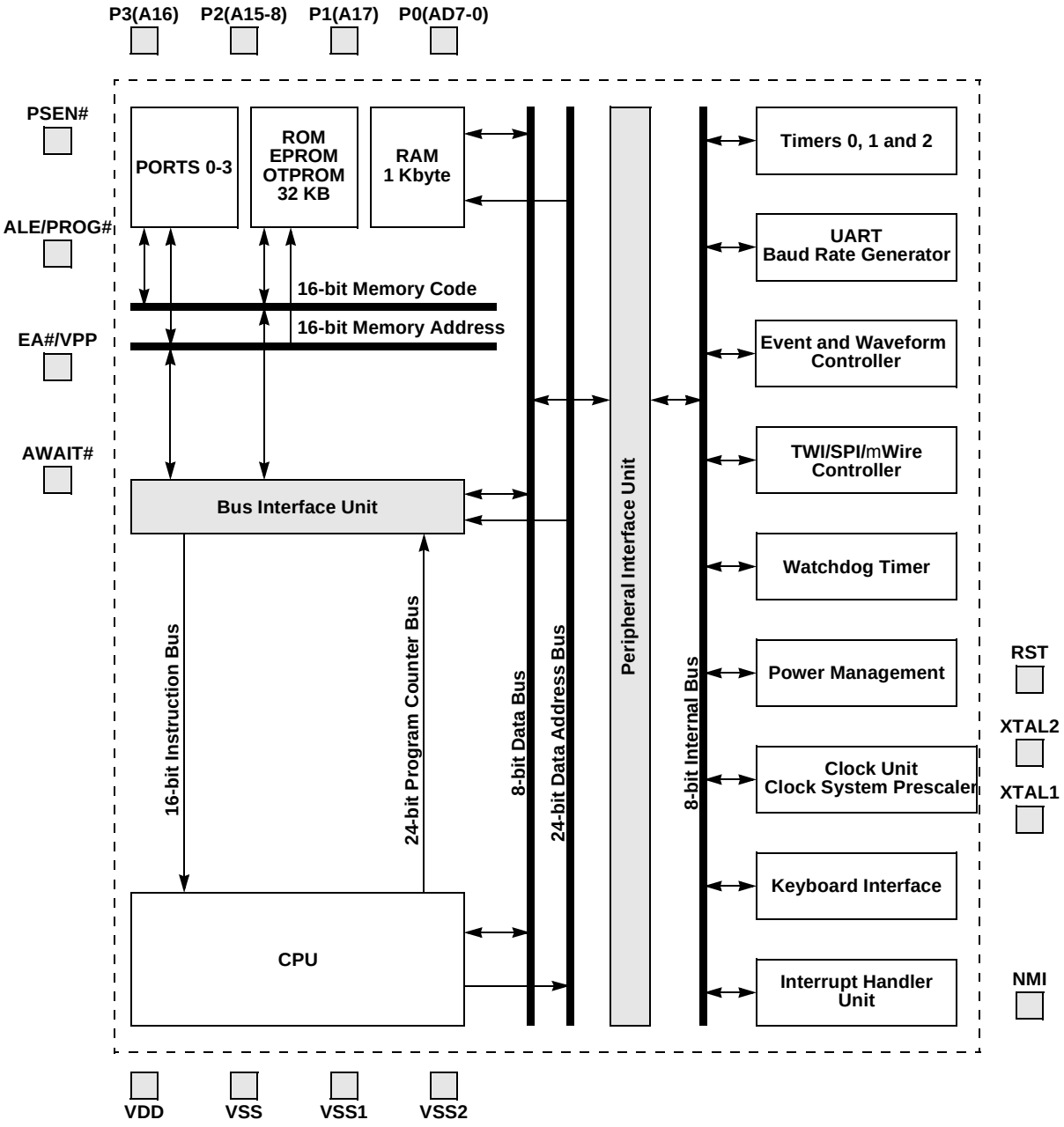
## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | C251 |
| Core Size | 8/16-Bit |
| Speed | 16MHz |
| Connectivity | EBI/EMI, I²C, Microwire, SPI, UART/USART |
| Peripherals | POR, PWM, WDT |
| Number of I/O | 32 |
| Program Memory Size | - |
| Program Memory Type | ROMless |
| EEPROM Size | - |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-LCC (J-Lead) |
| Supplier Device Package | 44-PLCC (16.6x16.6) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/tsc80251g2d-l16cbr |

## Block Diagram



# Pin Description

## Pinout

**Figure 1.** TSC80251G2D 40-pin DIP package

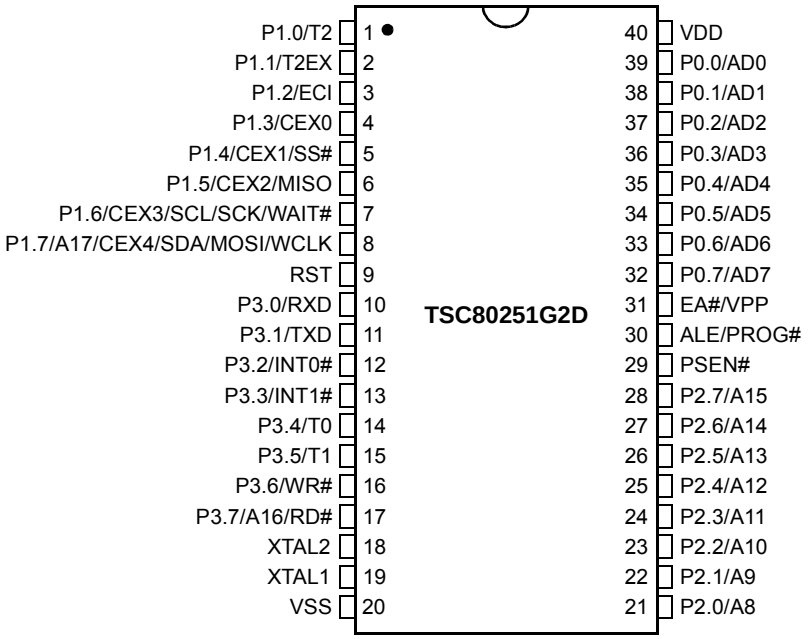



**Figure 2.** TSC80251G2D 44-pin PLCC Package

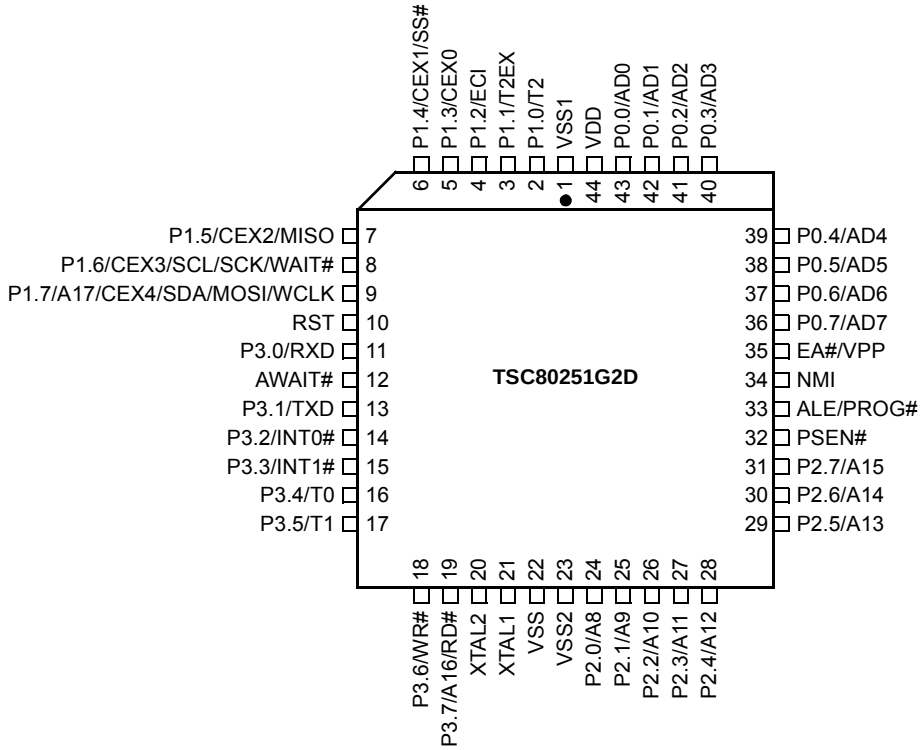


**Table 2.** Product Name Signal Description (Continued)

| Signal Name | Type | Description | Alternate Function |
|---|---|---|---|
| NMI | I | **Non Maskable Interrupt**<br>Holding this pin high for 24 oscillator periods triggers an interrupt.<br>When using the Product Name as a pin-for-pin replacement for a 8xC51 product, NMI can be unconnected without loss of compatibility or power consumption increase (on-chip pull-down).<br>Not available on DIP package. | – |
| P0.0:7 | I/O | **Port 0**<br>P0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. To avoid any paraitic current consumption, Floating P0 inputs must be polarized to $V_{DD}$ or $V_{SS}$. | AD7:0 |
| P1.0:7 | I/O | **Port 1**<br>P1 is an 8-bit bidirectional I/O port with internal pull-ups. P1 provides interrupt capability for a keyboard interface. | – |
| P2.0:7 | I/O | **Port 2**<br>P2 is an 8-bit bidirectional I/O port with internal pull-ups. | A15:8 |
| P3.0:7 | I/O | **Port 3**<br>P3 is an 8-bit bidirectional I/O port with internal pull-ups. | – |
| PROG# | I | **Programming Pulse input**<br>The programming pulse is applied to this input for programming the on-chip EPROM/OTPROM. | – |
| PSEN# | O | **Program Store Enable/Read signal output**<br>PSEN# is asserted for a memory address range that depends on bits RD0 and RD1 in UCONFIG0 byte (see ). | – |
| RD# | O | **Read or 17$^{th}$ Address Bit (A16)**<br>Read signal output to external data memory depending on the values of bits RD0 and RD1 in UCONFIG0 byte (see Table 13, Page 20). | P3.7 |
| RST | I | **Reset input to the chip**<br>Holding this pin high for 64 oscillator periods while the oscillator is running resets the device. The Port pins are driven to their reset conditions when a voltage greater than $V_{IH1}$ is applied, whether or not the oscillator is running. This pin has an internal pull-down resistor which allows the device to be reset by connecting a capacitor between this pin and VDD.<br>Asserting RST when the chip is in Idle mode or Power-Down mode returns the chip to normal operation. | – |
| RXD | I/O | **Receive Serial Data**<br>RXD sends and receives data in serial I/O mode 0 and receives data in serial I/O modes 1, 2 and 3. | P3.0 |
| SCL | I/O | **TWI Serial Clock**<br>When TWI controller is in master mode, SCL outputs the serial clock to slave peripherals. When TWI controller is in slave mode, SCL receives clock from the master controller. | P1.6 |
| SCK | I/O | **SPI Serial Clock**<br>When SPI is in master mode, SCK outputs clock to the slave peripheral.<br>When SPI is in slave mode, SCK receives clock from the master controller. | P1.6 |
| SDA | I/O | **TWI Serial Data**<br>SDA is the bidirectional TWI data line. | P1.7 |
| SS# | I | **SPI Slave Select Input**<br>When in Slave mode, SS# enables the slave mode. | P1.4 |

**Table 4.** Serial I/O Port SFRs

| Mnemonic | Name |
|---|---|
| SCON | Serial Control |
| SBUF | Serial Data Buffer |
| SADEN | Slave Address Mask |

| Mnemonic | Name |
|---|---|
| SADDR | Slave Address |
| BRL | Baud Rate Reload |
| BDRCON | Baud Rate Control |

**Table 5.** SSLC SFRs

| Mnemonic | Name |
|---|---|
| SSCON | Synchronous Serial control |
| SSDAT | Synchronous Serial Data |
| SSCS | Synchronous Serial Control and Status |

| Mnemonic | Name |
|---|---|
| SSADR | Synchronous Serial Address |
| SSBR | Synchronous Serial Bit Rate |

**Table 6.** Event Waveform Control SFRs

| Mnemonic | Name |
|---|---|
| CCON | EWC-PCA Timer/Counter Control |
| CMOD | EWC-PCA Timer/Counter Mode |
| CL | EWC-PCA Timer/Counter Low Register |
| CH | EWC-PCA Timer/Counter High Register |
| CCAPM0 | EWC-PCA Timer/Counter Mode 0 |
| CCAPM1 | EWC-PCA Timer/Counter Mode 1 |
| CCAPM2 | EWC-PCA Timer/Counter Mode 2 |
| CCAPM3 | EWC-PCA Timer/Counter Mode 3 |
| CCAPM4 | EWC-PCA Timer/Counter Mode 4 |

| Mnemonic | Name |
|---|---|
| CCAP0L | EWC-PCA Compare Capture Module 0 Low Register |
| CCAP1L | EWC-PCA Compare Capture Module 1 Low Register |
| CCAP2L | EWC-PCA Compare Capture Module 2 Low Register |
| CCAP3L | EWC-PCA Compare Capture Module 3 Low Register |
| CCAP4L | EWC-PCA Compare Capture Module 4 Low Register |
| CCAP0H | EWC-PCA Compare Capture Module 0 High Register |
| CCAP1H | EWC-PCA Compare Capture Module 1 High Register |
| CCAP2H | EWC-PCA Compare Capture Module 2 High Register |
| CCAP3H | EWC-PCA Compare Capture Module 3 High Register |
| CCAP4H | EWC-PCA Compare Capture Module 4 High Register |

**Table 7.** System Management SFRs

| Mnemonic | Name |
|---|---|
| PCON | Power Control |
| POWM | Power Management |

| Mnemonic | Name |
|---|---|
| CKRL | Clock Reload |
| WCON | Synchronous Real-Time Wait State Control |

**Table 8.** Interrupt SFRs

| Mnemonic | Name |
|---|---|
| IE0 | Interrupt Enable Control 0 |
| IE1 | Interrupt Enable Control 1 |
| IPH0 | Interrupt Priority Control High 0 |

| Mnemonic | Name |
|---|---|
| IPL0 | Interrupt Priority Control Low 0 |
| IPH1 | Interrupt Priority Control High 1 |
| IPL1 | Interrupt Priority Control Low 1 |

**Table 9.** Keyboard Interface SFRs

| Mnemonic | Name |
|---|---|
| P1IE | Port 1 Input Interrupt Enable |
| P1F | Port 1 Flag |

| Mnemonic | Name |
|---|---|
| P1LS | Port 1 Level Selection |

**Table 16.** Notation for Immediate Addressing

| Immediate Address | Description | C251 | C51 |
|---|---|---|---|
| #data | An 8-bit constant that is immediately addressed in an instruction | 3 | 3 |
| #data16 | A 16-bit constant that is immediately addressed in an instruction | 3 | – |
| #0data16<br>#1data16 | A 32-bit constant that is immediately addressed in an instruction. The upper word is filled with zeros (#0data16) or ones (#1data16). | 3 | – |
| #short | A constant, equal to 1, 2, or 4, that is immediately addressed in an instruction. | 3 | – |

**Table 17.** Notation for Bit Addressing

| Direct Address | Description | C251 | C51 |
|---|---|---|---|
| bit51 | A directly addressed bit (bit number = 00h-FFh) in memory or an SFR. Bits 00h-7Fh are the 128 bits in byte locations 20h-2Fh in the on-chip RAM. Bits 80h-FFh are the 128 bits in the 16 SFRs with addresses that end in 0h or 8h, S:80h, S:88h, S:90h,..., S:F0h, S:F8h. | – | 3 |
| bit | A directly addressed bit in memory locations 00:0020h-00:007Fh or in any defined SFR. | 3 | |

**Table 18.** Notation for Destination in Control Instructions

| Direct Address | Description | C251 | C51 |
|---|---|---|---|
| rel | A signed (two's complement) 8-bit relative address. The destination is -128 to +127 bytes relative to the next instruction's first byte. | 3 | 3 |
| addr11 | An 11-bit target address. The target is in the same 2-Kbyte block of memory as the next instruction's first byte. | – | 3 |
| addr16 | A 16-bit target address. The target can be anywhere within the same 64-Kbyte region as the next instruction's first byte. | – | 3 |
| addr24 | A 24-bit target address. The target can be anywhere within the 16-Mbyte address space. | 3 | – |

Notes: 1. Logical instructions that affect a bit are in Table 27.
2. A shaded cell denotes an instruction in the C51 Architecture.
3. If this instruction addresses an I/O Port (Px, x = 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.
4. If this instruction addresses an I/O Port (Px, x = 0-3), add 2 to the number of states. Add 3 if it addresses a Peripheral SFR.
5. If this instruction addresses external memory location, add N+2 to the number of states (N: number of wait states).
6. If this instruction addresses external memory location, add 2(N+2) to the number of states (N: number of wait states).

**Table 23.** Summary of Logical Instructions (2/2)

Shift Left LogicalSLL <dest><dest>$_0 \leftarrow 0$
<dest>$_{n+1} \leftarrow$ <dest>$_n$, n = 0..msb-1
(CY) $\leftarrow$ <dest>$_{msb}$
Shift Right ArithmeticSRA <dest><dest>$_{msb} \leftarrow$ <dest>$_{msb}$
<dest>$_{n-1} \leftarrow$ <dest>$_n$, n = msb..1
(CY) $\leftarrow$ <dest>$_0$
Shift Right LogicalSRL <dest><dest>$_{msb} \leftarrow 0$
<dest>$_{n-1} \leftarrow$ <dest>$_n$, n = msb..1
(CY) $\leftarrow$ <dest>$_0$
SwapSWAP $AA_{3:0}$ $A_{7:4}$

| Mnemonic | <dest>, <src>(1) | Comments | Binary Mode | | Source Mode | |
|---|---|---|---|---|---|---|
| | | | Bytes | States | Bytes | States |
| SLL | Rm | Shift byte register left through the MSB | 3 | 2 | 2 | 1 |
| | WRj | Shift word register left through the MSB | 3 | 2 | 2 | 1 |
| SRA | Rm | Shift byte register right | 3 | 2 | 2 | 1 |
| | WRj | Shift word register right | 3 | 2 | 2 | 1 |
| SRL | Rm | Shift byte register left | 3 | 2 | 2 | 1 |
| | WRj | Shift word register left | 3 | 2 | 2 | 1 |
| SWAP | A | Swap nibbles within ACC | 1 | 2 | 1 | 2 |

Note: 1. A shaded cell denotes an instruction in the C51 Architecture.

| | | | | | | |
|---|---|---|---|---|---|---|
| MOV | WRj, at WRj +dis24 | Indirect with 16-bit displacement (16M) to word register | 5 | 8[5] | 4 | 7[5] |
| MOV | at WRj +dis16, Rm | Byte register to indirect with 16-bit displacement (64K) | 5 | 6[4] | 4 | 5[4] |
| MOV | at WRj +dis16, WRj | Word register to indirect with 16-bit displacement (64K) | 5 | 7[5] | 4 | 6[5] |
| MOV | at DRk +dis24, Rm | Byte register to indirect with 16-bit displacement (16M) | 5 | 7[4] | 4 | 6[4] |
| MOV | at DRk +dis24, WRj | Word register to indirect with 16-bit displacement (16M) | 5 | 8[5] | 4 | 7[5] |

Notes:
1. Instructions that move bits are in Table 27.
2. Move instructions unique to the C251 Architecture.
3. If this instruction addresses an I/O Port (Px, x = 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.
4. If this instruction addresses external memory location, add N+2 to the number of states (N: number of wait states).
5. If this instruction addresses external memory location, add 2(N+1) to the number of states (N: number of wait states).
6. If this instruction addresses external memory location, add 4(N+2) to the number of states (N: number of wait states).

**Table 32.** Summary of Call and Return Instructions

Absolute callACALL <src>(PC) ← (PC) +2; push $(PC)_{15:0}$;
$(PC)_{10:0}$ ← src opnd
Extended callECALL <src>(PC) ← (PC) + size (instr); push $(PC)_{23:0}$;
$(PC)_{23:0}$ ← src opnd
Long callLCALL <src>(PC) ← (PC) + size (instr); push $(PC)_{15:0}$;
$(PC)_{15:0}$ ← src opnd
Return from subroutineRETpop $(PC)_{15:0}$
Extended return from subroutineERETpop $(PC)_{23:0}$
Return from interruptRETIIF [INTR = 0] THEN pop $(PC)_{15:0}$
IF [INTR = 1] THEN pop $(PC)_{23:0}$; pop (PSW1)
Trap interruptTRAP(PC) ← (PC) + size (instr);
IF [INTR = 0] THEN push $(PC)_{15:0}$
IF [INTR = 1] THEN push (PSW1); push $(PC)_{23:0}$

| Mnemonic | <dest>, <src>(1) | Comments | Binary Mode | | Source Mode | |
|---|---|---|---|---|---|---|
| | | | Bytes | States | Bytes | States |
| ACALL | addr11 | Absolute subroutine call | 2 | 9(2)(3) | 2 | 9(2)(3) |
| ECALL | at DRk | Extended subroutine call (indirect) | 3 | 14(2)(3) | 2 | 13(2)(3) |
| | addr24 | Extended subroutine call | 5 | 14(2)(3) | 4 | 13(2)(3) |
| LCALL | at WRj | Long subroutine call (indirect) | 3 | 10(2)(3) | 2 | 9(2)(3) |
| | addr16 | Long subroutine call | 3 | 9(2)(3) | 3 | 9(2)(3) |
| RET | | Return from subroutine | 1 | 7(2) | 1 | 7(2) |
| ERET | | Extended subroutine return | 3 | 9(2) | 2 | 8(2) |
| RETI | | Return from interrupt | 1 | 7(2)(4) | 1 | 7(2)(4) |
| TRAP | | Jump to the trap interrupt vector | 2 | 12(4) | 1 | 11(4) |

Notes:
1. A shaded cell denotes an instruction in the C51 Architecture.
2. In internal execution only, add 1 to the number of states if the destination/return address is internal and odd.
3. Add 2 to the number of states if the destination address is external.
4. Add 5 to the number of states if INTR = 1.

- PSEN# and the other control signals have to be released to complete a sequence of programming operations or a sequence of programming and verifying operations.

**Figure 6.** Setup for Programming

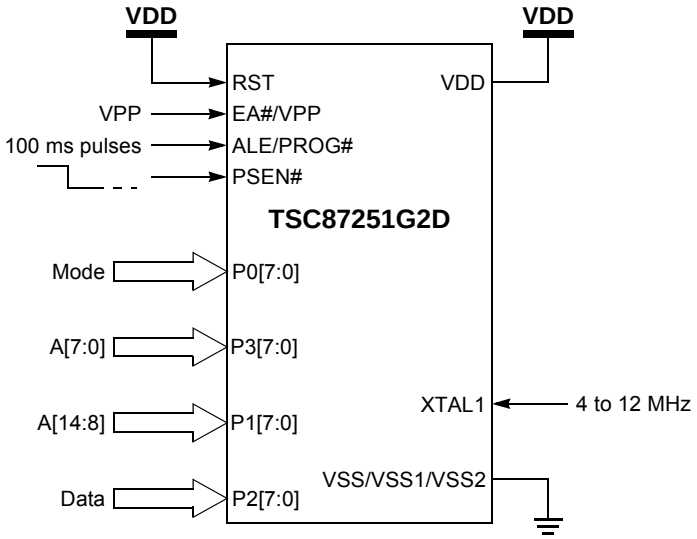



**Table 36.** Programming Modes

| ROM Area[1] | RST | EA#/VPP | PSEN # | ALE/PROG#[2] | P0 | P2 | P1(MSB) P3(LSB) |
|---|---|---|---|---|---|---|---|
| On-chip Code Memory | 1 | $V_{PP}$ | 0 | 1 Pulse | 68h | Data | 16-bit Address 0000h-7FFFh (32 kilobytes) |
| Configuration Bytes | 1 | $V_{PP}$ | 0 | 1 Pulse | 69h | Data | CONFIG0: FFF8h CONFIG1: FFF9h |
| Lock Bits | 1 | $V_{PP}$ | 0 | 1 Pulse | 6Bh | X | LB0: 0001h LB1: 0002h LB2: 0003h |
| Encryption Array | 1 | $V_{PP}$ | 0 | 1 Pulse | 6Ch | Data | 0000h-007Fh |

Notes: 1. Signature Bytes are not user-programmable.
2. The ALE/PROG# pulse waveform is shown in Figure 23 page 59.

## Verify Algorithm

Figure 7 shows the hardware setup needed to verify the TSC87251G2D EPROM/OTPROM or TSC83251G2D ROM areas:

- The chip has to be put under reset and maintained in this state until the completion of the verifying sequence.
- PSEN# and the other control signals (ALE and Port 0) have to be set to a high level.
- Then PSEN# has to be to forced to a low level after two clock cycles or more and it has to be maintained in this state until the completion of the verifying sequence (see below).
- The voltage on the EA# pin must be set to $V_{DD}$ and ALE must be set to a high level.
- The Verifying Mode is selected according to the code applied on Port 0. It has to be applied until the completion of this verifying operation.
- The verifying address is applied on Ports 1 and 3 which are respectively the MSB and the LSB of the address.

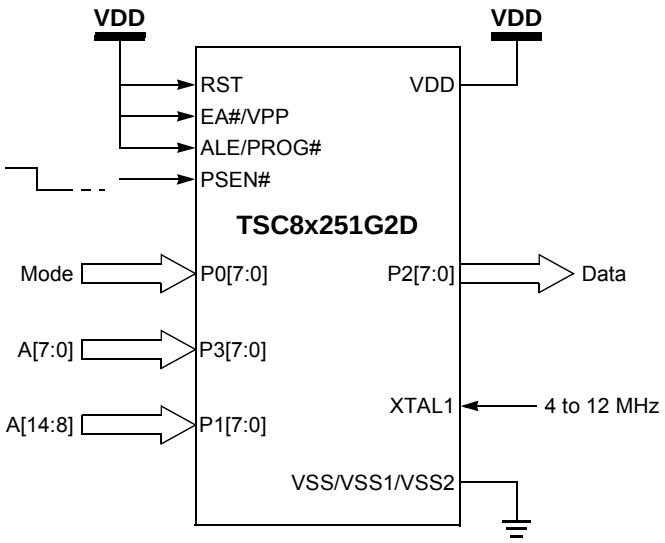
- Then device is driving the data on Port 2.
- It is possible to alternate programming and verification operation (see Paragraph Programming Algorithm). Please make sure the voltage on the EA# pin has actually been lowered to $V_{DD}$ before performing the verifying operation.
- PSEN# and the other control signals have to be released to complete a sequence of verifying operations or a sequence of programming and verifying operations.

**Table 37.** Verifying Modes

| ROM Area[1] | RST | EA#/VPP | PSEN# | ALE/PROG# | P0 | P2 | P1(MSB) P3(LSB) |
|---|---|---|---|---|---|---|---|
| On-chip code memory | 1 | 1 | 0 | 1 | 28h | Data | 16-bit Address 0000h-7FFFh (32 kilobytes) |
| Configuration Bytes | 1 | 1 | 0 | 1 | 29h | Data | CONFIG0: FFF8h CONFIG1: FFF9h |
| Lock Bits | 1 | 1 | 0 | 1 | 2Bh | Data | 0000h |
| Signature Bytes | 1 | 1 | 0 | 1 | 29h | Data | 0030h, 0031h, 0060h, 0061h |

Notes: 1. To preserve the secrecy of on-chip code memory when encrypted, the Encryption Array can not be verified.

**Figure 7.** Setup for Verifying



# AC Characteristics - Commercial & Industrial

## AC Characteristics - External Bus Cycles

### Definition of Symbols

**Table 38.** External Bus Cycles Timing Symbol Definitions

| Signals | |
|---|---|
| A | Address |
| D | Data In |
| L | ALE |
| Q | Data Out |
| R | RD#/PSEN# |
| W | WR# |

| Conditions | |
|---|---|
| H | High |
| L | Low |
| V | Valid |
| X | No Longer Valid |
| Z | Floating |

### Timings

Test conditions: capacitive load on all pins = 50 pF.

Table 39 and Table 40 list the AC timing parameters for the TSC80251G2D derivatives with no wait states. External wait states can be added by extending PSEN#/RD#/WR# and or by extending ALE. In these tables, Note 2 marks parameters affected by one ALE wait state, and Note 3 marks parameters affected by PSEN#/RD#/WR# wait states.

Figure 8 to Figure 13 show the bus cycles with the timing parameters.

**Table 39.** Bus Cycles AC Timings; $V_{DD}$ = 4.5 to 5.5 V, $T_A$ = -40 to 85°C

| Symbol | Parameter | 12 MHz | | 16 MHz | | 24 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $T_{OSC}$ | $1/F_{OSC}$ | 83 | | 62 | | 41 | | ns |
| $T_{LHLL}$ | ALE Pulse Width | 78 | | 58 | | 38 | | ns(2) |
| $T_{AVLL}$ | Address Valid to ALE Low | 78 | | 58 | | 37 | | ns(2) |
| $T_{LLAX}$ | Address hold after ALE Low | 19 | | 11 | | 3 | | ns |
| $T_{RLRH}$(1) | RD#/PSEN# Pulse Width | 162 | | 121 | | 78 | | ns(3) |
| $T_{WLWH}$ | WR# Pulse Width | 165 | | 124 | | 81 | | ns(3) |
| $T_{LLRL}$(1) | ALE Low to RD#/PSEN# Low | 22 | | 14 | | 6 | | ns |
| $T_{LHAX}$ | ALE High to Address Hold | 99 | | 70 | | 40 | | ns(2) |
| $T_{RLDV}$(1) | RD#/PSEN# Low to Valid Data | | 146 | | 104 | | 61 | ns(3) |
| $T_{RHDX}$(1) | Data Hold After RD#/PSEN# High | 0 | | 0 | | 0 | | ns |
| $T_{RHAX}$(1) | Address Hold After RD#/PSEN# High | 0 | | 0 | | 0 | | ns |
| $T_{RLAZ}$(1) | RD#/PSEN# Low to Address Float | | 0 | | 0 | | 0 | ns |
| $T_{RHDZ1}$ | Instruction Float After RD#/PSEN# High | | 45 | | 40 | | 30 | ns |
| $T_{RHDZ2}$ | Data Float After RD#/PSEN# High | | 215 | | 165 | | 115 | ns |
| $T_{RHLH1}$ | RD#/PSEN# high to ALE High (Instruction) | 49 | | 43 | | 31 | | ns |
| $T_{RHLH2}$ | RD#/PSEN# high to ALE High (Data) | 215 | | 169 | | 115 | | ns |
| $T_{WHLH}$ | WR# High to ALE High | 215 | | 169 | | 115 | | ns |
| $T_{AVDV1}$ | Address (P0) Valid to Valid Data In | | 250 | | 175 | | 105 | ns(2)(3) |
| $T_{AVDV2}$ | Address (P2) Valid to Valid Data In | | 306 | | 223 | | 140 | ns(2)(3) |
| $T_{AVDV3}$ | Address (P0) Valid to Valid Instruction In | | 150 | | 109 | | 68 | ns(3) |
| $T_{AXDX}$ | Data Hold after Address Hold | 0 | | 0 | | 0 | | ns |
| $T_{AVRL}$(1) | Address Valid to RD# Low | 100 | | 70 | | 40 | | ns(2) |
| $T_{AVWL1}$ | Address (P0) Valid to WR# Low | 100 | | 70 | | 40 | | ns(2) |
| $T_{AVWL2}$ | Address (P2) Valid to WR# Low | 158 | | 115 | | 74 | | ns(2) |
| $T_{WHQX}$ | Data Hold after WR# High | 90 | | 69 | | 32 | | ns |
| $T_{QVWH}$ | Data Valid to WR# High | 133 | | 102 | | 72 | | ns(3) |
| $T_{WHAX}$ | WR# High to Address Hold | 167 | | 125 | | 84 | | ns |

Notes:
1. Specification for PSEN# are identical to those for RD#.
2. If a wait state is added by extending ALE, add $2 \cdot T_{OSC.}$
3. If wait states are added by extending RD#/PSEN#/WR#, add $2N \cdot T_{OSC}$ (N = 1..3).

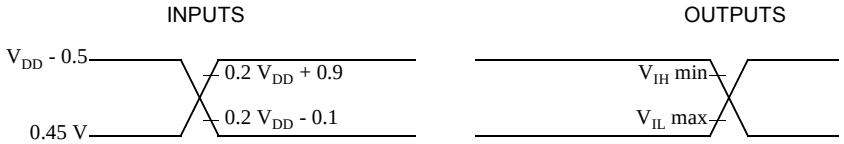
**Timings**

**Table 49.** SPI Interface AC Timing; $V_{DD}$ = 2.7 to 5.5 V, $T_A$ = -40 to 85°C

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| **Slave Mode(1)** | | | | |
| $T_{CHCH}$ | Clock Period | 8 | | $T_{OSC}$ |
| $T_{CHCX}$ | Clock High Time | 3.2 | | $T_{OSC}$ |
| $T_{CLCX}$ | Clock Low Time | 3.2 | | $T_{OSC}$ |
| $T_{SLCH}$, $T_{SLCL}$ | SS# Low to Clock edge | 200 | | ns |
| $T_{IVCL}$, $T_{IVCH}$ | Input Data Valid to Clock Edge | 100 | | ns |
| $T_{CLIX}$, $T_{CHIX}$ | Input Data Hold after Clock Edge | 100 | | ns |
| $T_{CLOV,}$ $T_{CHOV}$ | Output Data Valid after Clock Edge | | 100 | ns |
| $T_{CLOX}$, $T_{CHOX}$ | Output Data Hold Time after Clock Edge | 0 | | ns |
| $T_{CLSH}$, $T_{CHSH}$ | SS# High after Clock Edge | 0 | | ns |
| $T_{IVCL}$, $T_{IVCH}$ | Input Data Valid to Clock Edge | 100 | | ns |
| $T_{CLIX}$, $T_{CHIX}$ | Input Data Hold after Clock Edge | 100 | | ns |
| $T_{SLOV}$ | SS# Low to Output Data Valid | | 130 | ns |
| $T_{SHOX}$ | Output Data Hold after SS# High | | 130 | ns |
| $T_{SHSL}$ | SS# High to SS# Low | (2) | | |
| $T_{ILIH}$ | Input Rise Time | | 2 | µs |
| $T_{IHIL}$ | Input Fall Time | | 2 | µs |
| $T_{OLOH}$ | Output Rise time | | 100 | ns |
| $T_{OHOL}$ | Output Fall Time | | 100 | ns |
| **Master Mode(3)** | | | | |
| $T_{CHCH}$ | Clock Period | 4 | | $T_{OSC}$ |
| $T_{CHCX}$ | Clock High Time | 1.6 | | $T_{OSC}$ |
| $T_{CLCX}$ | Clock Low Time | 1.6 | | $T_{OSC}$ |
| $T_{IVCL}$, $T_{IVCH}$ | Input Data Valid to Clock Edge | 50 | | ns |
| $T_{CLIX}$, $T_{CHIX}$ | Input Data Hold after Clock Edge | 50 | | ns |
| $T_{CLOV,}$ $T_{CHOV}$ | Output Data Valid after Clock Edge | | 65 | ns |
| $T_{CLOX}$, $T_{CHOX}$ | Output Data Hold Time after Clock Edge | 0 | | ns |
| $T_{ILIH}$ | Input Data Rise Time | | 2 | µs |
| $T_{IHIL}$ | Input Data Fall Time | | 2 | µs |
| $T_{OLOH}$ | Output Data Rise time | | 50 | ns |
| $T_{OHOL}$ | Output Data Fall Time | | 50 | ns |

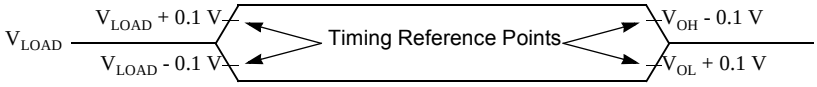
Notes: 1. Capacitive load on all pins = 200 pF in slave mode.
2. The value of this parameter depends on software.
3. Capacitive load on all pins = 100 pF in master mode.

**Figure 26.** AC Testing Input/Output Waveforms




Note: For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loading $V_{OH}/V_{OL}$ level occurs with $I_{OL}/I_{OH}$ = ±20 mA.

**Figure 27.** Float Waveforms



Notes: 1. Under steady-state (non-transient) conditions, $I_{OL}$ must be externally limited as follows:

Maximum IOL per port pin: 10 mA

Maximum IOL per 8-bit port:Port 0 26 mA

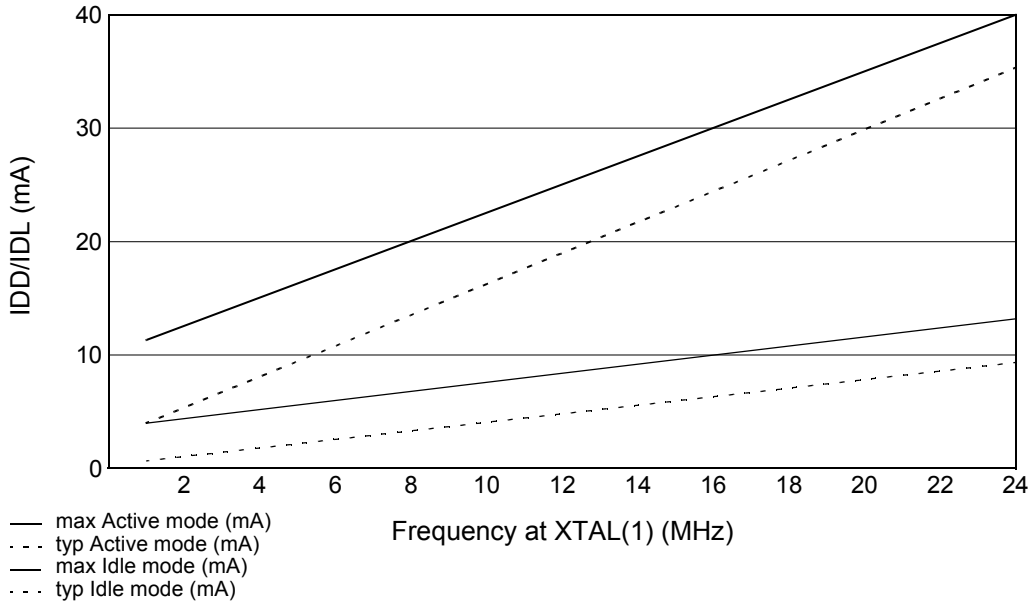
Ports 1-3 15 mA

Maximum Total IOL for all: Output Pins 71 mA

If IOL exceeds the test conditions, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

2. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses above 0.4 V on the low-level outputs of ALE and Ports 1, 2, and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from high to low. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8 V. It may be desirable to qualify ALE or other signals with a Schmitt Trigger or CMOS-level input logic.
3. Capacitive loading on Ports 0 and 2 causes the $V_{OH}$ on ALE and PSEN# to drop below the specification when the address lines are stabilizing.
4. Typical values are obtained using $V_{DD}$ = 5 V and $T_A$ = 25°C. They are not tested and there is not guarantee on these values.
5. The input threshold voltage of SCL and SDA meets the TWI specification, so an input voltage below $0.3 \cdot V_{DD}$ will be recognized as a logic 0 while an input voltage above $0.7 \cdot V_{DD}$ will be recognized as a logic 1.

**Figure 28.** $I_{DD}/I_{DL}$ Versus Frequency; $V_{DD}$ = 4.5 to 5.5 V




Note: 1. The clock prescaler is not used: $F_{OSC} = F_{XTAL}$.

**Figure 31.** $I_{DL}$ Test Condition, Idle Mode

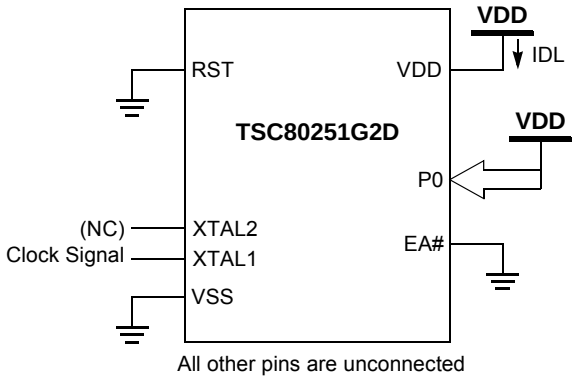
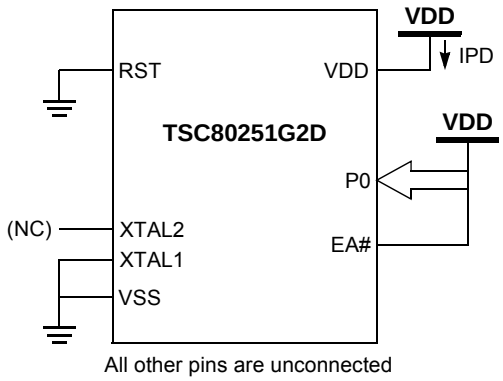



**Figure 32.** $I_{PD}$ Test Condition, Power-Down Mode



# Packages

## List of Packages

- PDIL 40
- CDIL 40 with window
- PLCC 44
- CQPJ 44 with window
- VQFP 44 (10x10)

## PDIL 40 - Mechanical Outline

**Figure 33.** Plastic Dual In Line

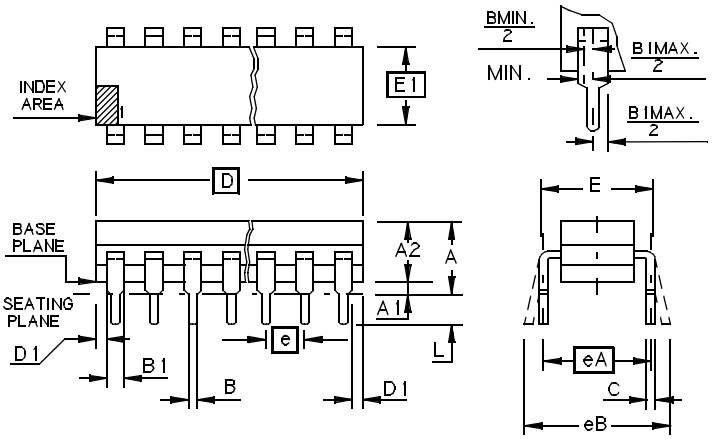



**Table 57.** PDIL Package Size

| | MM | | Inch | |
|---|---|---|---|---|
| | **Min** | **Max** | **Min** | **Max** |
| A | - | 5.08 | - | .200 |
| A1 | 0.38 | - | .015 | - |
| A2 | 3.18 | 4.95 | .125 | .195 |
| B | 0.36 | 0.56 | .014 | .022 |
| B1 | 0.76 | 1.78 | .030 | .070 |
| C | 0.20 | 0.38 | .008 | .015 |
| D | 50.29 | 53.21 | 1.980 | 2.095 |
| E | 15.24 | 15.87 | .600 | .625 |
| E1 | 12.32 | 14.73 | .485 | .580 |
| e | 2.54 B.S.C. | | .100 B.S.C. | |
| eA | 15.24 B.S.C. | | .600 B.S.C. | |
| eB | - | 17.78 | - | .700 |
| L | 2.93 | 3.81 | .115 | .150 |
| D1 | 0.13 | - | .005 | - |

## CQPJ 44 with Window - Mechanical Outline

**Figure 36.** Ceramic Quad Pack J

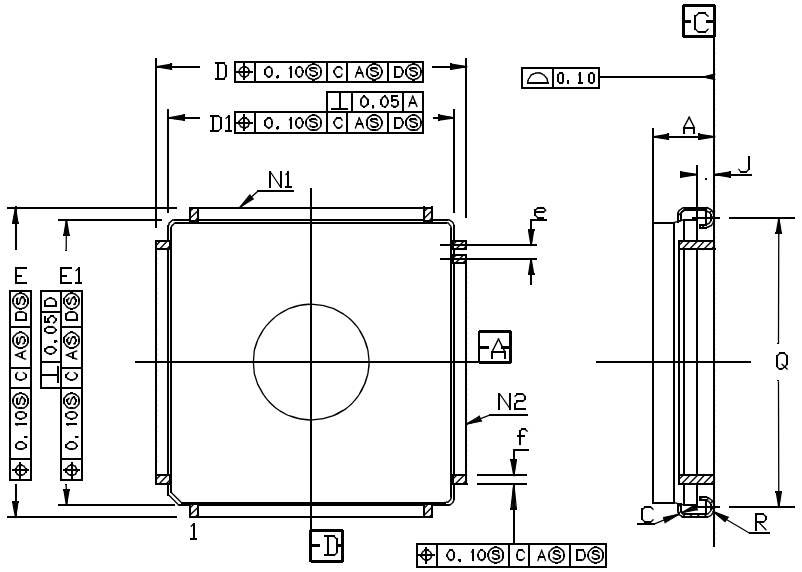



**Table 60.** CQPJ Package Size

| | MM | | Inch | |
|---|---|---|---|---|
| | **Min** | **Max** | **Min** | **Max** |
| A | - | 4.90 | - | .193 |
| C | 0.15 | 0.25 | .006 | .010 |
| D - E | 17.40 | 17.55 | .685 | .691 |
| D1 - E1 | 16.36 | 16.66 | .644 | .656 |
| e | 1.27 TYP | | .050 TYP | |
| f | 0.43 | 0.53 | .017 | .021 |
| J | 0.86 | 1.12 | .034 | .044 |
| Q | 15.49 | 16.00 | .610 | .630 |
| R | 0.86 TYP | | .034 TYP | |
| N1 | 11 | | 11 | |
| N2 | 11 | | 11 | |

| Part Number[1] | ROM | Description |
|---|---|---|
| **Low Voltage Versions 2.7 to 5.5 V** | | |
| TSC251G2Dxxx-L16CB | 32K MaskROM | 16 MHz, Commercial 0° to 70°C, PLCC 44 |
| TSC251G2Dxxx-L16CE | 32K MaskROM | 16 MHz, Commercial 0° to 70°C, VQFP 44 |
| AT251G2Dxxx-SLSUL | 32K MaskROM | 16 MHz, Industrial & Green, PLCC 44 |
| AT251G2Dxxx-RLTUL | 32K MaskROM | 16 MHz, Industrial & Green, VQFP 44 |

Note: 1. xxx: means ROM code, is Cxxx in case of encrypted code.