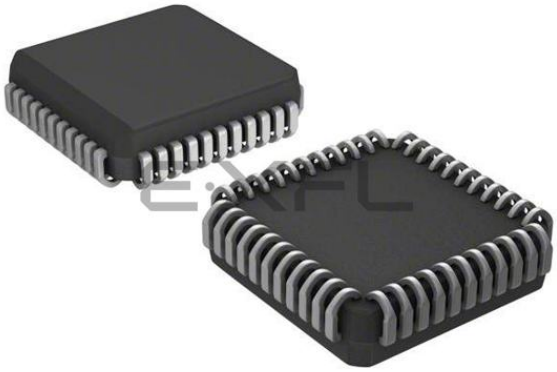

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | C251 |
| Core Size | 8/16-Bit |
| Speed | 16MHz |
| Connectivity | EBI/EMI, I²C, Microwire, SPI, UART/USART |
| Peripherals | POR, PWM, WDT |
| Number of I/O | 32 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-LCC (J-Lead) |
| Supplier Device Package | 44-PLCC (16.6x16.6) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/tsc87251g2d-16cbr |

# Pin Description

## Pinout

**Figure 1.** TSC80251G2D 40-pin DIP package

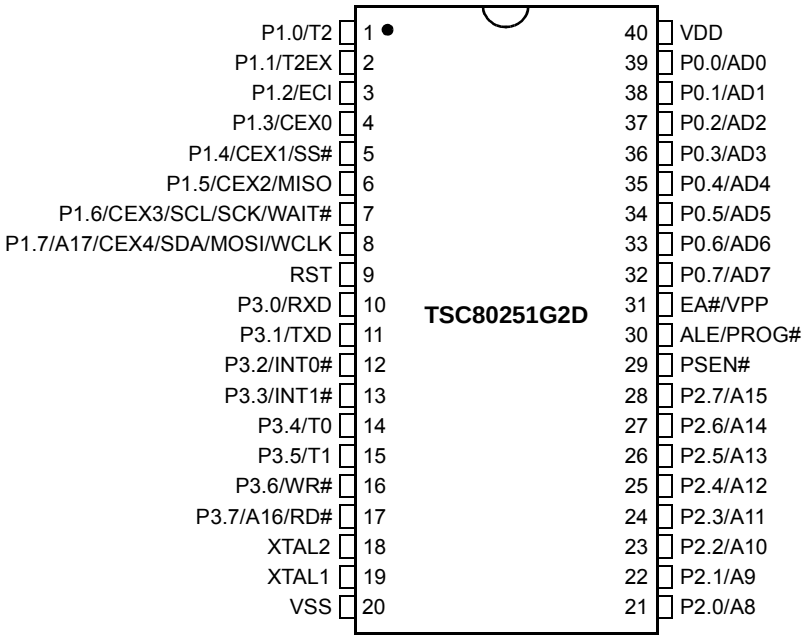



**Figure 2.** TSC80251G2D 44-pin PLCC Package

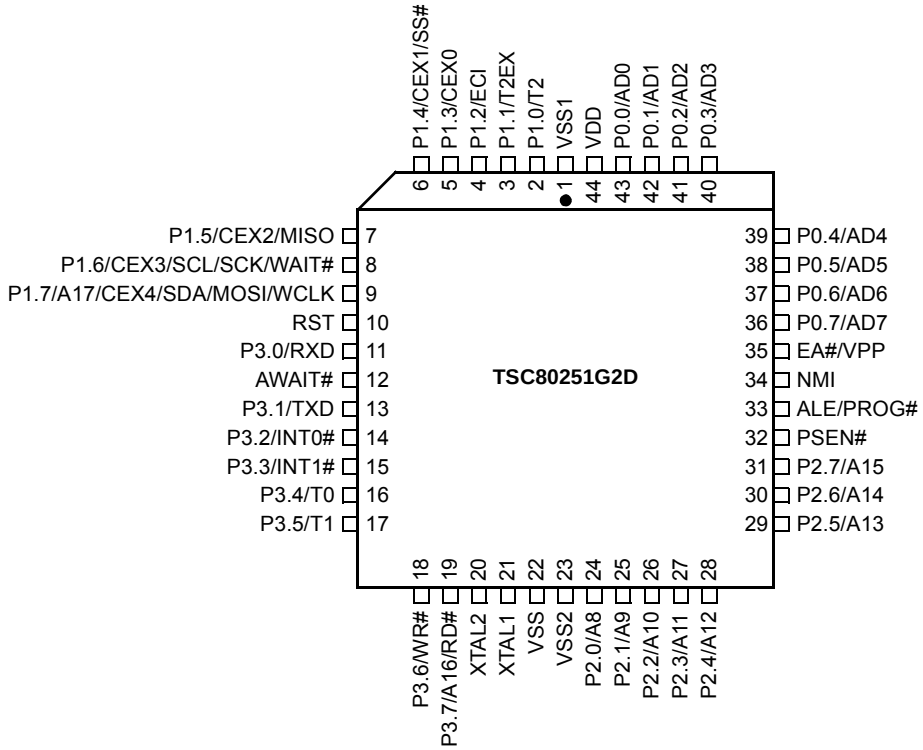


**Table 1.** TSC80251G2D Pin Assignment

| DIP | PLCC | VQFP | Name | DIP | PLCC | VQFP | Name |
|---|---|---|---|---|---|---|---|
| | 1 | 39 | VSS1 | | 23 | 17 | VSS2 |
| 1 | 2 | 40 | P1.0/T2 | 21 | 24 | 18 | P2.0/A8 |
| 2 | 3 | 41 | P1.1/T2EX | 22 | 25 | 19 | P2.1/A9 |
| 3 | 4 | 42 | P1.2/ECI | 23 | 26 | 20 | P2.2/A10 |
| 4 | 5 | 43 | P1.3/CEX0 | 24 | 27 | 21 | P2.3/A11 |
| 5 | 6 | 44 | P1.4/CEX1/SS# | 25 | 28 | 22 | P2.4/A12 |
| 6 | 7 | 1 | P1.5/CEX2/MISO | 26 | 29 | 23 | P2.5/A13 |
| 7 | 8 | 2 | P1.6/CEX3/SCL/SCK/WAIT# | 27 | 30 | 24 | P2.6/A14 |
| 8 | 9 | 3 | P1.7/A17/CEX4/SDA/MOSI/WCLK | 28 | 31 | 25 | P2.7/A15 |
| 9 | 10 | 4 | RST | 29 | 32 | 26 | PSEN# |
| 10 | 11 | 5 | P3.0/RXD | 30 | 33 | 27 | ALE/PROG# |
| | 12 | 6 | AWAIT# | | 34 | 28 | NMI |
| 11 | 13 | 7 | P3.1/TXD | 31 | 35 | 29 | EA#/VPP |
| 12 | 14 | 8 | P3.2/INT0# | 32 | 36 | 30 | P0.7/AD7 |
| 13 | 15 | 9 | P3.3/INT1# | 33 | 37 | 31 | P0.6/AD6 |
| 14 | 16 | 10 | P3.4/T0 | 34 | 38 | 32 | P0.5/AD5 |
| 15 | 17 | 11 | P3.5/T1 | 35 | 39 | 33 | P0.4/AD4 |
| 16 | 18 | 12 | P3.6/WR# | 36 | 40 | 34 | P0.3/AD3 |
| 17 | 19 | 13 | P3.7/A16/RD# | 37 | 41 | 35 | P0.2/AD2 |
| 18 | 20 | 14 | XTAL2 | 38 | 42 | 36 | P0.1/AD1 |
| 19 | 21 | 15 | XTAL1 | 39 | 43 | 37 | P0.0/AD0 |
| 20 | 22 | 16 | VSS | 40 | 44 | 38 | VDD |

**Table 7.** System Management SFRs

| Mnemonic | Name |
|---|---|
| PCON | Power Control |
| POWM | Power Management |

| Mnemonic | Name |
|---|---|
| CKRL | Clock Reload |
| WCON | Synchronous Real-Time Wait State Control |

**Table 8.** Interrupt SFRs

| Mnemonic | Name |
|---|---|
| IE0 | Interrupt Enable Control 0 |
| IE1 | Interrupt Enable Control 1 |
| IPH0 | Interrupt Priority Control High 0 |

| Mnemonic | Name |
|---|---|
| IPL0 | Interrupt Priority Control Low 0 |
| IPH1 | Interrupt Priority Control High 1 |
| IPL1 | Interrupt Priority Control Low 1 |

**Table 9.** Keyboard Interface SFRs

| Mnemonic | Name |
|---|---|
| P1IE | Port 1 Input Interrupt Enable |
| P1F | Port 1 Flag |

| Mnemonic | Name |
|---|---|
| P1LS | Port 1 Level Selection |

**Table 12.** Configuration Byte 1
UCONFIG1

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **CSIZE** | **-** | **-** | **INTR** | **WSB** | **WSB1#** | **WSB0#** | **EMAP#** |

| Bit Number | Bit Mnemonic | Description |
|---|---|---|
| 7 | CSIZE<br>TSC87251G2D | **On-Chip Code Memory Size bit**(1)<br>Clear to select 16 KB of on-chip code memory (TSC87251G1D product).<br>Set to select 32 KB of on-chip code memory (TSC87251G2D product). |
| | TSC80251G2D<br>TSC83251G2D | **Reserved**<br>Set this bit when writing to UCONFIG1. |
| 6 | - | **Reserved**<br>Set this bit when writing to UCONFIG1. |
| 5 | - | **Reserved**<br>Set this bit when writing to UCONFIG1. |
| 4 | INTR | **Interrupt Mode bit**(2)<br>Clear so that the interrupts push two bytes onto the stack (the two lower bytes of the PC register).<br>Set so that the interrupts push four bytes onto the stack (the three bytes of the PC register and the PSW1 register). |
| 3 | WSB | **Wait State B bit**(3)<br>Clear to generate one wait state for memory region 01:.<br>Set for no wait states for memory region 01:. |
| 2 | WSB1# | **Wait State B bits**<br>Select the number of wait states for RD#, WR# and PSEN# signals for external memory accesses (only region 01:).<br>WSB1# WSB0# Number of Wait States<br>0 0 3<br>0 1 2<br>1 0 1<br>1 1 0 |
| 1 | WSB0# | |
| 0 | EMAP# | **On-Chip Code Memory Map bit**<br>Clear to map the upper 16 KB of on-chip code memory (at FF:4000h-FF:7FFFh) to the data space (at 00:C000h-00:FFFFh).<br>Set not to map the upper 16 KB of on-chip code memory (at FF:4000h-FF:7FFFh) to the data space. |

Notes:
1. The CSIZE is only available on EPROM/OTPROM products.
2. Two or four bytes are transparently popped according to INTR when using the RETI instruction. INTR must be set if interrupts are used with code executing outside region FF:.
3. Use only for Step A compatibility; set this bit when WSB1:0# are used.

**Table 25.** Summary of Move Instructions (1/3)

| | | | | | | |
|---|---|---|---|---|---|---|
| Move to High wordMOVH <dest>, <src>dest $opnd_{31:16}$ ← src opnd<br>Move with Sign extensionMOVS <dest>, <src>dest opnd ← src opnd with sign extend<br>Move with Zero extensionMOVZ <dest>, <src>dest opnd ← src opnd with zero extend<br>Move CodeMOVC A, <src>(A) ← src opnd<br>Move eXtendedMOVX <dest>, <src>dest opnd ← src opnd | | | | | | |
| **Mnemonic** | **<dest>, <src>(2)** | **Comments** | **Binary Mode** | | **Source Mode** | |
| | | | **Bytes** | **States** | **Bytes** | **States** |
| MOVH | DRk, #data16 | 16-bit immediate data into upper word of dword register | 5 | 3 | 4 | 2 |
| MOVS | WRj, Rm | Byte register to word register with sign extension | 3 | 2 | 2 | 1 |
| MOVZ | WRj, Rm | Byte register to word register with zeros extension | 3 | 2 | 2 | 1 |
| MOVC | A, at A +DPTR | Code byte relative to DPTR to ACC | 1 | 6(3) | 1 | 6(3) |
| | A, at A +PC | Code byte relative to PC to ACC | 1 | 6(3) | 1 | 6(3) |
| MOVX | A, at Ri | Extended memory (8-bit address) to ACC(2) | 1 | 4 | 1 | 5 |
| | A, at DPTR | Extended memory (16-bit address) to ACC(2) | 1 | 3(4) | 1 | 3(4) |
| | at Ri, A | ACC to extended memory (8-bit address)(2) | 1 | 4 | 1 | 4 |
| | at DPTR, A | ACC to extended memory (16-bit address)(2) | 1 | 4(3) | 1 | 4(3) |

Notes:
1. A shaded cell denotes an instruction in the C51 Architecture.
2. Extended memory addressed is in the region specified by DPXL (reset value = 01h).
3. If this instruction addresses external memory location, add N+1 to the number of states (N: number of wait states).
4. If this instruction addresses external memory location, add N+2 to the number of states (N: number of wait states).

**Table 27.** Summary of Bit Instructions

| | | | | | | |
|---|---|---|---|---|---|---|
| Clear BitCLR <dest>dest opnd ← 0 | | | | | | |
| Set BitSETB <dest>dest opnd ← 1 | | | | | | |
| Complement BitCPL <dest>dest opnd ← ∅ bit | | | | | | |
| AND Carry with BitANL CY, <src>(CY) ← (CY) ∧ src opnd | | | | | | |
| AND Carry with Complement of BitANL CY, /<src>(CY) ← (CY) ∧ ∅ src opnd | | | | | | |
| OR Carry with BitORL CY, <src>(CY) ← (CY) ∨ src opnd | | | | | | |
| OR Carry with Complement of BitORL CY, /<src>(CY) ← (CY) ∨ ∅ src opnd | | | | | | |
| Move Bit to CarryMOV CY, <src>(CY) ← src opnd | | | | | | |
| Move Bit from CarryMOV <dest>, CYdest opnd ← (CY) | | | | | | |
| **Mnemonic** | **<dest>, <src>(1)** | **Comments** | **Binary Mode** | | **Source Mode** | |
| | | | **Bytes** | **States** | **Bytes** | **States** |
| CLR | CY | Clear carry | 1 | 1 | 1 | 1 |
| | bit51 | Clear direct bit | 2 | 2(3) | 2 | 2(3) |
| | bit | Clear direct bit | 4 | 4(3) | 3 | 3(3) |
| SETB | CY | Set carry | 1 | 1 | 1 | 1 |
| | bit51 | Set direct bit | 2 | 2(3) | 2 | 2(3) |
| | bit | Set direct bit | 4 | 4(3) | 3 | 3(3) |
| CPL | CY | Complement carry | 1 | 1 | 1 | 1 |
| | bit51 | Complement direct bit | 2 | 2(3) | 2 | 2(3) |
| | bit | Complement direct bit | 4 | 4(3) | 3 | 3(3) |
| ANL | CY, bit51 | And direct bit to carry | 2 | 1(2) | 2 | 1(2) |
| | CY, bit | And direct bit to carry | 4 | 3(2) | 3 | 2(2) |
| | CY, /bit51 | And complemented direct bit to carry | 2 | 1(2) | 2 | 1(2) |
| | CY, /bit | And complemented direct bit to carry | 4 | 3(2) | 3 | 2(2) |
| ORL | CY, bit51 | Or direct bit to carry | 2 | 1(2) | 2 | 1(2) |
| | CY, bit | Or direct bit to carry | 4 | 3(2) | 3 | 2(2) |
| | CY, /bit51 | Or complemented direct bit to carry | 2 | 1(2) | 2 | 1(2) |
| | CY, /bit | Or complemented direct bit to carry | 4 | 3(2) | 3 | 2(2) |
| MOV | CY, bit51 | Move direct bit to carry | 2 | 1(2) | 2 | 1(2) |
| | CY, bit | Move direct bit to carry | 4 | 3(2) | 3 | 2(2) |
| | bit51, CY | Move carry to direct bit | 2 | 2(3) | 2 | 2(3) |
| | bit, CY | Move carry to direct bit | 4 | 4(3) | 3 | 3(3) |

Notes:
1. A shaded cell denotes an instruction in the C51 Architecture.
2. If this instruction addresses an I/O Port (Px, x = 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.
3. If this instruction addresses an I/O Port (Px, x = 0-3), add 2 to the number of states. Add 3 if it addresses a Peripheral SFR.

**Table 30.** Summary of Conditional Jump Instructions (2/2)

Jump if bitJB <src>, rel(PC) ← (PC) + size (instr);
IF [src opnd = 1] THEN (PC) ← (PC) + rel

Jump if not bitJNB <src>, rel(PC) ← (PC) + size (instr);
IF [src opnd = 0] THEN (PC) ← (PC) + rel

Jump if bit and clearJBC <dest>, rel(PC) ← (PC) + size (instr);
IF [dest opnd = 1] THEN
dest opnd ← 0
(PC) ← (PC) + rel

Jump if accumulator is zeroJZ rel(PC) ← (PC) + size (instr);
IF [(A) = 0] THEN (PC) ← (PC) + rel

Jump if accumulator is not zeroJNZ rel(PC) ← (PC) + size (instr);
IF [(A) ≠ 0] THEN (PC) ← (PC) + rel

Compare and jump if not equalCJNE <src1>, <src2>, rel(PC) ← (PC) + size (instr);
IF [src opnd1 < src opnd2] THEN (CY) ← 1
IF [src opnd1 ≥ src opnd2] THEN (CY) ← 0
IF [src opnd1 ≠ src opnd2] THEN (PC) ← (PC) + rel

Decrement and jump if not zeroDJNZ <dest>, rel(PC) ← (PC) + size (instr); dest opnd ← dest opnd -1;
IF [φ (Z)] THEN (PC) ← (PC) + rel

| Mnemonic | <dest>, <src>[1] | Comments | Binary Mode[2] | | Source Mode[2] | |
|---|---|---|---|---|---|---|
| | | | Bytes | States | Bytes | States |
| JB | bit51, rel | Jump if direct bit is set | 3 | 2/5[3][6] | 3 | 2/5[3][6] |
| | bit, rel | Jump if direct bit of 8-bit address location is set | 5 | 4/7[3][6] | 4 | 3/6[3][6] |
| JNB | bit51, rel | Jump if direct bit is not set | 3 | 2/5[3][6] | 3 | 2/5[3][6] |
| | bit, rel | Jump if direct bit of 8-bit address location is not set | 5 | 4/7[3][6] | 4 | 3/6[3] |
| JBC | bit51, rel | Jump if direct bit is set & clear bit | 3 | 4/7[5][6] | 3 | 4/7[5][6] |
| | bit, rel | Jump if direct bit of 8-bit address location is set and clear | 5 | 7/10[5][6] | 4 | 6/9[5][6] |
| JZ | rel | Jump if ACC is zero | 2 | 2/5[6] | 2 | 2/5[6] |
| JNZ | rel | Jump if ACC is not zero | 2 | 2/5[6] | 2 | 2/5[6] |
| CJNE | A, dir8, rel | Compare direct address to ACC and jump if not equal | 3 | 2/5[3][6] | 3 | 2/5[3][6] |
| | A, #data, rel | Compare immediate to ACC and jump if not equal | 3 | 2/5[6] | 3 | 2/5[6] |
| | Rn, #data, rel | Compare immediate to register and jump if not equal | 3 | 2/5[6] | 4 | 3/6[6] |
| | at Ri, #data, rel | Compare immediate to indirect and jump if not equal | 3 | 3/6[6] | 4 | 4/7[6] |
| DJNZ | Rn, rel | Decrement register and jump if not zero | 2 | 2/5[6] | 3 | 3/6[6] |
| | dir8, rel | Decrement direct address and jump if not zero | 3 | 3/6[4][6] | 3 | 3/6[4][6] |

Notes:
1. A shaded cell denotes an instruction in the C51 Architecture.
2. States are given as jump not-taken/taken.
3. If this instruction addresses an I/O Port (Px, x = 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.
4. If this instruction addresses an I/O Port (Px, x = 0-3), add 2 to the number of states.

Add 3 if it addresses a Peripheral SFR.

5. If this instruction addresses an I/O Port (Px, x = 0-3), add 3 to the number of states. Add 5 if it addresses a Peripheral SFR.
6. In internal execution only, add 1 to the number of states of the 'jump taken' if the destination address is internal and odd.

**Table 31.** Summary of Unconditional Jump Instructions

| | | | | | | |
|---|---|---|---|---|---|---|
| Absolute jumpAJMP <src>(PC) ← (PC) +2; $(PC)_{10:0}$ ← src opnd | | | | | | |
| Extended jumpEJMP <src>(PC) ← (PC) + size (instr); $(PC)_{23:0}$ ← src opnd | | | | | | |
| Long jumpLJMP <src>(PC) ← (PC) + size (instr); $(PC)_{15:0}$ ← src opnd | | | | | | |
| Short jumpSJMP rel(PC) ← (PC) +2; (PC) ← (PC) +rel | | | | | | |
| Jump indirectJMP at A +DPTR$(PC)_{23:16}$ ← FFh; $(PC)_{15:0}$ ← (A) + (DPTR) | | | | | | |
| No operationNOP(PC) ← (PC) +1 | | | | | | |
| **Mnemonic** | **<dest>, <src>(1)** | **Comments** | **Binary Mode** | | **Source Mode** | |
| | | | **Bytes** | **States** | **Bytes** | **States** |
| AJMP | addr11 | Absolute jump | 2 | 3(2)(3) | 2 | 3(2)(3) |
| EJMP | addr24 | Extended jump | 5 | 6(2)(4) | 4 | 5(2)(4) |
| | at DRk | Extended jump (indirect) | 3 | 7(2)(4) | 2 | 6(2)(4) |
| LJMP | at WRj | Long jump (indirect) | 3 | 6(2)(4) | 2 | 5(2)(4) |
| | addr16 | Long jump (direct address) | 3 | 5(2)(4) | 3 | 5(2)(4) |
| SJMP | rel | Short jump (relative address) | 2 | 4(2)(4) | 2 | 4(2)(4) |
| JMP | at A +DPTR | Jump indirect relative to the DPTR | 1 | 5(2)(4) | 1 | 5(2)(4) |
| NOP | | No operation (Jump never) | 1 | 1 | 1 | 1 |

Notes:
1. A shaded cell denotes an instruction in the C51 Architecture.
2. In internal execution only, add 1 to the number of states if the destination address is internal and odd.
3. Add 2 to the number of states if the destination address is external.
4. Add 3 to the number of states if the destination address is external.

# Programming and Verifying Non-volatile Memory

## Internal Features

The internal non-volatile memory of the TSC80251G2D derivatives contains five different areas:

- Code Memory
- Configuration Bytes
- Lock Bits
- Encryption Array
- Signature Bytes

### EPROM/OTPROM Devices

All the internal non-volatile memory but the Signature Bytes of the TSC87251G2D products is made of EPROM cells. The Signature Bytes of the TSC87251G2D products are made of Mask ROM.

The TSC87251G2D products are programmed and verified in the same manner as Atmel's TSC87251G1A, using a SINGLE-PULSE algorithm, which programs at $V_{PP}$ = 12.75V using only one 100µs pulse per byte. This results in a programming time of less than 10 seconds for the 32 kilobytes on-chip code memory.

The EPROM of the TSC87251G2D products in Window package is erasable by Ultra-Violet radiation(1) (UV). UV erasure set all the EPROM memory cells to one and allows reprogramming. The quartz window must be covered with an opaque label(2) when the device is in operation. This is not so much to protect the EPROM array from inadvertent erasure, as to protect the RAM and other on-chip logic. Allowing light to impinge on the silicon die during device operation may cause a logical malfunction.

The TSC87251G2D products in plastic packages are One Time Programmable (OTP). An EPROM cell cannot be reset by UV once programmed to zero.

Notes:
1. The recommended erasure procedure is exposure to ultra-violet light (at 2537 Å) to an integrated dose of at least 20 W-sec/cm$^2$. Exposing the EPROM to an ultra-violet lamp of 12000 µW/cm$^2$ rating for 30 minutes should be sufficient.
2. Erasure of the EPROM begins to occur when the chip is exposed to light wavelength shorter than 4000 Å. Since sunlight and fluorescent light have wavelength in this range, exposure to these light sources over an extended time (1 week in sunlight or 3 years in room-level fluorescent lighting) could cause inadvertent erasure.

### Mask ROM Devices

All the internal non-volatile memory of TSC83251G2D products is made of Mask ROM cells. They can only be verified by the user, using the same algorithm as the EPROM/OTPROM devices.

### ROMless Devices

The TSC80251G2D products do not include on-chip Configuration Bytes, Code Memory and Encryption Array. They only include Signature Bytes made of Mask ROM cells which can be read using the same algorithm as the EPROM/OTPROM devices.

## Security Features

In some microcontroller applications, it is desirable that the user's program code be secured from unauthorized access. The TSC83251G2D and TSC87251G2D offer two kinds of protection for program code stored in the on-chip array:

- Program code in the on-chip Code Memory is encrypted when read out for verification if the Encryption Array isprogrammed.
- A three-level lock bit system restricts external access to the on-chip code memory.

## Lock Bit System

The TSC87251G2D products implement 3 levels of security for User's program as described in Table 33. The TSC83251G2D products implement only the first level of security.

Level 0 is the level of an erased part and does not enable any security features.

Level 1 locks the programming of the User's internal Code Memory, the Configuration Bytes and the Encryption Array.

Level 2 locks the verifying of the User's internal Code Memory. It is always possible to verify the Configuration Bytes and the Lock Bits. It is not possible to verify the Encryption Array.

Level 3 locks the external execution.

**Table 33.** Lock Bits Programming

| Level | Lock bits LB[2:0] | Internal Execution | External Execution | Verification | Programming | External PROM read (MOVC) |
|---|---|---|---|---|---|---|
| 0 | 000 | Enable | Enable | Enable(1) | Enable | Enable(2) |
| 1 | 001 | Enable | Enable | Enable(1) | Disable | Disable |
| 2 | 01x(3) | Enable | Enable | Disable | Disable | Disable |
| 3 | 1xx(3) | Enable | Disable | Disable | Disable | Disable |

Notes: 1. Returns encrypted data if Encryption Array is programmed.
2. Returns non encrypted data.
3. x means don't care. Level 2 always enables level 1, and level 3 always enables levels 1 and 2.

The security level may be verified according to Table 34.

**Table 34.** Lock Bits Verifying

| Level | Lock bits Data(1) |
|---|---|
| 0 | xxxxx000 |
| 1 | xxxxx001 |
| 2 | xxxxx01x |
| 3 | xxxxx1xx |

Note: 1. x means don't care.

## Encryption Array

The TSC83251G2D and TSC87251G2D products include a 128-byte Encryption Array located in non-volatile memory outside the memory address space. During verification of the on-chip code memory, the seven low-order address bits also address the Encryption Array. As the byte of the code memory is read, it is exclusive-NOR'ed (XNOR) with the key byte from the Encryption Array. If the Encryption Array is not programmed (still all 1s), the user program code is placed on the data bus in its original, unencrypted form. If the Encryption Array is programmed with key bytes, the user program code is encrypted and cannot be used without knowledge of the key byte sequence.

To preserve the secrecy of the encryption key byte sequence, the Encryption Array can not be verified.

Notes:
1. When a MOVC instruction is executed, the content of the ROM is not encrypted. In order to fully protect the user program code, the lock bit level 1 (see Table 33) must always be set when encryption is used.
2. If the encryption feature is implemented, the portion of the on-chip code memory that does not contain program code should be filled with “random” byte values to prevent the encryption key sequence from being revealed.

## Signature Bytes

The TSC80251G2D derivatives contain factory-programmed Signature Bytes. These bytes are located in non-volatile memory outside the memory address space at 30h, 31h, 60h and 61h. To read the Signature Bytes, perform the procedure described in section Verify Algorithm, using the verify signature mode (see Table 37). Signature byte values are listed in Table 35.

**Table 35.** Signature Bytes (Electronic ID)

| | | Signature Address | Signature Data |
|---|---|---|---|
| Vendor | Atmel | 30h | 58h |
| Architecture | C251 | 31h | 40h |
| Memory | 32 kilobytes EPROM or OTPROM | 60h | F7h |
| | 32 kilobytes MaskROM or ROMless | | 77h |
| Revision | TSC80251G2D derivative | 61h | FDh |

## Programming Algorithm

Figure 6 shows the hardware setup needed to program the TSC87251G2D EPROM/OTPROM areas:

- The chip has to be put under reset and maintained in this state until completion of the programming sequence.
- PSEN# and the other control signals (ALE and Port 0) have to be set to a high level.
- Then PSEN# has to be to forced to a low level after two clock cycles or more and it has to be maintained in this state until the completion of the programming sequence (see below).
- The voltage on the EA# pin must be set to $V_{DD}$.
- The programming mode is selected according to the code applied on Port 0 (see Table 36). It has to be applied until the completion of this programming operation.
- The programming address is applied on Ports 1 and 3 which are respectively the Most Significant Byte (MSB) and the Least Significant Byte (LSB) of the address.
- The programming data are applied on Port 2.
- The EPROM Programming is done by raising the voltage on the EA# pin to $V_{PP}$, then by generating a low level pulse on ALE/PROG# pin.
- The voltage on the EA# pin must be lowered to $V_{DD}$ before completing the programming operation.
- It is possible to alternate programming and verifying operation (See Paragraph Verify Algorithm). Please make sure the voltage on the EA# pin has actually been lowered to $V_{DD}$ before performing the verifying operation.

## Timings

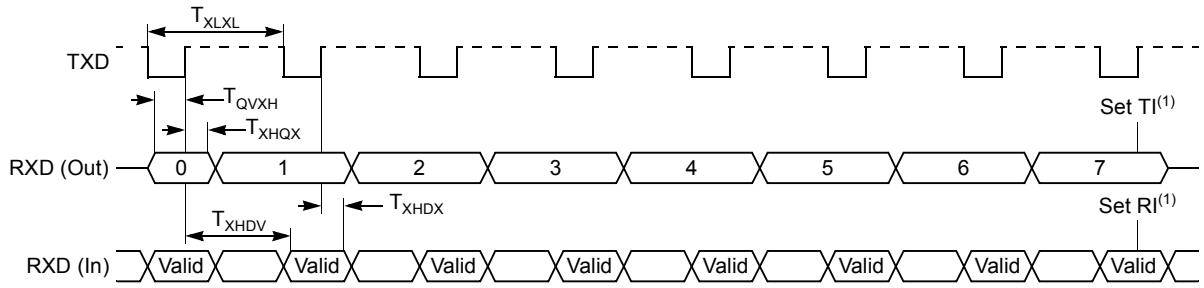
**Table 46.** Serial Port AC Timing -Shift Register Mode; $V_{DD}$ = 2.7 to 5.5 V, $T_A$ = -40 to 85°C

| | | 12 MHz | | 16 MHz | | 24 MHz(1) | | |
|---|---|---|---|---|---|---|---|---|
| Symbol | Parameter | Min | Max | Min | Max | Min | Max | Unit |
| $T_{XLXL}$ | Serial Port Clock Cycle Time | 998 | | 749 | | 500 | | ns |
| $T_{QVXH}$ | Output Data Setup to Clock Rising Edge | 833 | | 625 | | 417 | | ns |
| $T_{XHQX}$ | Output Data hold after Clock Rising Edge | 165 | | 124 | | 82 | | ns |
| $T_{XHDX}$ | Input Data Hold after Clock Rising Edge | 0 | | 0 | | 0 | | ns |
| $T_{XHDV}$ | Clock Rising Edge to Input Data Valid | | 974 | | 732 | | 482 | ns |

Note: 1. For high speed versions only.

## Waveforms

**Figure 17.** Serial Port Waveforms - Shift Register Mode




Note: 1. TI and RI are set during S1P1 of the peripheral cycle following the shift of the eight bit.

## Timings

**Table 51.** EPROM Programming AC timings; $V_{DD}$ = 4.5 to 5.5 V, $T_A$ = 0 to 40°C

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $T_{OSC}$ | XTAL1 Period | 83.5 | 250 | ns |
| $T_{AVGL}$ | Address Setup to PROG# low | 48 | | $T_{OSC}$ |
| $T_{GHAX}$ | Address Hold after PROG# low | 48 | | $T_{OSC}$ |
| $T_{DVGL}$ | Data Setup to PROG# low | 48 | | $T_{OSC}$ |
| $T_{GHDX}$ | Data Hold after PROG# | 48 | | $T_{OSC}$ |
| $T_{ELSH}$ | ENABLE High to $V_{PP}$ | 48 | | $T_{OSC}$ |
| $T_{SHGL}$ | $V_{PP}$ Setup to PROG# low | 10 | | µs |
| $T_{GHSL}$ | $V_{PP}$ Hold after PROG# | 10 | | µs |
| $T_{SLEH}$ | ENABLE Hold after $V_{PP}$ | 0 | | ns |
| $T_{GLGH}$ | PROG# Width | 90 | 110 | µs |

**Table 52.** EPROM Verifying AC timings; $V_{DD}$ = 4.5 to 5.5 V, $V_{DD}$ = 2.7 to 5.5 V, $T_A$ = 0 to 40°C

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $T_{OSC}$ | XTAL1 Period | 83.5 | 250 | ns |
| $T_{AVQV}$ | Address to Data Valid | | 48 | $T_{OSC}$ |
| $T_{AXQX}$ | Address to Data Invalid | 0 | | ns |
| $T_{ELQV}$ | ENABLE low to Data Valid | 0 | 48 | $T_{OSC}$ |
| $T_{EHQZ}$ | Data Float after ENABLE | 0 | 48 | $T_{OSC}$ |

## Waveforms

**Figure 23.** EPROM Programming Waveforms

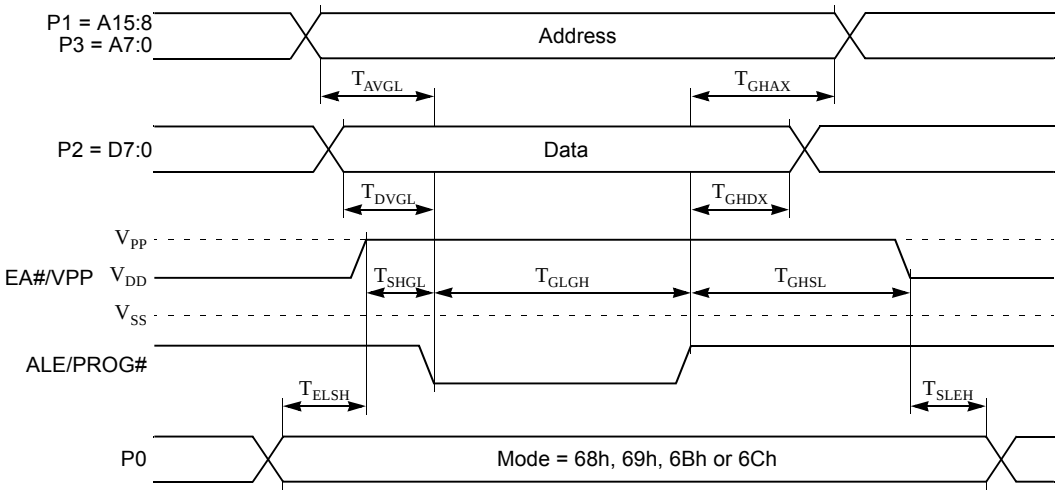
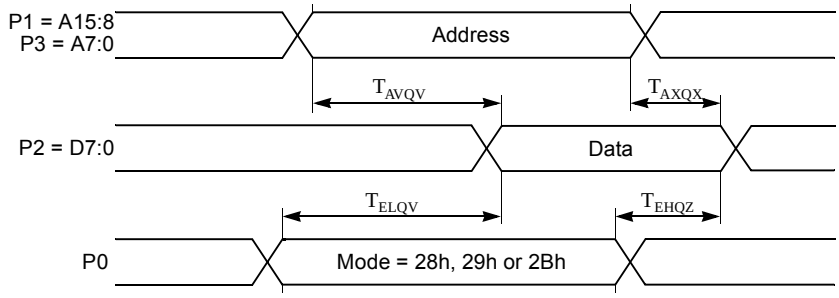


**Figure 24.** EPROM Verifying Waveforms




## AC Characteristics - External Clock Drive and Logic Level References

### Definition of Symbols

**Table 53.** External Clock Timing Symbol Definitions

| Signals | |
|---|---|
| C | Clock |

| Conditions | |
|---|---|
| H | High |
| L | Low |
| X | No Longer Valid |

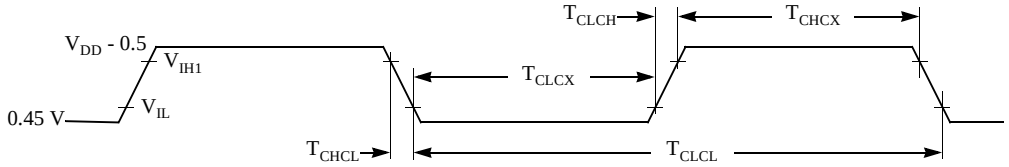
### Timings

**Table 54.** External Clock AC Timings; $V_{DD}$ = 4.5 to 5.5 V, $T_A$ = -40 to +85°C

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $F_{OSC}$ | Oscillator Frequency | | 24 | MHz |
| $T_{CHCX}$ | High Time | 10 | | ns |
| $T_{CLCX}$ | Low Time | 10 | | ns |
| $T_{CLCH}$ | Rise Time | 3 | | ns |
| $T_{CHCL}$ | Fall Time | 3 | | ns |

### Waveforms

**Figure 25.** External Clock Waveform




Notes: 1. During AC testing, all inputs are driven at $V_{DD}$ -0.5 V for a logic 1 and 0.45 V for a logic 0.
2. Timing measurements are made on all outputs at $V_{IH}$ min for a logic 1 and $V_{IL}$ max for a logic 0.

Notes: 1. Under steady-state (non-transient) conditions, $I_{OL}$ must be externally limited as follows:

Maximum IOL per port pin: 10 mA

Maximum IOL per 8-bit port:Port 0 26 mA

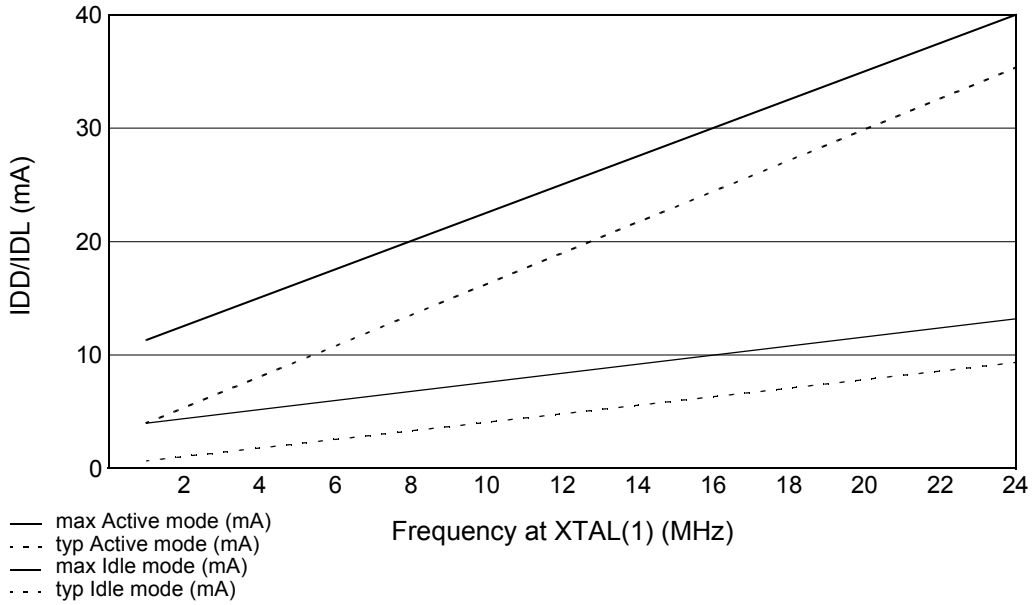
Ports 1-3 15 mA

Maximum Total IOL for all: Output Pins 71 mA

If IOL exceeds the test conditions, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

2. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses above 0.4 V on the low-level outputs of ALE and Ports 1, 2, and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from high to low. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8 V. It may be desirable to qualify ALE or other signals with a Schmitt Trigger or CMOS-level input logic.
3. Capacitive loading on Ports 0 and 2 causes the $V_{OH}$ on ALE and PSEN# to drop below the specification when the address lines are stabilizing.
4. Typical values are obtained using $V_{DD}$ = 5 V and $T_A$ = 25°C. They are not tested and there is not guarantee on these values.
5. The input threshold voltage of SCL and SDA meets the TWI specification, so an input voltage below $0.3 \cdot V_{DD}$ will be recognized as a logic 0 while an input voltage above $0.7 \cdot V_{DD}$ will be recognized as a logic 1.

**Figure 28.** $I_{DD}/I_{DL}$ Versus Frequency; $V_{DD}$ = 4.5 to 5.5 V




Note: 1. The clock prescaler is not used: $F_{OSC} = F_{XTAL}$.

## Low Voltage Versions - Commercial & Industrial

**Table 56.** DC Characteristics; $V_{DD}$ = 2.7 to 5.5 V, $T_A$ = -40 to +85°C

| Symbol | Parameter | Min | Typical[4] | Max | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage (except EA#, SCL, SDA) | -0.5 | | $0.2 \cdot V_{DD}$ - 0.1 | V | |
| $V_{IL1}$[5] | Input Low Voltage (SCL, SDA) | -0.5 | | $0.3 \cdot V_{DD}$ | V | |
| $V_{IL2}$ | Input Low Voltage (EA#) | 0 | | $0.2 \cdot V_{DD}$ - 0.3 | V | |
| $V_{IH}$ | Input high Voltage (except XTAL1, RST, SCL, SDA) | $0.2 \cdot V_{DD}$ + 0.9 | | $V_{DD}$ + 0.5 | V | |
| $V_{IH1}$[5] | Input high Voltage (XTAL1, RST, SCL, SDA) | $0.7 \cdot V_{DD}$ | | $V_{DD}$ + 0.5 | V | |
| $V_{OL}$ | Output Low Voltage (Ports 1, 2, 3) | | | 0.45 | V | $I_{OL}$ = 0.8 mA[1][2] |
| $V_{OL1}$ | Output Low Voltage (Ports 0, ALE, PSEN#, Port 2 in Page Mode during External Address) | | | 0.45 | V | $I_{OL}$ = 1.6 mA[1][2] |
| $V_{OH}$ | Output high Voltage (Ports 1, 2, 3, ALE, PSEN#) | $0.9 \cdot V_{DD}$ | | | V | $I_{OH}$ = -10 µA[3] |
| $V_{OH1}$ | Output high Voltage (Port 0, Port 2 in Page Mode during External Address) | $0.9 \cdot V_{DD}$ | | | V | $I_{OH}$ = -40 µA |
| $V_{RET}$ | $V_{DD}$ data retention limit | | | 1.8 | V | |
| $I_{IL0}$ | Logical 0 Input Current (Ports 1, 2, 3 - AWAIT#) | | | - 50 | µA | $V_{IN}$ = 0.45 V |
| $I_{IL1}$ | Logical 1 Input Current (NMI) | | | + 50 | µA | $V_{IN} = V_{DD}$ |
| $I_{LI}$ | Input Leakage Current (Port 0) | | | ± 10 | µA | 0.45 V < $V_{IN}$ < $V_{DD}$ |
| $I_{TL}$ | Logical 1-to-0 Transition Current (Ports 1, 2, 3) | | | - 650 | µA | $V_{IN}$ = 2.0 V |
| $R_{RST}$ | RST Pull-Down Resistor | 40 | 110 | 225 | kΩ | |
| $C_{IO}$ | Pin Capacitance | | 10 | | pF | $T_A$ = 25°C |
| $I_{DD}$ | Operating Current | | 4<br>8<br>9<br>11 | 8<br>11<br>12<br>14 | mA | 5 MHz, $V_{DD}$ < 3.6 V<br>10 MHz, $V_{DD}$ < 3.6 V<br>12 MHz, $V_{DD}$ < 3.6 V<br>16 MHz, $V_{DD}$ < 3.6 V |
| $I_{DL}$ | Idle Mode Current | | 0.5<br>1.5<br>2<br>3 | 1<br>4<br>5<br>7 | mA | 5 MHz, $V_{DD}$ < 3.6 V<br>10 MHz, $V_{DD}$ < 3.6 V<br>12 MHz, $V_{DD}$ < 3.6 V<br>16 MHz, $V_{DD}$ < 3.6 V |
| $I_{PD}$ | Power-Down Current | | 1 | 10 | µA | $V_{RET}$ < $V_{DD}$ < 3.6 V |

Notes: 1. Under steady-state (non-transient) conditions, $I_{OL}$ must be externally limited as follows:

Maximum IOL per port pin: 10 mA

Maximum IOL per 8-bit port: Port 0 26 mA

Ports 1-315 mA

# Packages

## List of Packages

- PDIL 40
- CDIL 40 with window
- PLCC 44
- CQPJ 44 with window
- VQFP 44 (10x10)

## PDIL 40 - Mechanical Outline

**Figure 33.** Plastic Dual In Line

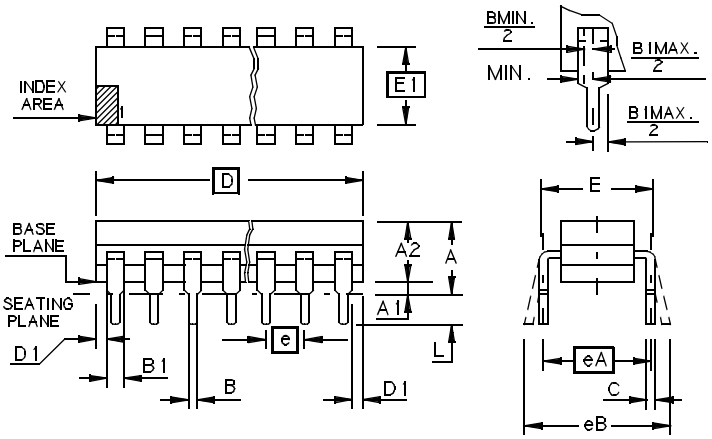



**Table 57.** PDIL Package Size

| | MM | | Inch | |
|---|---|---|---|---|
| | **Min** | **Max** | **Min** | **Max** |
| A | - | 5.08 | - | .200 |
| A1 | 0.38 | - | .015 | - |
| A2 | 3.18 | 4.95 | .125 | .195 |
| B | 0.36 | 0.56 | .014 | .022 |
| B1 | 0.76 | 1.78 | .030 | .070 |
| C | 0.20 | 0.38 | .008 | .015 |
| D | 50.29 | 53.21 | 1.980 | 2.095 |
| E | 15.24 | 15.87 | .600 | .625 |
| E1 | 12.32 | 14.73 | .485 | .580 |
| e | 2.54 B.S.C. | | .100 B.S.C. | |
| eA | 15.24 B.S.C. | | .600 B.S.C. | |
| eB | - | 17.78 | - | .700 |
| L | 2.93 | 3.81 | .115 | .150 |
| D1 | 0.13 | - | .005 | - |

## CDIL 40 with Window - Mechanical Outline

**Figure 34.** Ceramic Dual In Line

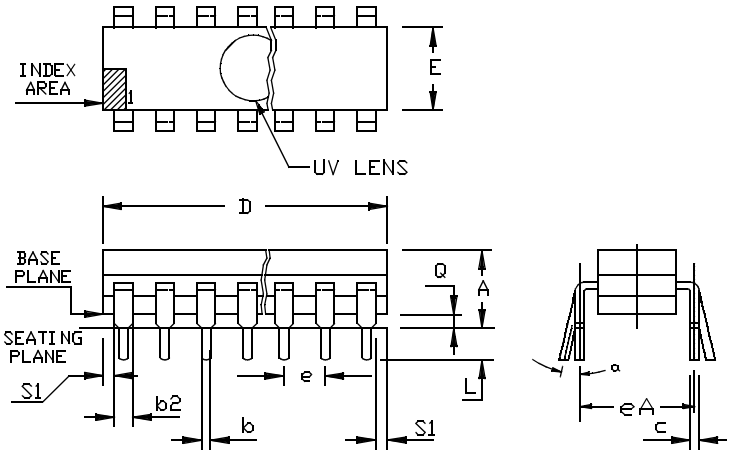



**Table 58.** CDIL Package Size

| | MM | | Inch | |
|---|---|---|---|---|
| | **Min** | **Max** | **Min** | **Max** |
| A | - | 5.71 | - | .225 |
| b | 0.36 | 0.58 | .014 | .023 |
| b2 | 1.14 | 1.65 | .045 | .065 |
| c | 0.20 | 0.38 | .008 | .015 |
| D | - | 53.47 | - | 2.105 |
| E | 13.06 | 15.37 | .514 | .605 |
| e | 2.54 B.S.C. | | .100 B.S.C. | |
| eA | 15.24 B.S.C. | | .600 B.S.C. | |
| L | 3.18 | 5.08 | .125 | .200 |
| Q | 0.38 | 1.40 | .015 | .055 |
| S1 | 0.13 | - | .005 | - |
| a | 0 - 15 | | 0 - 15 | |
| N | 40 | | | |

## VQFP 44 (10x10) - Mechanical Outline

**Figure 37.** Shrink Quad Flat Pack (Plastic)

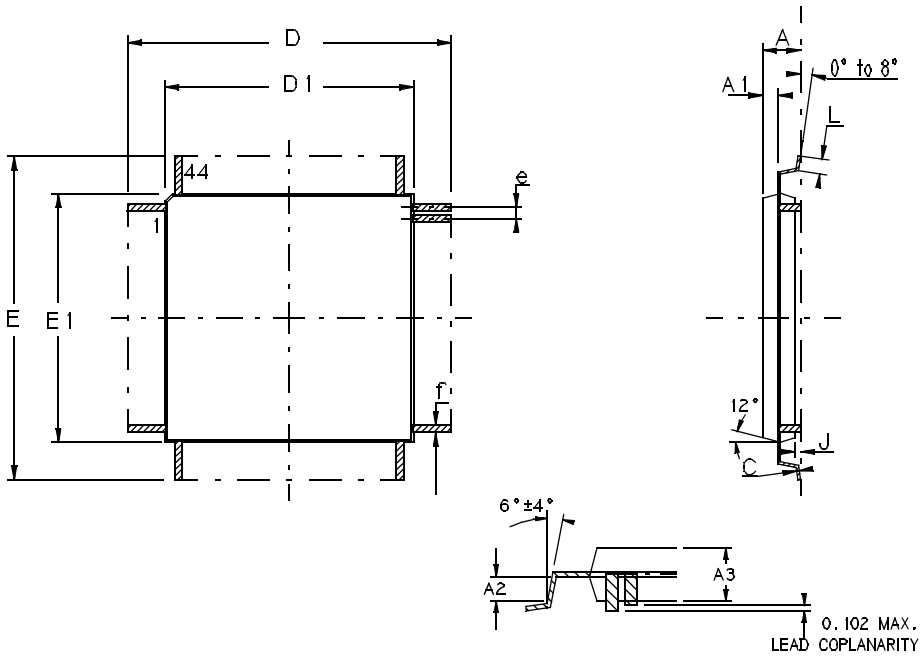



**Table 61.** VQFP Package Size

| | MM | | Inch | |
|---|---|---|---|---|
| | **Min** | **Max** | **Min** | **Max** |
| A | - | 1.60 | - | .063 |
| A1 | 0.64 REF | | .025 REF | |
| A2 | 0.64 REF | | .025REF | |
| A3 | 1.35 | 1.45 | .053 | .057 |
| D | 11.90 | 12.10 | .468 | .476 |
| D1 | 9.90 | 10.10 | .390 | .398 |
| E | 11.90 | 12.10 | .468 | .476 |
| E1 | 9.90 | 10.10 | .390 | .398 |
| J | 0.05 | - | .002 | 6 |
| L | 0.45 | 0.75 | .018 | .030 |
| e | 0.80 BSC | | .0315 BSC | |
| f | 0.35 BSC | | .014 BSC | |

### AT/TSC87251G2D OTPROM

| Part Number | ROM | Description |
|---|---|---|
| **High Speed Versions 4.5 to 5.5 V, Commercial and Industrial** | | |
| TSC87251G2D-16CB | 32K OTPROM | 16 MHz, Commercial 0° to 70°C, PLCC 44 |
| TSC87251G2D-24CB | 32K OTPROM | 24 MHz, Commercial 0° to 70°C, PLCC 44 |
| TSC87251G2D-24CED | 32K OTPROM | 24 MHz, Commercial 0° to 70°C, VQFP 44 |
| TSC87251G2D-24IA | 32K OTPROM | 24 MHz, Industrial -40° to 85°C, PDIL 40 |
| TSC87251G2D-24IB | 32K OTPROM | 24 MHz, Industrial -40° to 85°C, PLCC 44 |
| AT87251G2D-SLSUM | 32K OTPROM | 24 MHz, Industrial & Green -40° to 85°C, PLCC 44 |
| AT87251G2D-3CSUM | 32K OTPROM | 24 MHz, Industrial & Green -40° to 85°C, PDIL 40 |
| AT87251G2D-RLTUM | 32K OTPROM | 24 MHz, Industrial & Green -40° to 85°C, VQFP 44 |
| **Low Voltage Versions 2.7 to 5.5 V** | | |
| TSC87251G2D-L16CB | 32K OTPROM | 16 MHz, Commercial 0° to 70°C, PLCC 44 |
| TSC87251G2D-L16CED | 32K OTPROM | 16 MHz, Commercial 0° to 70°C, VQFP 44 |
| AT87251G2D-SLSUL | 32K OTPROM | 16 MHz, Industrial & Green, 0° to 70°C, PLCC 44 |
| AT87251G2D-RLTUL | 32K OTPROM | 16 MHz, Industrial & Green, 0° to 70°C, VQFP 44 |

## Document Revision History

**Changes from 4135D to 4135E**

1. Added automotive qualification, and ordering information for ROM product version.

**Changes from 4135E to 4135F**

1. Absolute Maximum Ratings added for automotive product version.