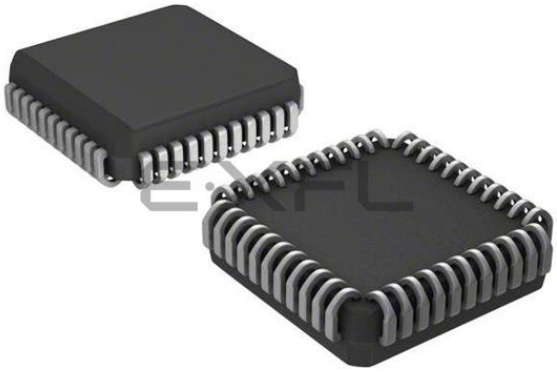

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C251
Core Size	8/16-Bit
Speed	24MHz
Connectivity	EBI/EMI, I²C, Microwire, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.6x16.6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/tsc87251g2d-24cb

- **Typical Operating Current:11 mA at 3V**
- **Typical Power-down Current: 1 µA**
- **Temperature Ranges: Commercial (0°C to +70°C), Industrial (-40°C to +85°C), Automotive ((-40°C to +85°C) ROM only)**
- **Option: Extended Range (-55°C to +125°C)**
- **Packages: PDIL 40, PLCC 44 and VQFP 44**
- **Options: Known Good Dice and Ceramic Packages**

Description

The TSC80251G2D products are derivatives of the Atmel Microcontroller family based on the 8/16-bit C251 Architecture. This family of products is tailored to 8/16-bit microcontroller applications requiring an increased instruction throughput, a reduced operating frequency or a larger addressable memory space. The architecture can provide a significant code size reduction when compiling C programs while fully preserving the legacy of C51 assembly routines.

The TSC80251G2D derivatives are pin and software compatible with standard 80C51/Fx/Rx/Rx+ with extended on-chip data memory (1 Kbyte RAM) and up to 256 kilobytes of external code and data. Additionally, the TSC83251G2D and TSC87251G2D provide on-chip code memory: 32 kilobytes ROM and 32 kilobytes EPROM/OTPROM respectively.

They provide transparent enhancements to Intel's 8xC251Sx family with an additional Synchronous Serial Link Controller (SSLC supporting TWI, µWire and SPI protocols), a Keyboard interrupt interface, a dedicated Baud Rate Generator for UART, and Power Management features.

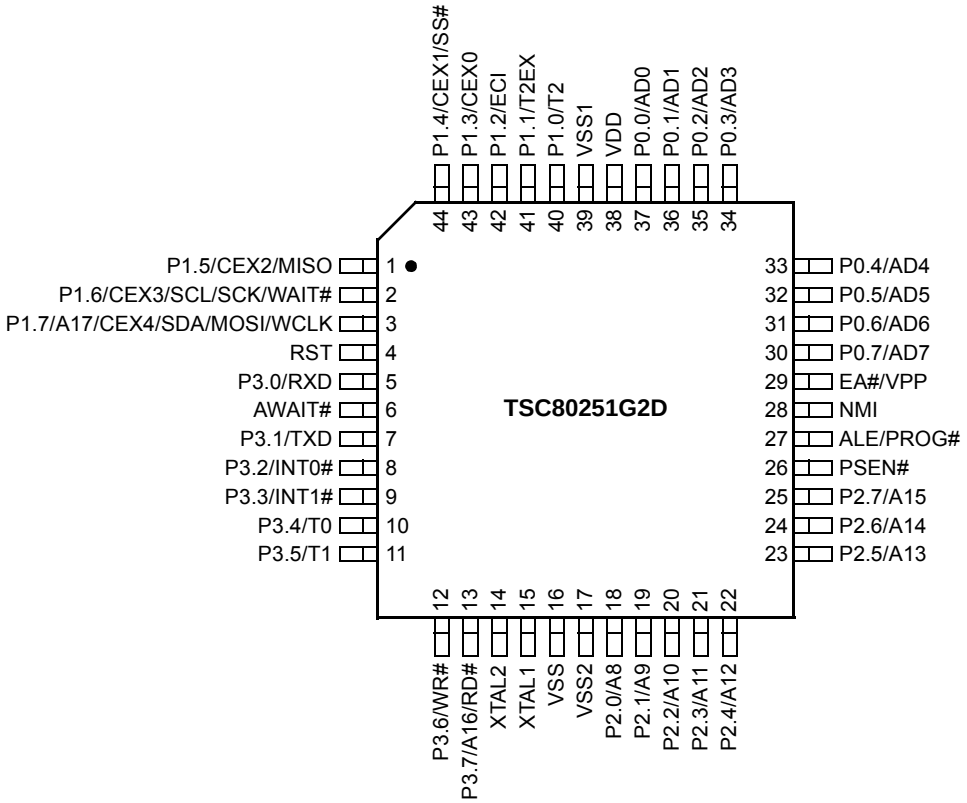
TSC80251G2D derivatives are optimized for speed and for low power consumption on a wide voltage range.

Note: 1. This Datasheet provides the technical description of the TSC80251G2D derivatives. For further information on the device usage, please request the TSC80251 Programmer's Guide and the TSC80251G1D Design Guide and errata sheet.

Typical Applications

- ISDN Terminals
- High-Speed Modems
- PABX (SOHO)
- Line Cards
- DVD ROM and Players
- Printers
- Plotters
- Scanners
- Banking Machines
- Barcode Readers
- Smart Cards Readers
- High-End Digital Monitors
- High-End Joysticks
- High-end TV's

Figure 3. TSC80251G2D 44-pin VQFP Package



Signals

Table 2. Product Name Signal Description

Signal Name	Type	Description	Alternate Function
A17	O	**18th Address Bit** Output to memory as 18th external address bit (A17) in extended bus applications, depending on the values of bits RD0 and RD1 in UCONFIG0 byte (see Table 13, Page 20).	P1.7
A16	O	**17th Address Bit** Output to memory as 17th external address bit (A16) in extended bus applications, depending on the values of bits RD0 and RD1 in UCONFIG0 byte (see Table 13, Page 20).	P3.7
A15:8(1)	O	**Address Lines** Upper address lines for the external bus.	P2.7:0
AD7:0(1)	I/O	**Address/Data Lines** Multiplexed lower address lines and data for the external memory.	P0.7:0
ALE	O	**Address Latch Enable** ALE signals the start of an external bus cycle and indicates that valid address information are available on lines A16/A17 and A7:0. An external latch can use ALE to demultiplex the address from address/data bus.	–
AWAIT#	I	**Real-time Asynchronous Wait States Input** When this pin is active (low level), the memory cycle is stretched until it becomes high. When using the Product Name as a pin-for-pin replacement for a 8xC51 product, AWAIT# can be unconnected without loss of compatibility or power consumption increase (on-chip pull-up). Not available on DIP package.	–
CEX4:0	I/O	**PCA Input/Output pins** CEXx are input signals for the PCA capture mode and output signals for the PCA compare and PWM modes.	P1.7:3
EA#	I	**External Access Enable** EA# directs program memory accesses to on-chip or off-chip code memory. For EA# = 0, all program memory accesses are off-chip. For EA# = 1, an access is on-chip ROM if the address is within the range of the on-chip ROM; otherwise the access is off-chip. The value of EA# is latched at reset. For devices without ROM on-chip, EA# must be strapped to ground.	–
ECI	O	**PCA External Clock input** ECI is the external clock input to the 16-bit PCA timer.	P1.2
MISO	I/O	**SPI Master Input Slave Output line** When SPI is in master mode, MISO receives data from the slave peripheral. When SPI is in slave mode, MISO outputs data to the master controller.	P1.5
MOSI	I/O	**SPI Master Output Slave Input line** When SPI is in master mode, MOSI outputs data to the slave peripheral. When SPI is in slave mode, MOSI receives data from the master controller.	P1.7
INT1:0#	I	**External Interrupts 0 and 1** INT1#/INT0# inputs set IE1:0 in the TCON register. If bits IT1:0 in the TCON register are set, bits IE1:0 are set by a falling edge on INT1#/INT0#. If bits IT1:0 are cleared, bits IE1:0 are set by a low level on INT1#/INT0#.	P3.3:2

Table 2. Product Name Signal Description (Continued)

Signal Name	Type	Description	Alternate Function
XTAL2	O	**Output of the on-chip inverting oscillator amplifier** To use the internal oscillator, a crystal/resonator circuit is connected to this pin. If an external oscillator is used, leave XTAL2 unconnected.	–

Note: The description of A15:8/P2.7:0 and AD7:0/P0.7:0 are for the Non-Page mode chip configuration. If the chip is configured in Page mode operation, port 0 carries the lower address bits (A7:0) while port 2 carries the upper address bits (A15:8) and the data (D7:0).

Table 10. SFR Descriptions

	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h		CH 0000 0000	CCAP0H 0000 0000	CCAP1H 0000 0000	CCAP2H 0000 0000	CCAP3H 0000 0000	CCAP4H 0000 0000		FFh
F0h	B(1) 0000 0000								F7h
E8h		CL 0000 0000	CCAP0L 0000 0000	CCAP1L 0000 0000	CCAP2L 0000 0000	CCAP3L 0000 0000	CCAP4L 0000 0000		EFh
E0h	ACC(1) 0000 0000								E7h
D8h	CCON 00X0 0000	CMOD 00XX X000	CCAPM0 X000 0000	CCAPM1 X000 0000	CCAPM2 X000 0000	CCAPM3 X000 0000	CCAPM4 X000 0000		DFh
D0h	PSW(1) 0000 0000	PSW1(1) 0000 0000							D7h
C8h	T2CON 0000 0000	T2MOD XXXX XX00	RCAP2L 0000 0000	RCAP2H 0000 0000	TL2 0000 0000	TH2 0000 0000			CFh
C0h									C7h
B8h	IPL0 X000 0000	SADEN 0000 0000					SPH(1) 0000 0000		BFh
B0h	P3 1111 1111	IE1 XX0X XXX0	IPL1 XX0X XXX0	IPH1 XX0X XXX0				IPH0 X000 0000	B7h
A8h	IE0 0000 0000	SADDR 0000 0000							AFh
A0h	P2 1111 1111						WDTRST 1111 1111	WCON XXXX XX00	A7h
98h	SCON 0000 0000	SBUF XXXX XXXX	BRL 0000 0000	BDRCON XXX0 0000	P1LS 0000 0000	P1IE 0000 0000	P1F 0000 0000		9Fh
90h	P1 1111 1111		SSBR 0000 0000	SSCON(2)	SSCS(3)	SSDAT 0000 0000	SSADR 0000 0000		97h
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	CKRL 0000 1000	POWM 0XXX XXXX	8Fh
80h	P0 1111 1111	SP(1) 0000 0111	DPL(1) 0000 0000	DPH(1) 0000 0000	DPXL(1) 0000 0001			PCON 0000 0000	87h
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

Reserved

Notes:
1. These registers are described in the TSC80251 Programmer's Guide (C251 core registers).
2. In TWI and SPI modes, SSCON is splitted in two separate registers. SSCON reset value is 0000 0000 in TWI mode and 0000 0100 in SPI mode.
3. In read and write modes, SSCS is splitted in two separate registers. SSCS reset value is 1111 1000 in read mode and 0000 0000 in write mode.

4. If this instruction addresses external memory location, add 2(N+2) to the number of states (N: number of wait states).

Table 21. Summary of Increment and Decrement Instructions

IncrementINC <dest>dest opnd ← dest opnd + 1 IncrementINC <dest>, <src>dest opnd ← dest opnd + src opnd DecrementDEC <dest>dest opnd ← dest opnd - 1 DecrementDEC <dest>, <src>dest opnd ← dest opnd - src opnd						
Mnemonic	**<dest>, <src>(1)**	**Comments**	**Binary Mode**		**Source Mode**	
			Bytes	**States**	**Bytes**	**States**
INC DEC	A	ACC by 1	1	1	1	1
	Rn	Register by 1	1	1	2	2
	dir8	Direct address (on-chip RAM or SFR) by 1	2	2(2)	2	2(2)
	at Ri	Indirect address by 1	1	3	2	4
INC DEC	Rm, #short	Byte register by 1, 2, or 4	3	2	2	1
	WRj, #short	Word register by 1, 2, or 4	3	2	2	1
INC	DRk, #short	Double word register by 1, 2, or 4	3	4	2	3
DEC	DRk, #short	Double word register by 1, 2, or 4	3	5	2	4
INC	DPTR	Data pointer by 1	1	1	1	1

Notes: 1. A shaded cell denotes an instruction in the C51 Architecture.
2. If this instruction addresses an I/O Port (Px, x = 0-3), add 2 to the number of states. Add 3 if it addresses a Peripheral SFR.

MOV	WRj, at WRj +dis24	Indirect with 16-bit displacement (16M) to word register	5	8[5]	4	7[5]
MOV	at WRj +dis16, Rm	Byte register to indirect with 16-bit displacement (64K)	5	6[4]	4	5[4]
MOV	at WRj +dis16, WRj	Word register to indirect with 16-bit displacement (64K)	5	7[5]	4	6[5]
MOV	at DRk +dis24, Rm	Byte register to indirect with 16-bit displacement (16M)	5	7[4]	4	6[4]
MOV	at DRk +dis24, WRj	Word register to indirect with 16-bit displacement (16M)	5	8[5]	4	7[5]

Notes:
1. Instructions that move bits are in Table 27.
2. Move instructions unique to the C251 Architecture.
3. If this instruction addresses an I/O Port (Px, x = 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.
4. If this instruction addresses external memory location, add N+2 to the number of states (N: number of wait states).
5. If this instruction addresses external memory location, add 2(N+1) to the number of states (N: number of wait states).
6. If this instruction addresses external memory location, add 4(N+2) to the number of states (N: number of wait states).

Table 27. Summary of Bit Instructions

Clear BitCLR <dest>dest opnd ← 0						
Set BitSETB <dest>dest opnd ← 1						
Complement BitCPL <dest>dest opnd ← ∅ bit						
AND Carry with BitANL CY, <src>(CY) ← (CY) ∧ src opnd						
AND Carry with Complement of BitANL CY, /<src>(CY) ← (CY) ∧ ∅ src opnd						
OR Carry with BitORL CY, <src>(CY) ← (CY) ∨ src opnd						
OR Carry with Complement of BitORL CY, /<src>(CY) ← (CY) ∨ ∅ src opnd						
Move Bit to CarryMOV CY, <src>(CY) ← src opnd						
Move Bit from CarryMOV <dest>, CYdest opnd ← (CY)						
Mnemonic	**<dest>, <src>(1)**	**Comments**	**Binary Mode**		**Source Mode**	
			Bytes	**States**	**Bytes**	**States**
CLR	CY	Clear carry	1	1	1	1
	bit51	Clear direct bit	2	2(3)	2	2(3)
	bit	Clear direct bit	4	4(3)	3	3(3)
SETB	CY	Set carry	1	1	1	1
	bit51	Set direct bit	2	2(3)	2	2(3)
	bit	Set direct bit	4	4(3)	3	3(3)
CPL	CY	Complement carry	1	1	1	1
	bit51	Complement direct bit	2	2(3)	2	2(3)
	bit	Complement direct bit	4	4(3)	3	3(3)
ANL	CY, bit51	And direct bit to carry	2	1(2)	2	1(2)
	CY, bit	And direct bit to carry	4	3(2)	3	2(2)
	CY, /bit51	And complemented direct bit to carry	2	1(2)	2	1(2)
	CY, /bit	And complemented direct bit to carry	4	3(2)	3	2(2)
ORL	CY, bit51	Or direct bit to carry	2	1(2)	2	1(2)
	CY, bit	Or direct bit to carry	4	3(2)	3	2(2)
	CY, /bit51	Or complemented direct bit to carry	2	1(2)	2	1(2)
	CY, /bit	Or complemented direct bit to carry	4	3(2)	3	2(2)
MOV	CY, bit51	Move direct bit to carry	2	1(2)	2	1(2)
	CY, bit	Move direct bit to carry	4	3(2)	3	2(2)
	bit51, CY	Move carry to direct bit	2	2(3)	2	2(3)
	bit, CY	Move carry to direct bit	4	4(3)	3	3(3)

Notes:
1. A shaded cell denotes an instruction in the C51 Architecture.
2. If this instruction addresses an I/O Port (Px, x = 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.
3. If this instruction addresses an I/O Port (Px, x = 0-3), add 2 to the number of states. Add 3 if it addresses a Peripheral SFR.

Table 30. Summary of Conditional Jump Instructions (2/2)

Jump if bitJB <src>, rel(PC) ← (PC) + size (instr);
IF [src opnd = 1] THEN (PC) ← (PC) + rel

Jump if not bitJNB <src>, rel(PC) ← (PC) + size (instr);
IF [src opnd = 0] THEN (PC) ← (PC) + rel

Jump if bit and clearJBC <dest>, rel(PC) ← (PC) + size (instr);
IF [dest opnd = 1] THEN
dest opnd ← 0
(PC) ← (PC) + rel

Jump if accumulator is zeroJZ rel(PC) ← (PC) + size (instr);
IF [(A) = 0] THEN (PC) ← (PC) + rel

Jump if accumulator is not zeroJNZ rel(PC) ← (PC) + size (instr);
IF [(A) ≠ 0] THEN (PC) ← (PC) + rel

Compare and jump if not equalCJNE <src1>, <src2>, rel(PC) ← (PC) + size (instr);
IF [src opnd1 < src opnd2] THEN (CY) ← 1
IF [src opnd1 ≥ src opnd2] THEN (CY) ← 0
IF [src opnd1 ≠ src opnd2] THEN (PC) ← (PC) + rel

Decrement and jump if not zeroDJNZ <dest>, rel(PC) ← (PC) + size (instr); dest opnd ← dest opnd -1;
IF [φ (Z)] THEN (PC) ← (PC) + rel

Mnemonic	<dest>, <src>[1]	Comments	Binary Mode[2]		Source Mode[2]	
			Bytes	States	Bytes	States
JB	bit51, rel	Jump if direct bit is set	3	2/5[3][6]	3	2/5[3][6]
	bit, rel	Jump if direct bit of 8-bit address location is set	5	4/7[3][6]	4	3/6[3][6]
JNB	bit51, rel	Jump if direct bit is not set	3	2/5[3][6]	3	2/5[3][6]
	bit, rel	Jump if direct bit of 8-bit address location is not set	5	4/7[3][6]	4	3/6[3]
JBC	bit51, rel	Jump if direct bit is set & clear bit	3	4/7[5][6]	3	4/7[5][6]
	bit, rel	Jump if direct bit of 8-bit address location is set and clear	5	7/10[5][6]	4	6/9[5][6]
JZ	rel	Jump if ACC is zero	2	2/5[6]	2	2/5[6]
JNZ	rel	Jump if ACC is not zero	2	2/5[6]	2	2/5[6]
CJNE	A, dir8, rel	Compare direct address to ACC and jump if not equal	3	2/5[3][6]	3	2/5[3][6]
	A, #data, rel	Compare immediate to ACC and jump if not equal	3	2/5[6]	3	2/5[6]
	Rn, #data, rel	Compare immediate to register and jump if not equal	3	2/5[6]	4	3/6[6]
	at Ri, #data, rel	Compare immediate to indirect and jump if not equal	3	3/6[6]	4	4/7[6]
DJNZ	Rn, rel	Decrement register and jump if not zero	2	2/5[6]	3	3/6[6]
	dir8, rel	Decrement direct address and jump if not zero	3	3/6[4][6]	3	3/6[4][6]

Notes:
1. A shaded cell denotes an instruction in the C51 Architecture.
2. States are given as jump not-taken/taken.
3. If this instruction addresses an I/O Port (Px, x = 0-3), add 1 to the number of states. Add 2 if it addresses a Peripheral SFR.
4. If this instruction addresses an I/O Port (Px, x = 0-3), add 2 to the number of states.

To preserve the secrecy of the encryption key byte sequence, the Encryption Array can not be verified.

Notes:
1. When a MOVC instruction is executed, the content of the ROM is not encrypted. In order to fully protect the user program code, the lock bit level 1 (see Table 33) must always be set when encryption is used.
2. If the encryption feature is implemented, the portion of the on-chip code memory that does not contain program code should be filled with “random” byte values to prevent the encryption key sequence from being revealed.

Signature Bytes

The TSC80251G2D derivatives contain factory-programmed Signature Bytes. These bytes are located in non-volatile memory outside the memory address space at 30h, 31h, 60h and 61h. To read the Signature Bytes, perform the procedure described in section Verify Algorithm, using the verify signature mode (see Table 37). Signature byte values are listed in Table 35.

Table 35. Signature Bytes (Electronic ID)

		Signature Address	Signature Data
Vendor	Atmel	30h	58h
Architecture	C251	31h	40h
Memory	32 kilobytes EPROM or OTPROM	60h	F7h
	32 kilobytes MaskROM or ROMless		77h
Revision	TSC80251G2D derivative	61h	FDh

Programming Algorithm

Figure 6 shows the hardware setup needed to program the TSC87251G2D EPROM/OTPROM areas:

- The chip has to be put under reset and maintained in this state until completion of the programming sequence.
- PSEN# and the other control signals (ALE and Port 0) have to be set to a high level.
- Then PSEN# has to be to forced to a low level after two clock cycles or more and it has to be maintained in this state until the completion of the programming sequence (see below).
- The voltage on the EA# pin must be set to V_{DD}.
- The programming mode is selected according to the code applied on Port 0 (see Table 36). It has to be applied until the completion of this programming operation.
- The programming address is applied on Ports 1 and 3 which are respectively the Most Significant Byte (MSB) and the Least Significant Byte (LSB) of the address.
- The programming data are applied on Port 2.
- The EPROM Programming is done by raising the voltage on the EA# pin to V_{PP}, then by generating a low level pulse on ALE/PROG# pin.
- The voltage on the EA# pin must be lowered to V_{DD} before completing the programming operation.
- It is possible to alternate programming and verifying operation (See Paragraph Verify Algorithm). Please make sure the voltage on the EA# pin has actually been lowered to V_{DD} before performing the verifying operation.

Timings

Table 42. Real-Time Synchronous Wait AC Timings; V_{DD} = 2.7 to 5.5 V, T_A = -40 to 85°C

Symbol	Parameter	Min	Max	Unit
T_{CLYV}	Wait Clock Low to Wait Set-up	0	T_{OSC} - 20	ns
T_{CLYX}	Wait Hold after Wait Clock Low	2W·T_{OSC} + 5	(1+2W)·T_{OSC} - 20	ns
T_{RLYV}	PSEN#/RD# Low to Wait Set-up	0	T_{OSC} - 20	ns
T_{RLYX}	Wait Hold after PSEN#/RD# Low	2W·T_{OSC} + 5	(1+2W)·T_{OSC} - 20	ns
T_{WLYV}	WR# Low to Wait Set-up	0	T_{OSC} - 20	ns
T_{WLYX}	Wait Hold after WR# Low	2W·T_{OSC} + 5	(1+2W)·T_{OSC} - 20	ns

Waveforms

Figure 14. Real-time Synchronous Wait State: Code Fetch/Data Read

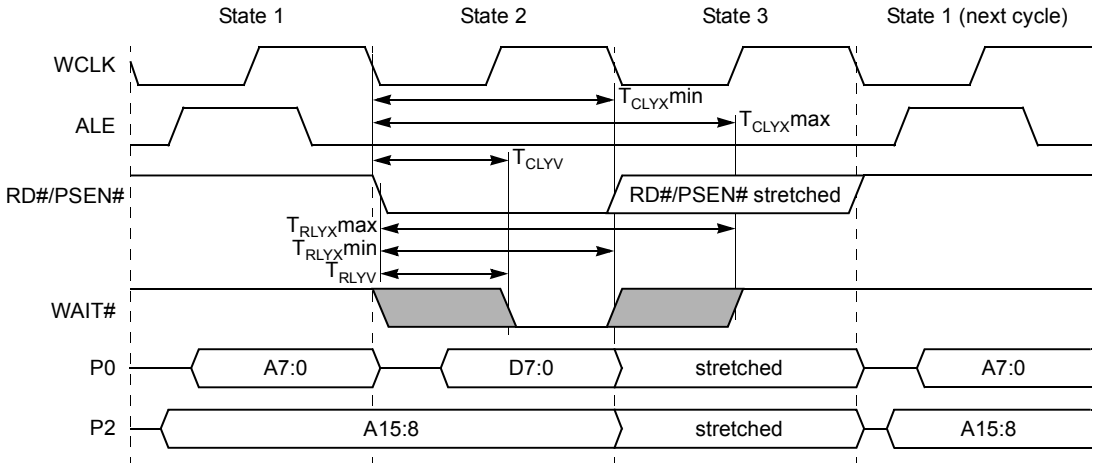
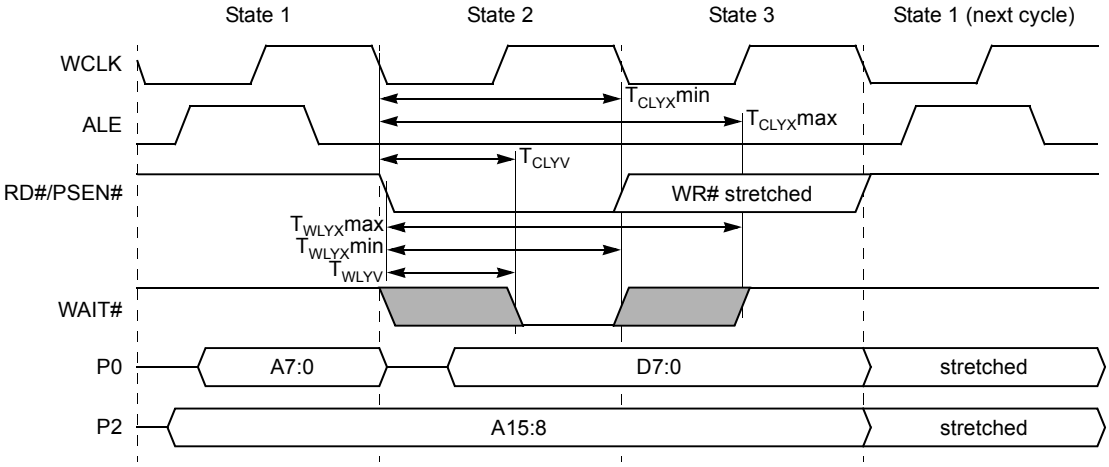


Figure 15. Real-time Synchronous Wait State: Data Write



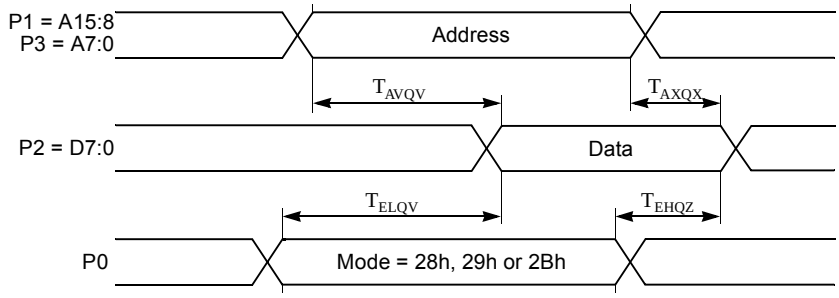
Timings

Table 49. SPI Interface AC Timing; V_{DD} = 2.7 to 5.5 V, T_A = -40 to 85°C

Symbol	Parameter	Min	Max	Unit
Slave Mode(1)				
T_{CHCH}	Clock Period	8		T_{OSC}
T_{CHCX}	Clock High Time	3.2		T_{OSC}
T_{CLCX}	Clock Low Time	3.2		T_{OSC}
T_{SLCH}, T_{SLCL}	SS# Low to Clock edge	200		ns
T_{IVCL}, T_{IVCH}	Input Data Valid to Clock Edge	100		ns
T_{CLIX}, T_{CHIX}	Input Data Hold after Clock Edge	100		ns
$T_{CLOV,}$ T_{CHOV}	Output Data Valid after Clock Edge		100	ns
T_{CLOX}, T_{CHOX}	Output Data Hold Time after Clock Edge	0		ns
T_{CLSH}, T_{CHSH}	SS# High after Clock Edge	0		ns
T_{IVCL}, T_{IVCH}	Input Data Valid to Clock Edge	100		ns
T_{CLIX}, T_{CHIX}	Input Data Hold after Clock Edge	100		ns
T_{SLOV}	SS# Low to Output Data Valid		130	ns
T_{SHOX}	Output Data Hold after SS# High		130	ns
T_{SHSL}	SS# High to SS# Low	(2)		
T_{ILIH}	Input Rise Time		2	µs
T_{IHIL}	Input Fall Time		2	µs
T_{OLOH}	Output Rise time		100	ns
T_{OHOL}	Output Fall Time		100	ns
Master Mode(3)				
T_{CHCH}	Clock Period	4		T_{OSC}
T_{CHCX}	Clock High Time	1.6		T_{OSC}
T_{CLCX}	Clock Low Time	1.6		T_{OSC}
T_{IVCL}, T_{IVCH}	Input Data Valid to Clock Edge	50		ns
T_{CLIX}, T_{CHIX}	Input Data Hold after Clock Edge	50		ns
$T_{CLOV,}$ T_{CHOV}	Output Data Valid after Clock Edge		65	ns
T_{CLOX}, T_{CHOX}	Output Data Hold Time after Clock Edge	0		ns
T_{ILIH}	Input Data Rise Time		2	µs
T_{IHIL}	Input Data Fall Time		2	µs
T_{OLOH}	Output Data Rise time		50	ns
T_{OHOL}	Output Data Fall Time		50	ns

Notes: 1. Capacitive load on all pins = 200 pF in slave mode.
2. The value of this parameter depends on software.
3. Capacitive load on all pins = 100 pF in master mode.

Figure 24. EPROM Verifying Waveforms



AC Characteristics - External Clock Drive and Logic Level References

Definition of Symbols

Table 53. External Clock Timing Symbol Definitions

Signals	
C	Clock

Conditions	
H	High
L	Low
X	No Longer Valid

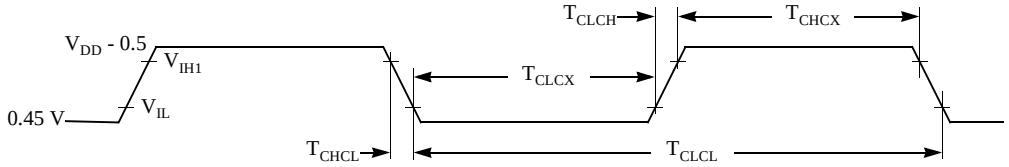
Timings

Table 54. External Clock AC Timings; V_{DD} = 4.5 to 5.5 V, T_A = -40 to +85°C

Symbol	Parameter	Min	Max	Unit
F_{OSC}	Oscillator Frequency		24	MHz
T_{CHCX}	High Time	10		ns
T_{CLCX}	Low Time	10		ns
T_{CLCH}	Rise Time	3		ns
T_{CHCL}	Fall Time	3		ns

Waveforms

Figure 25. External Clock Waveform



Notes: 1. During AC testing, all inputs are driven at V_{DD} -0.5 V for a logic 1 and 0.45 V for a logic 0.
2. Timing measurements are made on all outputs at V_{IH} min for a logic 1 and V_{IL} max for a logic 0.

Absolute Maximum Rating and Operating Conditions

Absolute Maximum Ratings

Storage Temperature ..... -65 to +150°C Voltage on any other Pin to VSS ..... -0.5 to +6.5 V I_{OL} per I/O Pin ..... 15 mA Power Dissipation ..... 1.5 W Ambient Temperature Under Bias Commercial.....0 to +70°C Industrial ..... -40 to +85°C Automotive..... -40 to +85°C V_{DD} High Speed versions..... 4.5 to 5.5 V Low Voltage versions..... 2.7 to 5.5 V	*NOTICE: Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only. Operation beyond the “operating conditions” is not recommended and extended exposure beyond the “Operating Conditions” may affect device reliability.

Figure 31. I_{DL} Test Condition, Idle Mode

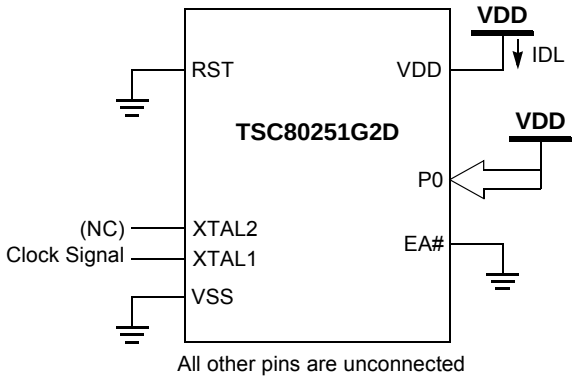
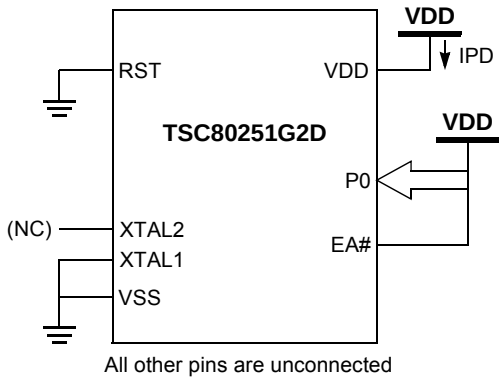


Figure 32. I_{PD} Test Condition, Power-Down Mode



Packages

List of Packages

- PDIL 40
- CDIL 40 with window
- PLCC 44
- CQPJ 44 with window
- VQFP 44 (10x10)

PDIL 40 - Mechanical Outline

Figure 33. Plastic Dual In Line

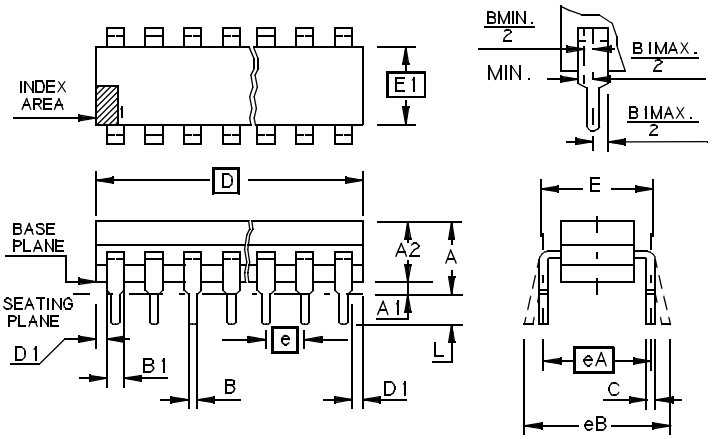


Table 57. PDIL Package Size

	MM		Inch	
	Min	**Max**	**Min**	**Max**
A	-	5.08	-	.200
A1	0.38	-	.015	-
A2	3.18	4.95	.125	.195
B	0.36	0.56	.014	.022
B1	0.76	1.78	.030	.070
C	0.20	0.38	.008	.015
D	50.29	53.21	1.980	2.095
E	15.24	15.87	.600	.625
E1	12.32	14.73	.485	.580
e	2.54 B.S.C.		.100 B.S.C.	
eA	15.24 B.S.C.		.600 B.S.C.	
eB	-	17.78	-	.700
L	2.93	3.81	.115	.150
D1	0.13	-	.005	-

CDIL 40 with Window - Mechanical Outline

Figure 34. Ceramic Dual In Line

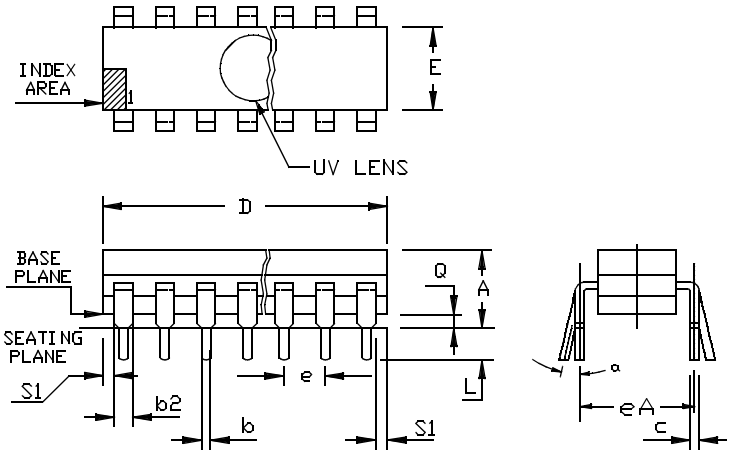


Table 58. CDIL Package Size

	MM		Inch	
	Min	**Max**	**Min**	**Max**
A	-	5.71	-	.225
b	0.36	0.58	.014	.023
b2	1.14	1.65	.045	.065
c	0.20	0.38	.008	.015
D	-	53.47	-	2.105
E	13.06	15.37	.514	.605
e	2.54 B.S.C.		.100 B.S.C.	
eA	15.24 B.S.C.		.600 B.S.C.	
L	3.18	5.08	.125	.200
Q	0.38	1.40	.015	.055
S1	0.13	-	.005	-
a	0 - 15		0 - 15	
N	40			

PLCC 44 - Mechanical Outline

Figure 35. Plastic Lead Chip Carrier

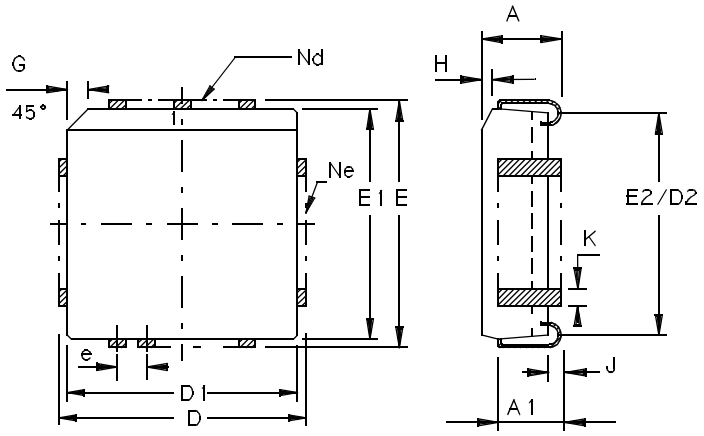


Table 59. PLCC Package Size

	MM		Inch	
	Min	**Max**	**Min**	**Max**
A	4.20	4.57	.165	.180
A1	2.29	3.04	.090	.120
D	17.40	17.65	.685	.695
D1	16.44	16.66	.647	.656
D2	14.99	16.00	.590	.630
E	17.40	17.65	.685	.695
E1	16.44	16.66	.647	.656
E2	14.99	16.00	.590	.630
e	1.27 BSC		.050 BSC	
G	1.07	1.22	.042	.048
H	1.07	1.42	.042	.056
J	0.51	-	.020	-
K	0.33	0.53	.013	.021
Nd	11		11	
Ne	11		11	

Ordering Information

AT/TSC80251G2D ROMless

Part Number	ROM	Description
High Speed Versions 4.5 to 5.5 V, Commercial and Industrial		
TSC80251G2D-16CB	ROMless	16 MHz, Commercial 0° to 70°C, PLCC 44
TSC80251G2D-24CB	ROMless	24 MHz, Commercial 0° to 70°C, PLCC 44
TSC80251G2D-24CE	ROMless	24 MHz, Commercial 0° to 70°C, VQFP 44
TSC80251G2D-24IA	ROMless	24 MHz, Industrial -40° to 85°C, PDIL 40
TSC80251G2D-24IB	ROMless	24 MHz, Industrial -40° to 85°C, PLCC 44
AT80251G2D-SLSUM	ROMless	24 MHz, Industrial & Green -40° to 85°C, PLCC 44
AT80251G2D-3CSUM	ROMless	24 MHz, Industrial & Green -40° to 85°C, PDIL 40
AT80251G2D-RLTUM	ROMless	24 MHz, Industrial & Green -40° to 85°C, VQFP 44
Low Voltage Versions 2.7 to 5.5 V		
TSC80251G2D-L16CB	ROMless	16 MHz, Commercial, PLCC 44
TSC80251G2D-L16CE	ROMless	16 MHz, Commercial, VQFP 44
AT80251G2D-SLSUL	ROMless	16 MHz, Industrial & Green, PLCC 44
AT80251G2D-RLTUL	ROMless	16 MHz, Industrial & Green, VQFP 44

AT/TSC83251G2D 32 kilobytes MaskROM

Part Number[1]	ROM	Description
High Speed Versions 4.5 to 5.5 V, Commercial and Industrial		
TSC251G2Dxxx-16CB	32K MaskROM	16 MHz, Commercial 0° to 70°C, PLCC 44
TSC251G2Dxxx-24CB	32K MaskROM	24 MHz, Commercial 0° to 70°C, PLCC 44
TSC251G2Dxxx-24CE	32K MaskROM	24 MHz, Commercial 0° to 70°C, VQFP 44
TSC251G2Dxxx-24IA	32K MaskROM	24 MHz, Industrial -40° to 85°C, PDIL 40
TSC251G2Dxxx-24IB	32K MaskROM	24 MHz, Industrial -40° to 85°C, PLCC 44
AT251G2Dxxx-SLSUM	32K MaskROM	24 MHz, Industrial & Green -40° to 85°C, PLCC 44
AT251G2Dxxx-3CSUM	32K MaskROM	24 MHz, Industrial & Green -40° to 85°C, PDIL 40
AT251G2Dxxx-RLTUM	32K MaskROM	24 MHz, Industrial & Green -40° to 85°C, VQFP 44
AT251G2Dxxx-SLSTM	32K MaskROM	24 MHz, Automotive & Green -40° to 85°C, PLCC 44

Options (Please consult Atmel sales)

- ROM code encryption
- Tape & Reel or Dry Pack
- Known good dice
- Extended temperature range: -55°C to +125°C

Product Markings

ROMless versions

ATMEL
Part number

YYWW . Lot Number

Mask ROM versions

ATMEL
Customer Part number

Part Number
YYWW . Lot Number

OTP versions

ATMEL
Part number

YYWW . Lot Number