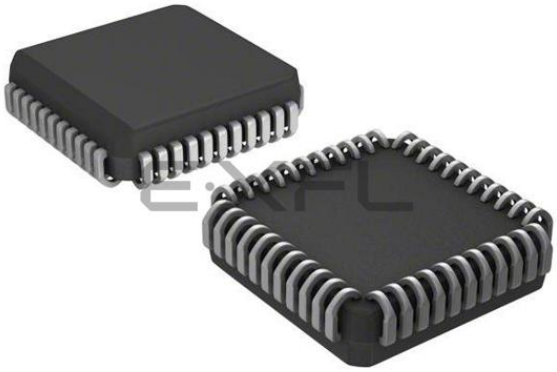

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C251
Core Size	8/16-Bit
Speed	16MHz
Connectivity	EBI/EMI, I²C, Microwire, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.6x16.6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/tsc87251g2d-l16cbr

Table 1. TSC80251G2D Pin Assignment

DIP	PLCC	VQFP	Name	DIP	PLCC	VQFP	Name
	1	39	VSS1		23	17	VSS2
1	2	40	P1.0/T2	21	24	18	P2.0/A8
2	3	41	P1.1/T2EX	22	25	19	P2.1/A9
3	4	42	P1.2/ECI	23	26	20	P2.2/A10
4	5	43	P1.3/CEX0	24	27	21	P2.3/A11
5	6	44	P1.4/CEX1/SS#	25	28	22	P2.4/A12
6	7	1	P1.5/CEX2/MISO	26	29	23	P2.5/A13
7	8	2	P1.6/CEX3/SCL/SCK/WAIT#	27	30	24	P2.6/A14
8	9	3	P1.7/A17/CEX4/SDA/MOSI/WCLK	28	31	25	P2.7/A15
9	10	4	RST	29	32	26	PSEN#
10	11	5	P3.0/RXD	30	33	27	ALE/PROG#
	12	6	AWAIT#		34	28	NMI
11	13	7	P3.1/TXD	31	35	29	EA#/VPP
12	14	8	P3.2/INT0#	32	36	30	P0.7/AD7
13	15	9	P3.3/INT1#	33	37	31	P0.6/AD6
14	16	10	P3.4/T0	34	38	32	P0.5/AD5
15	17	11	P3.5/T1	35	39	33	P0.4/AD4
16	18	12	P3.6/WR#	36	40	34	P0.3/AD3
17	19	13	P3.7/A16/RD#	37	41	35	P0.2/AD2
18	20	14	XTAL2	38	42	36	P0.1/AD1
19	21	15	XTAL1	39	43	37	P0.0/AD0
20	22	16	VSS	40	44	38	VDD

Table 2. Product Name Signal Description (Continued)

Signal Name	Type	Description	Alternate Function
NMI	I	**Non Maskable Interrupt** Holding this pin high for 24 oscillator periods triggers an interrupt. When using the Product Name as a pin-for-pin replacement for a 8xC51 product, NMI can be unconnected without loss of compatibility or power consumption increase (on-chip pull-down). Not available on DIP package.	–
P0.0:7	I/O	**Port 0** P0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. To avoid any paraitic current consumption, Floating P0 inputs must be polarized to V_{DD} or V_{SS}.	AD7:0
P1.0:7	I/O	**Port 1** P1 is an 8-bit bidirectional I/O port with internal pull-ups. P1 provides interrupt capability for a keyboard interface.	–
P2.0:7	I/O	**Port 2** P2 is an 8-bit bidirectional I/O port with internal pull-ups.	A15:8
P3.0:7	I/O	**Port 3** P3 is an 8-bit bidirectional I/O port with internal pull-ups.	–
PROG#	I	**Programming Pulse input** The programming pulse is applied to this input for programming the on-chip EPROM/OTPROM.	–
PSEN#	O	**Program Store Enable/Read signal output** PSEN# is asserted for a memory address range that depends on bits RD0 and RD1 in UCONFIG0 byte (see).	–
RD#	O	**Read or 17th Address Bit (A16)** Read signal output to external data memory depending on the values of bits RD0 and RD1 in UCONFIG0 byte (see Table 13, Page 20).	P3.7
RST	I	**Reset input to the chip** Holding this pin high for 64 oscillator periods while the oscillator is running resets the device. The Port pins are driven to their reset conditions when a voltage greater than V_{IH1} is applied, whether or not the oscillator is running. This pin has an internal pull-down resistor which allows the device to be reset by connecting a capacitor between this pin and VDD. Asserting RST when the chip is in Idle mode or Power-Down mode returns the chip to normal operation.	–
RXD	I/O	**Receive Serial Data** RXD sends and receives data in serial I/O mode 0 and receives data in serial I/O modes 1, 2 and 3.	P3.0
SCL	I/O	**TWI Serial Clock** When TWI controller is in master mode, SCL outputs the serial clock to slave peripherals. When TWI controller is in slave mode, SCL receives clock from the master controller.	P1.6
SCK	I/O	**SPI Serial Clock** When SPI is in master mode, SCK outputs clock to the slave peripheral. When SPI is in slave mode, SCK receives clock from the master controller.	P1.6
SDA	I/O	**TWI Serial Data** SDA is the bidirectional TWI data line.	P1.7
SS#	I	**SPI Slave Select Input** When in Slave mode, SS# enables the slave mode.	P1.4

Address Spaces

The TSC80251G2D derivatives implement four different address spaces:

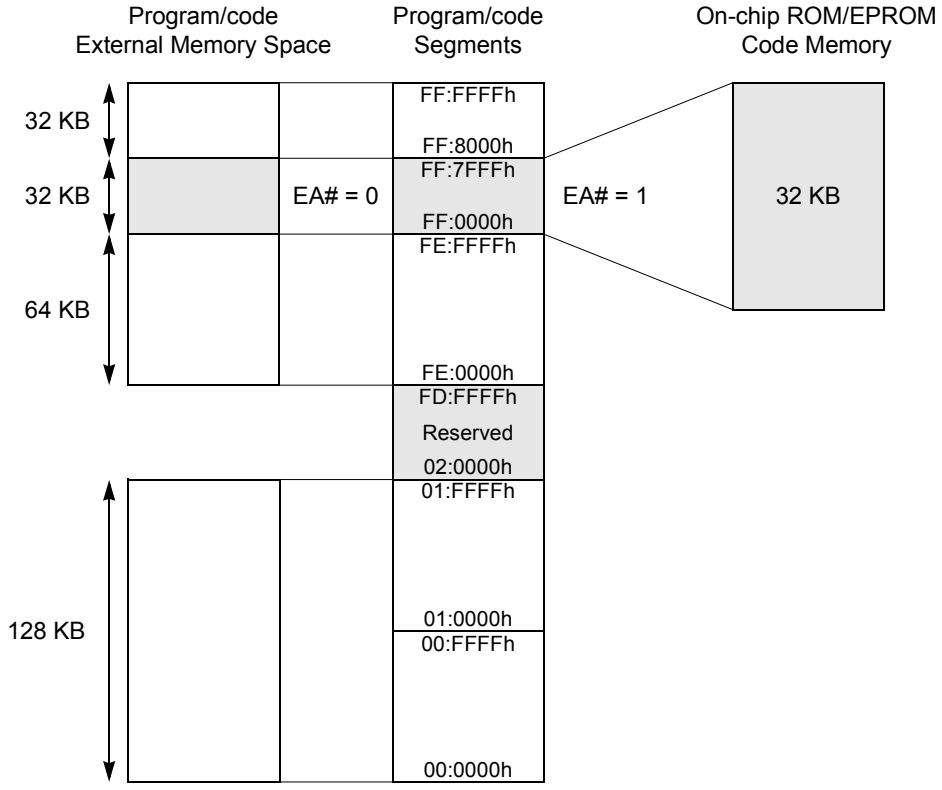
- On-chip ROM program/code memory (not present in ROMless devices)
- On-chip RAM data memory
- Special Function Registers (SFRs)
- Configuration array

Program/Code Memory

The TSC83251G2D and TSC87251G2D implement 32 KB of on-chip program/code memory. Figure 4 shows the split of the internal and external program/code memory spaces. If EA# is tied to a high level, the 32-Kbyte on-chip program memory is mapped in the lower part of segment FF: where the C251 core jumps after reset. The rest of the program/code memory space is mapped to the external memory. If EA# is tied to a low level, the internal program/code memory is not used and all the accesses are directed to the external memory.

The TSC83251G2D products provide the internal program/code memory in a masked ROM memory while the TSC87251G2D products provide it in an EPROM memory. For the TSC80251G2D products, there is no internal program/code memory and EA# must be tied to a low level.

Figure 4. Program/Code Memory Mapping



Note: Special care should be taken when the Program Counter (PC) increments:
If the program executes exclusively from on-chip code memory (not from external memory), beware of executing code from the upper eight bytes of the on-chip ROM (FF:7FF8h-FF:7FFFh). Because of its pipeline capability, the TSC80251G2D derivative may attempt to prefetch code from external memory (at an address above FF:7FFFh) and thereby disrupt I/O Ports 0 and 2. Fetching code constants from these 8 bytes does not affect Ports 0 and 2.
When PC reaches the end of segment FF:, it loops to the reset address FF:0000h (for

compatibility with the C51 Architecture). When PC increments beyond the end of segment FE:, it continues at the reset address FF:0000h (linearity). When PC increments beyond the end of segment 01:, it loops to the beginning of segment 00: (this prevents from its going into the reserved area).

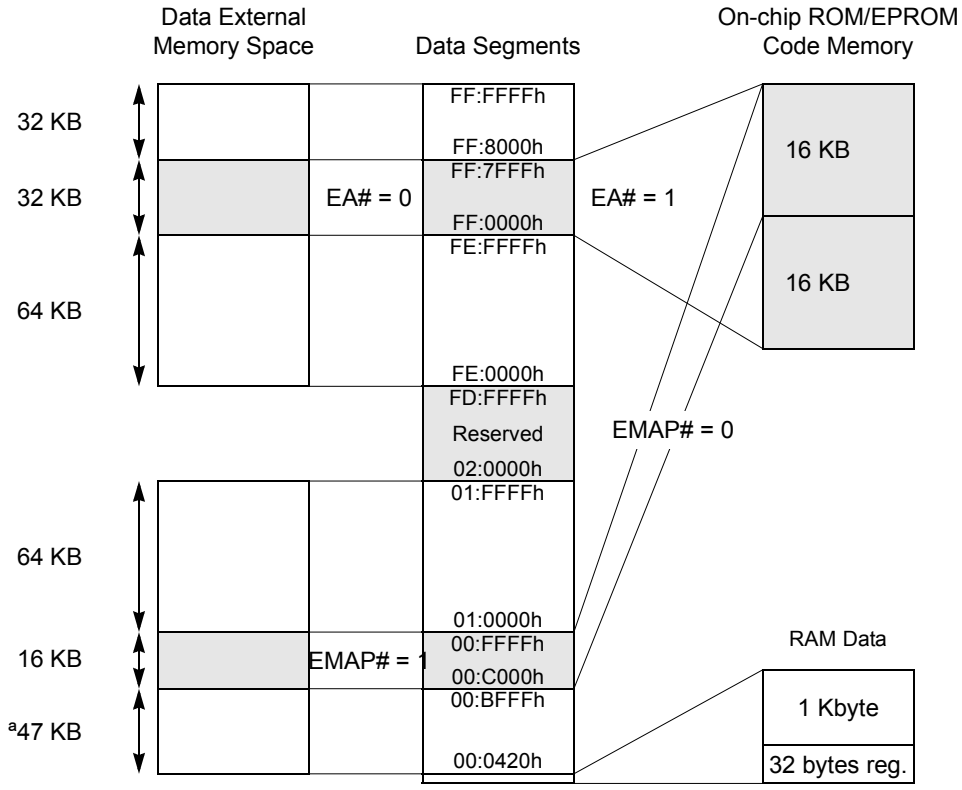
Data Memory

The TSC80251G2D derivatives implement 1 Kbyte of on-chip data RAM. Figure 5 shows the split of the internal and external data memory spaces. This memory is mapped in the data space just over the 32 bytes of registers area (see TSC80251 Programmers' Guide). Hence, the part of the on-chip RAM located from 20h to FFh is bit addressable. This on-chip RAM is not accessible through the program/code memory space.

For faster computation with the on-chip ROM/EPROM code of the TSC83251G2D/TSC87251G2D, its upper 16 KB are also mapped in the upper part of the region 00: if the On-Chip Code Memory Map configuration bit is cleared (EMAP# bit in UCONFIG1 byte, see Figure). However, if EA# is tied to a low level, the TSC80251G2D derivative is running as a ROMless product and the code is actually fetched in the corresponding external memory (i.e. the upper 16 KB of the lower 32 KB of the segment FF:). If EMAP# bit is set, the on-chip ROM is not accessible through the region 00:.

All the accesses to the portion of the data space with no on-chip memory mapped onto are redirected to the external memory.

Figure 5. Data Memory Mapping



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Special Function Registers

The Special Function Registers (SFRs) of the TSC80251G2D derivatives fall into the categories detailed in Table 1 to Table 9.

SFRs are placed in a reserved on-chip memory region S: which is not represented in the data memory mapping (Figure 5). The relative addresses within S: of these SFRs are provided together with their reset values in Table . They are upward compatible with the SFRs of the standard 80C51 and the Intel's 80C251Sx family. In this table, the C251 core registers are identified by Note 1 and are described in the TSC80251 Programmer's Guide. The other SFRs are described in the TSC80251G1D Design Guide. All the SFRs are bit-addressable using the C251 instruction set.

Table 1. C251 Core SFRs

Mnemonic	Name
ACC(1)	Accumulator
B(1)	B Register
PSW	Program Status Word
PSW1	Program Status Word 1
SP(1)	Stack Pointer - LSB of SPX

Mnemonic	Name
SPH(1)	Stack Pointer High - MSB of SPX
DPL(1)	Data Pointer Low byte - LSB of DPTR
DPH(1)	Data Pointer High byte - MSB of DPTR
DPXL(1)	Data Pointer Extended Low byte of DPX - Region number

Note: 1. These SFRs can also be accessed by their corresponding registers in the register file.

Table 2. I/O Port SFRs

Mnemonic	Name
P0	Port 0
P1	Port 1

Mnemonic	Name
P2	Port 2
P3	Port 3

Table 3. Timers SFRs

Mnemonic	Name
TL0	Timer/Counter 0 Low Byte
TH0	Timer/Counter 0 High Byte
TL1	Timer/Counter 1 Low Byte
TH1	Timer/Counter 1 High Byte
TL2	Timer/Counter 2 Low Byte
TH2	Timer/Counter 2 High Byte
TCON	Timer/Counter 0 and 1 Control

Mnemonic	Name
TMOD	Timer/Counter 0 and 1 Modes
T2CON	Timer/Counter 2 Control
T2MOD	Timer/Counter 2 Mode
RCAP2L	Timer/Counter 2 Reload/Capture Low Byte
RCAP2H	Timer/Counter 2 Reload/Capture High Byte
WDTRST	WatchDog Timer Reset

Table 10. SFR Descriptions

	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h		CH 0000 0000	CCAP0H 0000 0000	CCAP1H 0000 0000	CCAP2H 0000 0000	CCAP3H 0000 0000	CCAP4H 0000 0000		FFh
F0h	B(1) 0000 0000								F7h
E8h		CL 0000 0000	CCAP0L 0000 0000	CCAP1L 0000 0000	CCAP2L 0000 0000	CCAP3L 0000 0000	CCAP4L 0000 0000		EFh
E0h	ACC(1) 0000 0000								E7h
D8h	CCON 00X0 0000	CMOD 00XX X000	CCAPM0 X000 0000	CCAPM1 X000 0000	CCAPM2 X000 0000	CCAPM3 X000 0000	CCAPM4 X000 0000		DFh
D0h	PSW(1) 0000 0000	PSW1(1) 0000 0000							D7h
C8h	T2CON 0000 0000	T2MOD XXXX XX00	RCAP2L 0000 0000	RCAP2H 0000 0000	TL2 0000 0000	TH2 0000 0000			CFh
C0h									C7h
B8h	IPL0 X000 0000	SADEN 0000 0000					SPH(1) 0000 0000		BFh
B0h	P3 1111 1111	IE1 XX0X XXX0	IPL1 XX0X XXX0	IPH1 XX0X XXX0				IPH0 X000 0000	B7h
A8h	IE0 0000 0000	SADDR 0000 0000							AFh
A0h	P2 1111 1111						WDTRST 1111 1111	WCON XXXX XX00	A7h
98h	SCON 0000 0000	SBUF XXXX XXXX	BRL 0000 0000	BDRCON XXX0 0000	P1LS 0000 0000	P1IE 0000 0000	P1F 0000 0000		9Fh
90h	P1 1111 1111		SSBR 0000 0000	SSCON(2)	SSCS(3)	SSDAT 0000 0000	SSADR 0000 0000		97h
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	CKRL 0000 1000	POWM 0XXX XXXX	8Fh
80h	P0 1111 1111	SP(1) 0000 0111	DPL(1) 0000 0000	DPH(1) 0000 0000	DPXL(1) 0000 0001			PCON 0000 0000	87h
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

Reserved

Notes:
1. These registers are described in the TSC80251 Programmer's Guide (C251 core registers).
2. In TWI and SPI modes, SSCON is splitted in two separate registers. SSCON reset value is 0000 0000 in TWI mode and 0000 0100 in SPI mode.
3. In read and write modes, SSCS is splitted in two separate registers. SSCS reset value is 1111 1000 in read mode and 0000 0000 in write mode.

Table 16. Notation for Immediate Addressing

Immediate Address	Description	C251	C51
#data	An 8-bit constant that is immediately addressed in an instruction	3	3
#data16	A 16-bit constant that is immediately addressed in an instruction	3	–
#0data16 #1data16	A 32-bit constant that is immediately addressed in an instruction. The upper word is filled with zeros (#0data16) or ones (#1data16).	3	–
#short	A constant, equal to 1, 2, or 4, that is immediately addressed in an instruction.	3	–

Table 17. Notation for Bit Addressing

Direct Address	Description	C251	C51
bit51	A directly addressed bit (bit number = 00h-FFh) in memory or an SFR. Bits 00h-7Fh are the 128 bits in byte locations 20h-2Fh in the on-chip RAM. Bits 80h-FFh are the 128 bits in the 16 SFRs with addresses that end in 0h or 8h, S:80h, S:88h, S:90h,..., S:F0h, S:F8h.	–	3
bit	A directly addressed bit in memory locations 00:0020h-00:007Fh or in any defined SFR.	3	

Table 18. Notation for Destination in Control Instructions

Direct Address	Description	C251	C51
rel	A signed (two's complement) 8-bit relative address. The destination is -128 to +127 bytes relative to the next instruction's first byte.	3	3
addr11	An 11-bit target address. The target is in the same 2-Kbyte block of memory as the next instruction's first byte.	–	3
addr16	A 16-bit target address. The target can be anywhere within the same 64-Kbyte region as the next instruction's first byte.	–	3
addr24	A 24-bit target address. The target can be anywhere within the 16-Mbyte address space.	3	–

Add 3 if it addresses a Peripheral SFR.

5. If this instruction addresses an I/O Port (Px, x = 0-3), add 3 to the number of states. Add 5 if it addresses a Peripheral SFR.
6. In internal execution only, add 1 to the number of states of the 'jump taken' if the destination address is internal and odd.

Table 31. Summary of Unconditional Jump Instructions

Absolute jumpAJMP <src>(PC) ← (PC) +2; $(PC)_{10:0}$ ← src opnd						
Extended jumpEJMP <src>(PC) ← (PC) + size (instr); $(PC)_{23:0}$ ← src opnd						
Long jumpLJMP <src>(PC) ← (PC) + size (instr); $(PC)_{15:0}$ ← src opnd						
Short jumpSJMP rel(PC) ← (PC) +2; (PC) ← (PC) +rel						
Jump indirectJMP at A +DPTR$(PC)_{23:16}$ ← FFh; $(PC)_{15:0}$ ← (A) + (DPTR)						
No operationNOP(PC) ← (PC) +1						
Mnemonic	**<dest>, <src>(1)**	**Comments**	**Binary Mode**		**Source Mode**	
			Bytes	**States**	**Bytes**	**States**
AJMP	addr11	Absolute jump	2	3(2)(3)	2	3(2)(3)
EJMP	addr24	Extended jump	5	6(2)(4)	4	5(2)(4)
	at DRk	Extended jump (indirect)	3	7(2)(4)	2	6(2)(4)
LJMP	at WRj	Long jump (indirect)	3	6(2)(4)	2	5(2)(4)
	addr16	Long jump (direct address)	3	5(2)(4)	3	5(2)(4)
SJMP	rel	Short jump (relative address)	2	4(2)(4)	2	4(2)(4)
JMP	at A +DPTR	Jump indirect relative to the DPTR	1	5(2)(4)	1	5(2)(4)
NOP		No operation (Jump never)	1	1	1	1

Notes:
1. A shaded cell denotes an instruction in the C51 Architecture.
2. In internal execution only, add 1 to the number of states if the destination address is internal and odd.
3. Add 2 to the number of states if the destination address is external.
4. Add 3 to the number of states if the destination address is external.

Lock Bit System

The TSC87251G2D products implement 3 levels of security for User's program as described in Table 33. The TSC83251G2D products implement only the first level of security.

Level 0 is the level of an erased part and does not enable any security features.

Level 1 locks the programming of the User's internal Code Memory, the Configuration Bytes and the Encryption Array.

Level 2 locks the verifying of the User's internal Code Memory. It is always possible to verify the Configuration Bytes and the Lock Bits. It is not possible to verify the Encryption Array.

Level 3 locks the external execution.

Table 33. Lock Bits Programming

Level	Lock bits LB[2:0]	Internal Execution	External Execution	Verification	Programming	External PROM read (MOVC)
0	000	Enable	Enable	Enable(1)	Enable	Enable(2)
1	001	Enable	Enable	Enable(1)	Disable	Disable
2	01x(3)	Enable	Enable	Disable	Disable	Disable
3	1xx(3)	Enable	Disable	Disable	Disable	Disable

Notes: 1. Returns encrypted data if Encryption Array is programmed.
2. Returns non encrypted data.
3. x means don't care. Level 2 always enables level 1, and level 3 always enables levels 1 and 2.

The security level may be verified according to Table 34.

Table 34. Lock Bits Verifying

Level	Lock bits Data(1)
0	xxxxx000
1	xxxxx001
2	xxxxx01x
3	xxxxx1xx

Note: 1. x means don't care.

Encryption Array

The TSC83251G2D and TSC87251G2D products include a 128-byte Encryption Array located in non-volatile memory outside the memory address space. During verification of the on-chip code memory, the seven low-order address bits also address the Encryption Array. As the byte of the code memory is read, it is exclusive-NOR'ed (XNOR) with the key byte from the Encryption Array. If the Encryption Array is not programmed (still all 1s), the user program code is placed on the data bus in its original, unencrypted form. If the Encryption Array is programmed with key bytes, the user program code is encrypted and cannot be used without knowledge of the key byte sequence.

Table 39. Bus Cycles AC Timings; V_{DD} = 4.5 to 5.5 V, T_A = -40 to 85°C

Symbol	Parameter	12 MHz		16 MHz		24 MHz		Unit
		Min	Max	Min	Max	Min	Max	
T_{OSC}	$1/F_{OSC}$	83		62		41		ns
T_{LHLL}	ALE Pulse Width	78		58		38		ns(2)
T_{AVLL}	Address Valid to ALE Low	78		58		37		ns(2)
T_{LLAX}	Address hold after ALE Low	19		11		3		ns
T_{RLRH}(1)	RD#/PSEN# Pulse Width	162		121		78		ns(3)
T_{WLWH}	WR# Pulse Width	165		124		81		ns(3)
T_{LLRL}(1)	ALE Low to RD#/PSEN# Low	22		14		6		ns
T_{LHAX}	ALE High to Address Hold	99		70		40		ns(2)
T_{RLDV}(1)	RD#/PSEN# Low to Valid Data		146		104		61	ns(3)
T_{RHDX}(1)	Data Hold After RD#/PSEN# High	0		0		0		ns
T_{RHAX}(1)	Address Hold After RD#/PSEN# High	0		0		0		ns
T_{RLAZ}(1)	RD#/PSEN# Low to Address Float		0		0		0	ns
T_{RHDZ1}	Instruction Float After RD#/PSEN# High		45		40		30	ns
T_{RHDZ2}	Data Float After RD#/PSEN# High		215		165		115	ns
T_{RHLH1}	RD#/PSEN# high to ALE High (Instruction)	49		43		31		ns
T_{RHLH2}	RD#/PSEN# high to ALE High (Data)	215		169		115		ns
T_{WHLH}	WR# High to ALE High	215		169		115		ns
T_{AVDV1}	Address (P0) Valid to Valid Data In		250		175		105	ns(2)(3)
T_{AVDV2}	Address (P2) Valid to Valid Data In		306		223		140	ns(2)(3)
T_{AVDV3}	Address (P0) Valid to Valid Instruction In		150		109		68	ns(3)
T_{AXDX}	Data Hold after Address Hold	0		0		0		ns
T_{AVRL}(1)	Address Valid to RD# Low	100		70		40		ns(2)
T_{AVWL1}	Address (P0) Valid to WR# Low	100		70		40		ns(2)
T_{AVWL2}	Address (P2) Valid to WR# Low	158		115		74		ns(2)
T_{WHQX}	Data Hold after WR# High	90		69		32		ns
T_{QVWH}	Data Valid to WR# High	133		102		72		ns(3)
T_{WHAX}	WR# High to Address Hold	167		125		84		ns

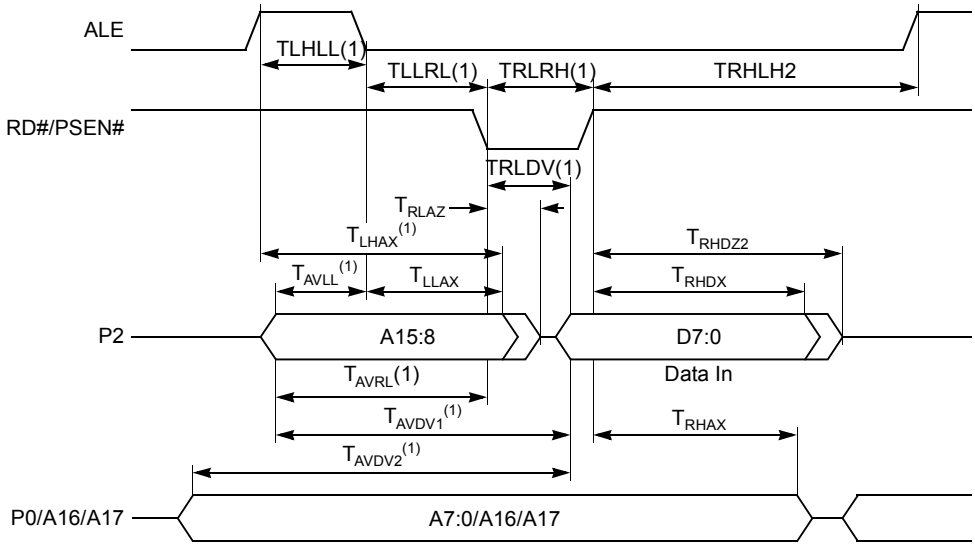
Notes:
1. Specification for PSEN# are identical to those for RD#.
2. If a wait state is added by extending ALE, add $2 \cdot T_{OSC.}$
3. If wait states are added by extending RD#/PSEN#/WR#, add $2N \cdot T_{OSC}$ (N = 1..3).

Table 40. Bus Cycles AC Timings; V_{DD} = 2.7 to 5.5 V, T_A = -40 to 85°C

Symbol	Parameter	12 MHz		16 MHz		Unit
		Min	Max	Min	Max	
T_{OSC}	$1/F_{OSC}$	83		62		ns
T_{LHLL}	ALE Pulse Width	72		52		ns(2)
T_{AVLL}	Address Valid to ALE Low	71		51		ns(2)
T_{LLAX}	Address hold after ALE Low	14		6		ns
T_{RLRH}(1)	RD#/PSEN# Pulse Width	163		121		ns(3)
T_{WLWH}	WR# Pulse Width	165		124		ns(3)
T_{LLRL}(1)	ALE Low to RD#/PSEN# Low	17		11		ns
T_{LHAX}	ALE High to Address Hold	90		57		ns(2)
T_{RLDV}(1)	RD#/PSEN# Low to Valid Data		133		92	ns(3)
T_{RHDX}(1)	Data Hold After RD#/PSEN# High	0		0		ns
T_{RHAX}(1)	Address Hold After RD#/PSEN# High	0		0		ns
T_{RLAZ}(1)	RD#/PSEN# Low to Address Float		0		0	ns
T_{RHDZ1}	Instruction Float After RD#/PSEN# High		59		48	ns
T_{RHDZ2}	Data Float After RD#/PSEN# High		225		175	ns
T_{RHLH1}	RD#/PSEN# high to ALE High (Instruction)	60		47		ns
T_{RHLH2}	RD#/PSEN# high to ALE High (Data)	226		172		ns
T_{WHLH}	WR# High to ALE High	226		172		ns
T_{AVDV1}	Address (P0) Valid to Valid Data In		289		160	ns(2)(3)
T_{AVDV2}	Address (P2) Valid to Valid Data In		296		211	ns(2)(3)
T_{AVDV3}	Address (P0) Valid to Valid Instruction In		144		98	ns(3)
T_{AXDX}	Data Hold after Address Hold	0		0		ns
T_{AVRL}(1)	Address Valid to RD# Low	111		64		ns(2)
T_{AVWL1}	Address (P0) Valid to WR# Low	111		64		ns(2)
T_{AVWL2}	Address (P2) Valid to WR# Low	158		116		ns(2)
T_{WHQX}	Data Hold after WR# High	82		66		ns
T_{QVWH}	Data Valid to WR# High	135		103		ns(3)
T_{WHAX}	WR# High to Address Hold	168		125		ns

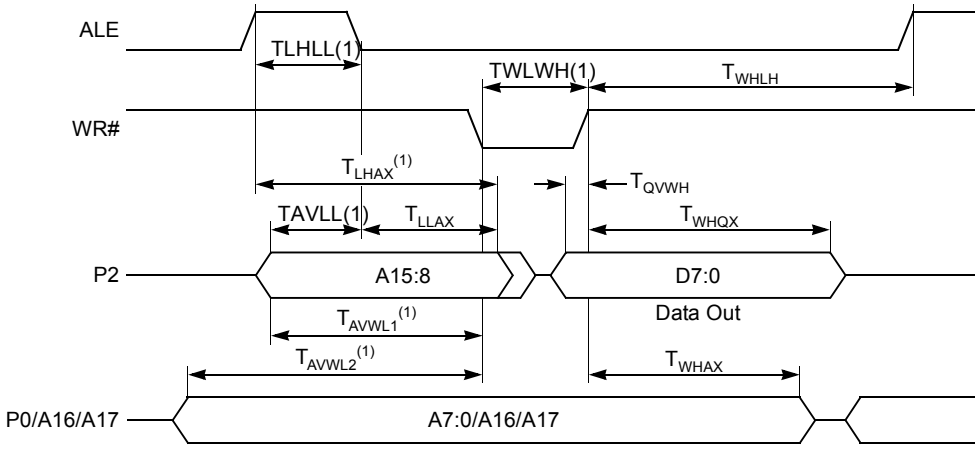
Notes: 1. Specification for PSEN# are identical to those for RD#.
2. If a wait state is added by extending ALE, add $2 \cdot T_{OSC.}$
3. If wait states are added by extending RD#/PSEN#/WR#, add $2N \cdot T_{OSC}$ (N = 1..3).

Figure 12. External Bus Cycle: Data Read (Page Mode)



Note: 1. The value of this parameter depends on wait states. See Table 39 and Table 40.

Figure 13. External Bus Cycle: Data Write (Page Mode)



Note: 1. The value of this parameter depends on wait states. See Table 39 and Table 40.

AC Characteristics - Real-Time Synchronous Wait State

Definition of Symbols

Table 41. Real-Time Synchronous Wait Timing Symbol Definitions

Signals	
C	WCLK
R	RD#/PSEN#
W	WR#
Y	WAIT#

Conditions	
L	Low
V	Valid
X	No Longer Valid

AC Characteristics - SSLC: SPI Interface

Definition of Symbols

Table 48. SPI Interface Timing Symbol Definitions

Signals	
C	Clock
I	Data In
O	Data Out
S	SS#

Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid
Z	Floating

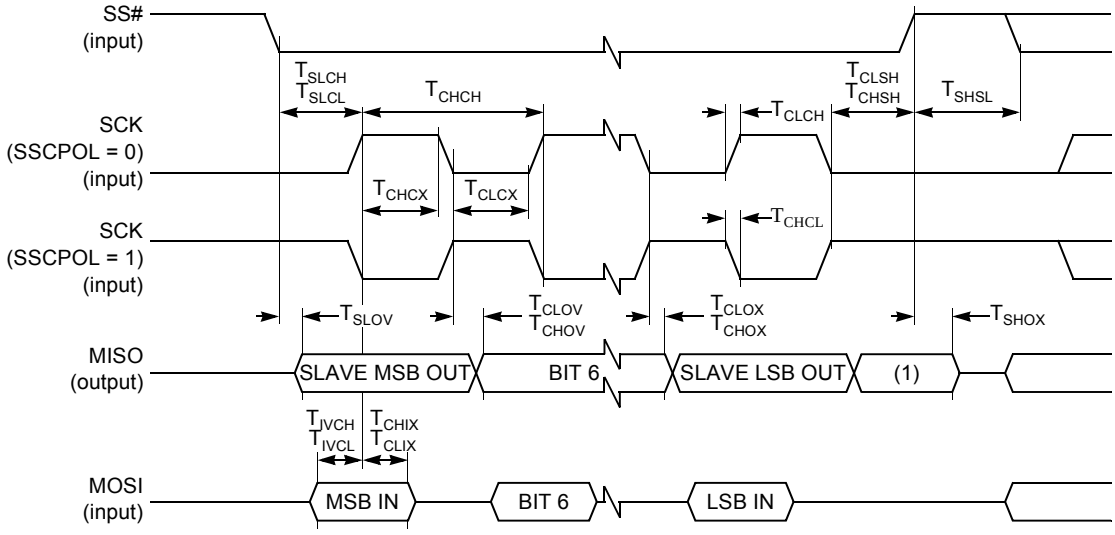
Timings

Table 49. SPI Interface AC Timing; V_{DD} = 2.7 to 5.5 V, T_A = -40 to 85°C

Symbol	Parameter	Min	Max	Unit
Slave Mode(1)				
T_{CHCH}	Clock Period	8		T_{OSC}
T_{CHCX}	Clock High Time	3.2		T_{OSC}
T_{CLCX}	Clock Low Time	3.2		T_{OSC}
T_{SLCH}, T_{SLCL}	SS# Low to Clock edge	200		ns
T_{IVCL}, T_{IVCH}	Input Data Valid to Clock Edge	100		ns
T_{CLIX}, T_{CHIX}	Input Data Hold after Clock Edge	100		ns
$T_{CLOV,}$ T_{CHOV}	Output Data Valid after Clock Edge		100	ns
T_{CLOX}, T_{CHOX}	Output Data Hold Time after Clock Edge	0		ns
T_{CLSH}, T_{CHSH}	SS# High after Clock Edge	0		ns
T_{IVCL}, T_{IVCH}	Input Data Valid to Clock Edge	100		ns
T_{CLIX}, T_{CHIX}	Input Data Hold after Clock Edge	100		ns
T_{SLOV}	SS# Low to Output Data Valid		130	ns
T_{SHOX}	Output Data Hold after SS# High		130	ns
T_{SHSL}	SS# High to SS# Low	(2)		
T_{ILIH}	Input Rise Time		2	µs
T_{IHIL}	Input Fall Time		2	µs
T_{OLOH}	Output Rise time		100	ns
T_{OHOL}	Output Fall Time		100	ns
Master Mode(3)				
T_{CHCH}	Clock Period	4		T_{OSC}
T_{CHCX}	Clock High Time	1.6		T_{OSC}
T_{CLCX}	Clock Low Time	1.6		T_{OSC}
T_{IVCL}, T_{IVCH}	Input Data Valid to Clock Edge	50		ns
T_{CLIX}, T_{CHIX}	Input Data Hold after Clock Edge	50		ns
$T_{CLOV,}$ T_{CHOV}	Output Data Valid after Clock Edge		65	ns
T_{CLOX}, T_{CHOX}	Output Data Hold Time after Clock Edge	0		ns
T_{ILIH}	Input Data Rise Time		2	µs
T_{IHIL}	Input Data Fall Time		2	µs
T_{OLOH}	Output Data Rise time		50	ns
T_{OHOL}	Output Data Fall Time		50	ns

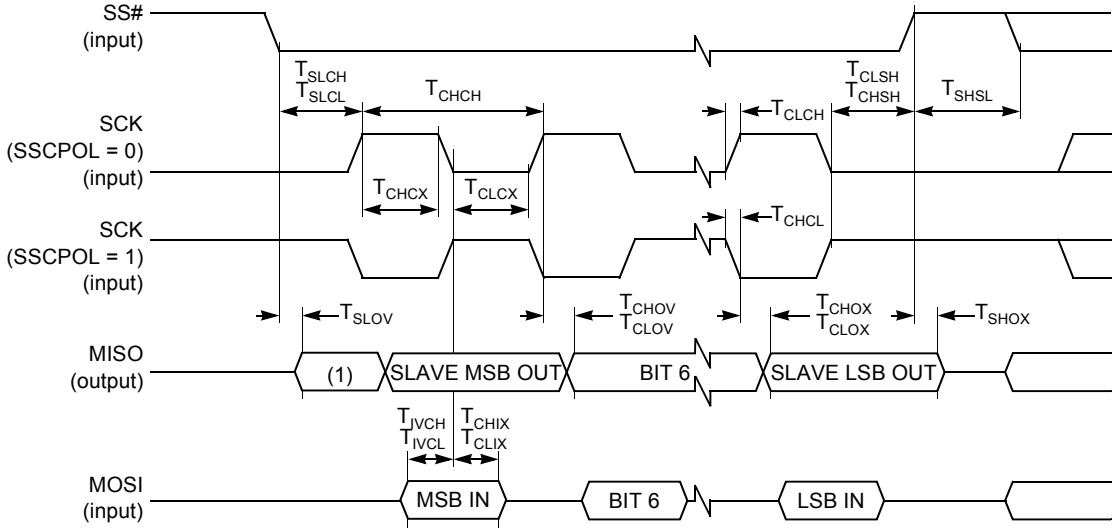
Notes: 1. Capacitive load on all pins = 200 pF in slave mode.
2. The value of this parameter depends on software.
3. Capacitive load on all pins = 100 pF in master mode.

Figure 21. SPI Slave Waveforms (SSCPHA = 0)



Note: 1. Not Defined but generally the LSB of the character which has just been received.

Figure 22. SPI Slave Waveforms (SSCPHA = 1)



AC Characteristics - EPROM Programming and Verifying

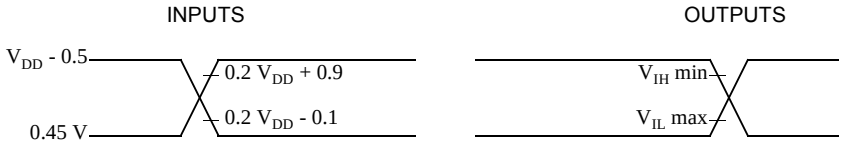
Definition of Symbols

Table 50. EPROM Programming and Verifying Timing Symbol Definitions

Signals	
A	Address
E	Enable: mode set on Port 0
G	Program
Q	Data Out
S	Supply (V_{PP})

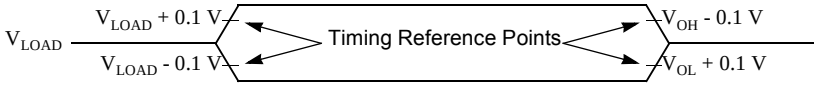
Conditions	
H	High
L	Low
V	Valid
X	No Longer Valid
Z	Floating

Figure 26. AC Testing Input/Output Waveforms



Note: For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loading V_{OH}/V_{OL} level occurs with I_{OL}/I_{OH} = ±20 mA.

Figure 27. Float Waveforms



Notes: 1. Under steady-state (non-transient) conditions, I_{OL} must be externally limited as follows:

Maximum IOL per port pin: 10 mA

Maximum IOL per 8-bit port:Port 0 26 mA

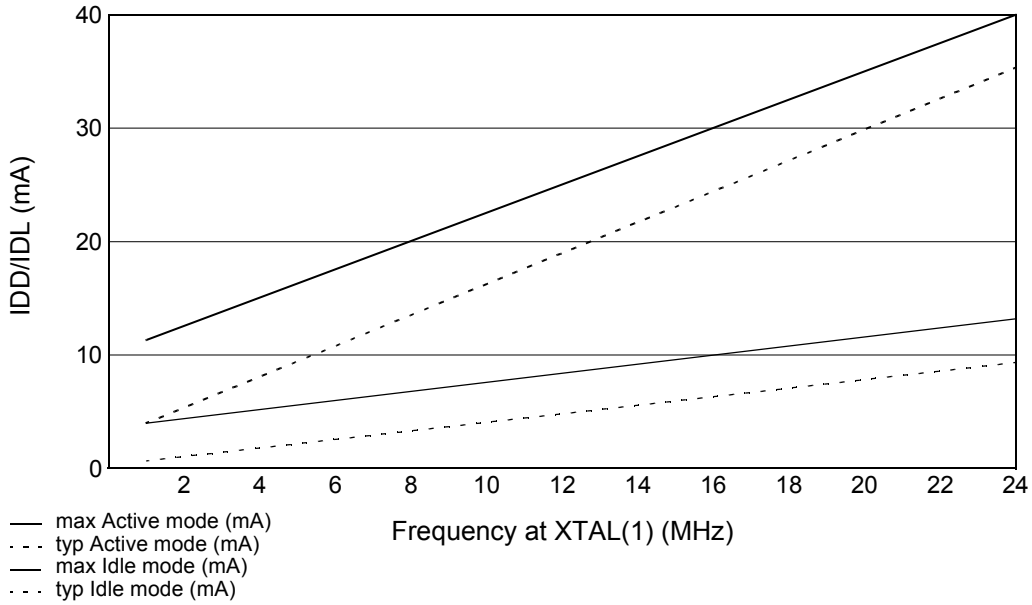
Ports 1-3 15 mA

Maximum Total IOL for all: Output Pins 71 mA

If IOL exceeds the test conditions, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

2. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses above 0.4 V on the low-level outputs of ALE and Ports 1, 2, and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins change from high to low. In applications where capacitive loading exceeds 100 pF, the noise pulses on these signals may exceed 0.8 V. It may be desirable to qualify ALE or other signals with a Schmitt Trigger or CMOS-level input logic.
3. Capacitive loading on Ports 0 and 2 causes the V_{OH} on ALE and PSEN# to drop below the specification when the address lines are stabilizing.
4. Typical values are obtained using V_{DD} = 5 V and T_A = 25°C. They are not tested and there is not guarantee on these values.
5. The input threshold voltage of SCL and SDA meets the TWI specification, so an input voltage below $0.3 \cdot V_{DD}$ will be recognized as a logic 0 while an input voltage above $0.7 \cdot V_{DD}$ will be recognized as a logic 1.

Figure 28. I_{DD}/I_{DL} Versus Frequency; V_{DD} = 4.5 to 5.5 V



Note: 1. The clock prescaler is not used: $F_{OSC} = F_{XTAL}$.

Low Voltage Versions - Commercial & Industrial

Table 56. DC Characteristics; V_{DD} = 2.7 to 5.5 V, T_A = -40 to +85°C

Symbol	Parameter	Min	Typical[4]	Max	Units	Test Conditions
V_{IL}	Input Low Voltage (except EA#, SCL, SDA)	-0.5		$0.2 \cdot V_{DD}$ - 0.1	V	
V_{IL1}[5]	Input Low Voltage (SCL, SDA)	-0.5		$0.3 \cdot V_{DD}$	V	
V_{IL2}	Input Low Voltage (EA#)	0		$0.2 \cdot V_{DD}$ - 0.3	V	
V_{IH}	Input high Voltage (except XTAL1, RST, SCL, SDA)	$0.2 \cdot V_{DD}$ + 0.9		V_{DD} + 0.5	V	
V_{IH1}[5]	Input high Voltage (XTAL1, RST, SCL, SDA)	$0.7 \cdot V_{DD}$		V_{DD} + 0.5	V	
V_{OL}	Output Low Voltage (Ports 1, 2, 3)			0.45	V	I_{OL} = 0.8 mA[1][2]
V_{OL1}	Output Low Voltage (Ports 0, ALE, PSEN#, Port 2 in Page Mode during External Address)			0.45	V	I_{OL} = 1.6 mA[1][2]
V_{OH}	Output high Voltage (Ports 1, 2, 3, ALE, PSEN#)	$0.9 \cdot V_{DD}$			V	I_{OH} = -10 µA[3]
V_{OH1}	Output high Voltage (Port 0, Port 2 in Page Mode during External Address)	$0.9 \cdot V_{DD}$			V	I_{OH} = -40 µA
V_{RET}	V_{DD} data retention limit			1.8	V	
I_{IL0}	Logical 0 Input Current (Ports 1, 2, 3 - AWAIT#)			- 50	µA	V_{IN} = 0.45 V
I_{IL1}	Logical 1 Input Current (NMI)			+ 50	µA	$V_{IN} = V_{DD}$
I_{LI}	Input Leakage Current (Port 0)			± 10	µA	0.45 V < V_{IN} < V_{DD}
I_{TL}	Logical 1-to-0 Transition Current (Ports 1, 2, 3)			- 650	µA	V_{IN} = 2.0 V
R_{RST}	RST Pull-Down Resistor	40	110	225	kΩ	
C_{IO}	Pin Capacitance		10		pF	T_A = 25°C
I_{DD}	Operating Current		4 8 9 11	8 11 12 14	mA	5 MHz, V_{DD} < 3.6 V 10 MHz, V_{DD} < 3.6 V 12 MHz, V_{DD} < 3.6 V 16 MHz, V_{DD} < 3.6 V
I_{DL}	Idle Mode Current		0.5 1.5 2 3	1 4 5 7	mA	5 MHz, V_{DD} < 3.6 V 10 MHz, V_{DD} < 3.6 V 12 MHz, V_{DD} < 3.6 V 16 MHz, V_{DD} < 3.6 V
I_{PD}	Power-Down Current		1	10	µA	V_{RET} < V_{DD} < 3.6 V

Notes: 1. Under steady-state (non-transient) conditions, I_{OL} must be externally limited as follows:

Maximum IOL per port pin: 10 mA

Maximum IOL per 8-bit port: Port 0 26 mA

Ports 1-315 mA

PLCC 44 - Mechanical Outline

Figure 35. Plastic Lead Chip Carrier

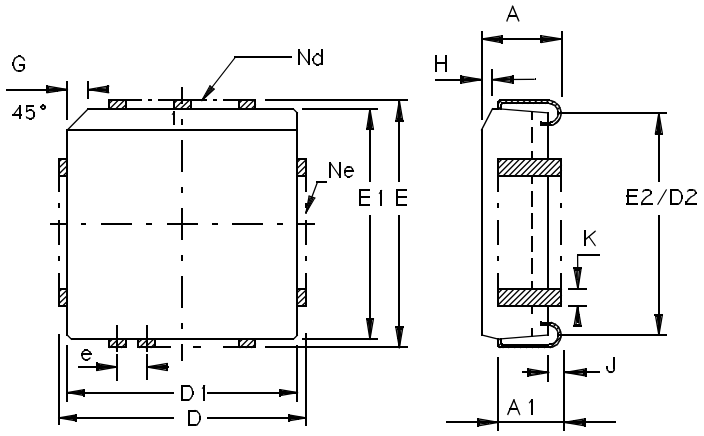


Table 59. PLCC Package Size

	MM		Inch	
	Min	**Max**	**Min**	**Max**
A	4.20	4.57	.165	.180
A1	2.29	3.04	.090	.120
D	17.40	17.65	.685	.695
D1	16.44	16.66	.647	.656
D2	14.99	16.00	.590	.630
E	17.40	17.65	.685	.695
E1	16.44	16.66	.647	.656
E2	14.99	16.00	.590	.630
e	1.27 BSC		.050 BSC	
G	1.07	1.22	.042	.048
H	1.07	1.42	.042	.056
J	0.51	-	.020	-
K	0.33	0.53	.013	.021
Nd	11		11	
Ne	11		11	

VQFP 44 (10x10) - Mechanical Outline

Figure 37. Shrink Quad Flat Pack (Plastic)

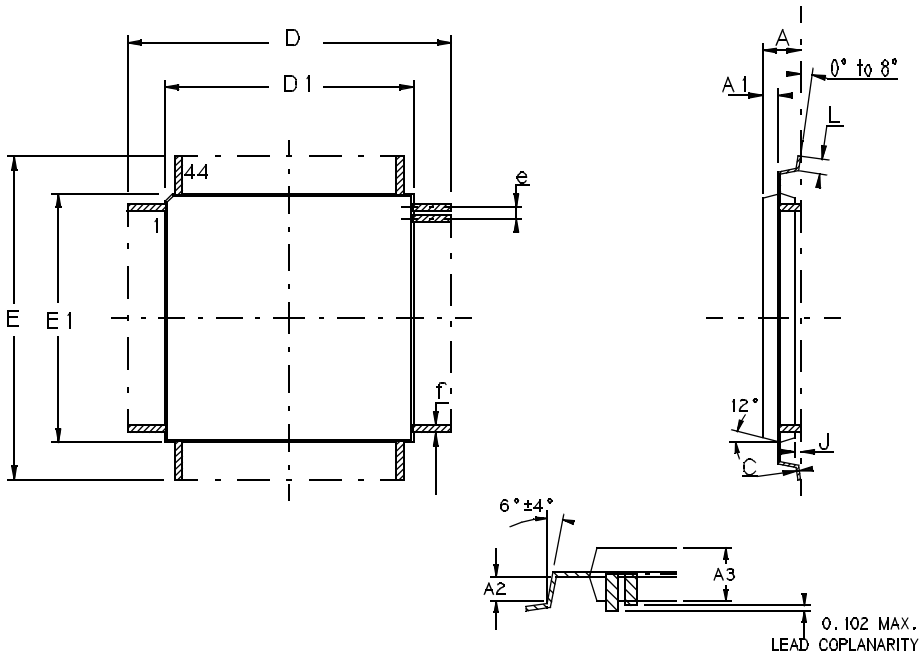


Table 61. VQFP Package Size

	MM		Inch	
	Min	**Max**	**Min**	**Max**
A	-	1.60	-	.063
A1	0.64 REF		.025 REF	
A2	0.64 REF		.025REF	
A3	1.35	1.45	.053	.057
D	11.90	12.10	.468	.476
D1	9.90	10.10	.390	.398
E	11.90	12.10	.468	.476
E1	9.90	10.10	.390	.398
J	0.05	-	.002	6
L	0.45	0.75	.018	.030
e	0.80 BSC		.0315 BSC	
f	0.35 BSC		.014 BSC	