What is "**Embedded - Microcontrollers**"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "**Embedded - Microcontrollers**"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	13
Program Memory Size	896B (512 x 14)
Program Memory Type	FLASH
EEPROM Size	64 x 8
RAM Size	36 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	18-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f83-04-p

PIC16F8X

PIC16CXX devices contain an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8-bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the working register (W register), and the other operand is a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a $\overline{\text{borrow}}$ and $\overline{\text{digit borrow}}$ out bit, respectively, in subtraction. See the SUBLW and SUBWF instructions for examples.

A simplified block diagram for the PIC16F8X is shown in Figure 3-1, its corresponding pin description is shown in Table 3-1.

FIGURE 3-1:   PIC16F8X BLOCK DIAGRAM
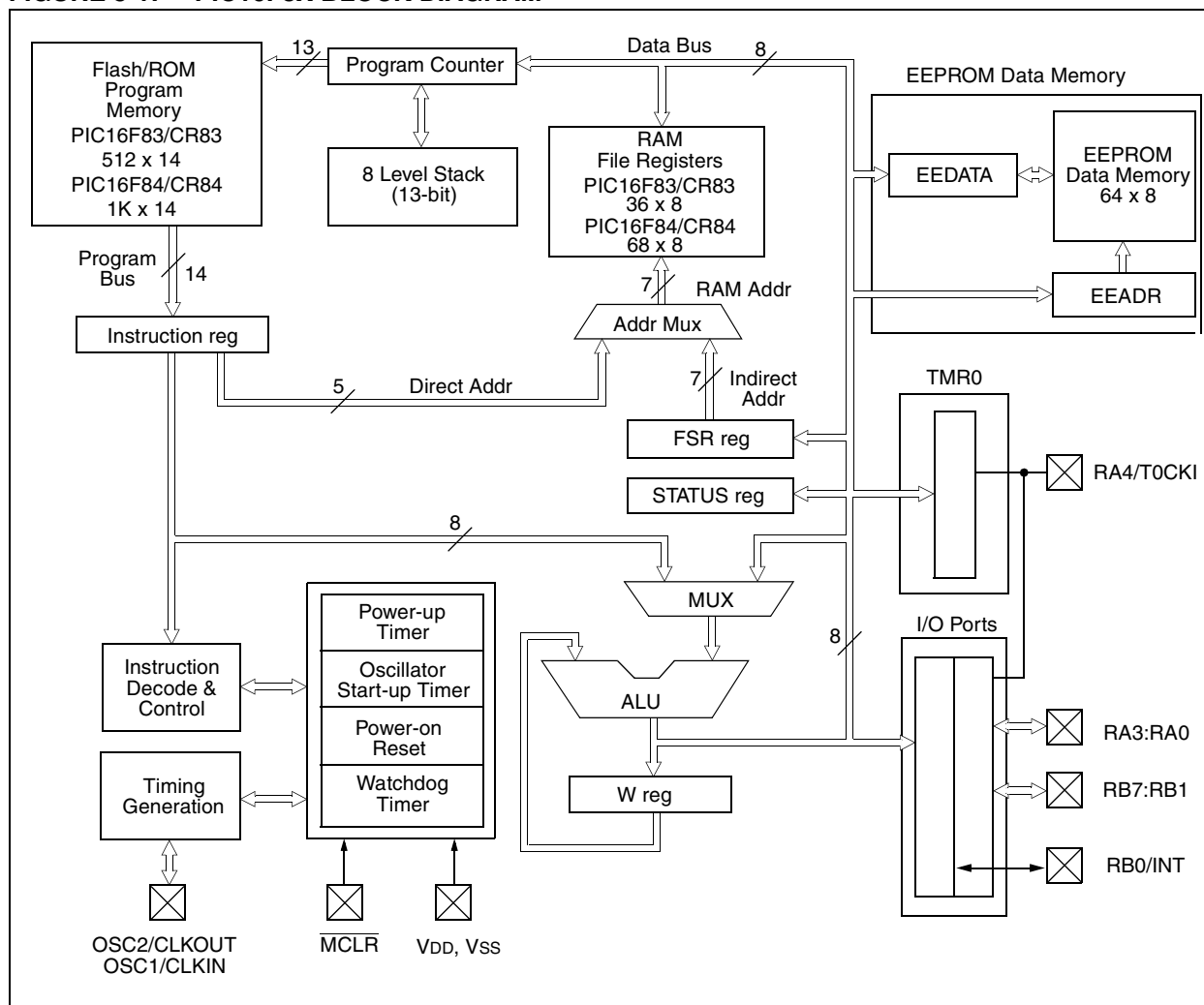
PIC16F8X

3.1 Clocking Scheme/Instruction Cycle

The clock input (from OSC1) is internally divided by four to generate four non-overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, the program counter (PC) is incremented every Q1, the instruction is fetched from the program memory and latched into the instruction register in Q4. The instruction is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3-2.

3.2 Instruction Flow/Pipelining

An "Instruction Cycle" consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., GOTO) then two cycles are required to complete the instruction (Example 3-1).

A fetch cycle begins with the Program Counter (PC) incrementing in Q1.
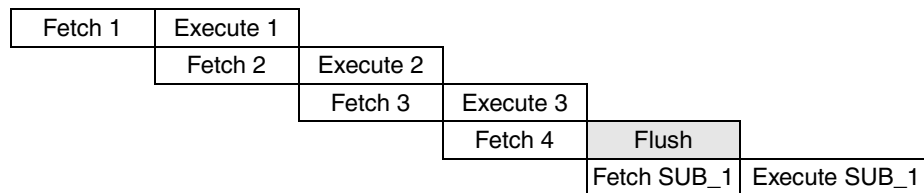
In the execution cycle, the fetched instruction is latched into the "Instruction Register" in cycle Q1. This instruction is then decoded and executed during the Q2, Q3, and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 3-2: CLOCK/INSTRUCTION CYCLE
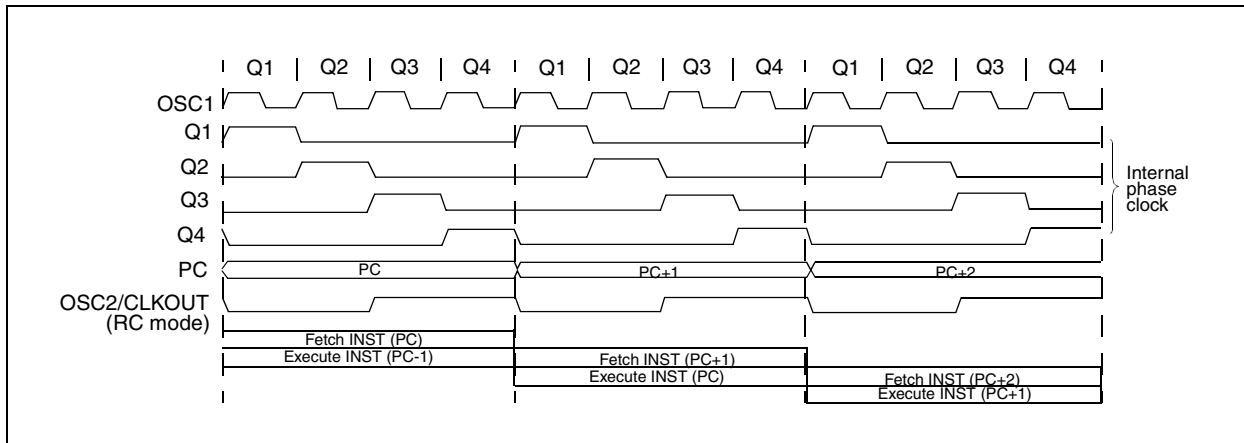
EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW


```
1. MOVLW 55h
2. MOVWF PORTB
3. CALL SUB_1
4. BSF  PORTA, BIT3
```

|	Fetch 1	Execute 1				
		Fetch 2	Execute 2			
			Fetch 3	Execute 3		
				Fetch 4	Flush	
					Fetch SUB_1	Execute SUB_1

All instructions are single cycle, except for any program branches. These take two cycles since the fetch instruction is "flushed" from the pipeline while the new instruction is being fetched and then executed.

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4.3   Program Counter: PCL and PCLATH

The Program Counter (PC) is 13-bits wide. The low byte is the PCL register, which is a readable and writable register. The high byte of the PC (PC<12:8>) is not directly readable nor writable and comes from the PCLATH register. The PCLATH (PC latch high) register is a holding register for PC<12:8>. The contents of PCLATH are transferred to the upper byte of the program counter when the PC is loaded with a new value. This occurs during a CALL, GOTO or a write to PCL. The high bits of PC are loaded from PCLATH as shown in Figure 4-1.

FIGURE 4-1:   LOADING OF PC IN DIFFERENT SITUATIONS
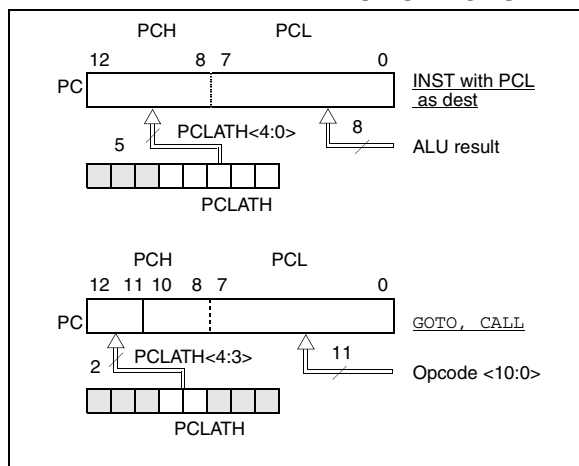
4.3.1   COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When doing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256 word block). Refer to the application note *"Implementing a Table Read"* (AN556).

4.3.2   PROGRAM MEMORY PAGING

The PIC16F83 and PIC16CR83 have 512 words of program memory. The PIC16F84 and PIC16CR84 have 1K of program memory. The CALL and GOTO instructions have an 11-bit address range. This 11-bit address range allows a branch within a 2K program memory page size. For future PIC16F8X program memory expansion, there must be another two bits to specify the program memory page. These paging bits come from the PCLATH<4:3> bits (Figure 4-1). When doing a CALL or a GOTO instruction, the user must ensure that these page bits (PCLATH<4:3>) are programmed to the desired program memory page. If a CALL instruction (or interrupt) is executed, the entire 13-bit PC is "pushed" onto the stack (see next section). Therefore,

manipulation of the PCLATH<4:3> is not required for the return instructions (which "pops" the PC from the stack).

Note:	The PIC16F8X ignores the PCLATH<4:3> bits, which are used for program memory pages 1, 2 and 3 (0800h - 1FFFh). The use of PCLATH<4:3> as general purpose R/W bits is not recommended since this may affect upward compatibility with future products.

4.4   Stack

The PIC16FXX has an 8 deep x 13-bit wide hardware stack (Figure 4-1). The stack space is not part of either program or data space and the stack pointer is not readable or writable.

The entire 13-bit PC is "pushed" onto the stack when a CALL instruction is executed or an interrupt is acknowledged. The stack is "popped" in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a push or a pop operation.

Note:	There are no instruction mnemonics called push or pop. These are actions that occur from the execution of the CALL, RETURN, RETLW, and RETFIE instructions, or the vectoring to an interrupt address.

The stack operates as a circular buffer. That is, after the stack has been pushed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

If the stack is effectively popped nine times, the PC value is the same as the value from the first pop.

Note:	There are no status bits to indicate stack overflow or stack underflow conditions.

5.3 I/O Programming Considerations

5.3.1 BI-DIRECTIONAL I/O PORTS

Any instruction which writes, operates internally as a read followed by a write operation. The BCF and BSF instructions, for example, read the register into the CPU, execute the bit operation and write the result back to the register. Caution must be used when these instructions are applied to a port with both inputs and outputs defined. For example, a BSF operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU. Then the BSF operation takes place on bit5 and PORTB is written to the output latches. If another bit of PORTB is used as a bi-directional I/O pin (i.e., bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit0 is switched into output mode later on, the content of the data latch is unknown.

Reading the port register, reads the values of the port pins. Writing to the port register writes the value to the port latch. When using read-modify-write instructions (i.e., BCF, BSF, etc.) on a port, the value of the port pins is read, the desired operation is done to this value, and this value is then written to the port latch.

A pin actively outputting a Low or High should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output current may damage the chip.

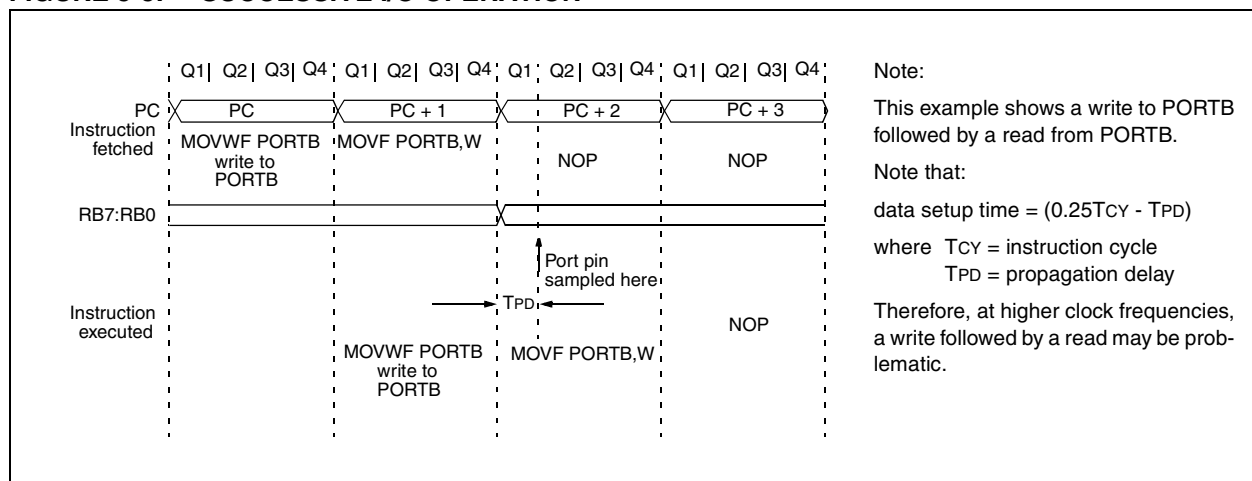### 5.3.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 5-5). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should be such that the pin voltage stabilizes (load dependent) before the next instruction which causes that file to be read into the CPU is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.

Example 5-1 shows the effect of two sequential read-modify-write instructions (e.g., BCF, BSF, etc.) on an I/O port.

EXAMPLE 5-1: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

```
;Initial PORT settings: PORTB<7:4> Inputs
;                       PORTB<3:0> Outputs
;PORTB<7:6> have external pull-ups and are
;not connected to other circuitry
;
;                   PORT latch   PORT pins
;                   ----------   ---------
  BCF PORTB, 7    ; 01pp ppp     11pp ppp
  BCF PORTB, 6    ; 10pp ppp     11pp ppp
  BSF STATUS, RP0 ;
  BCF TRISB, 7    ; 10pp ppp     11pp ppp
  BCF TRISB, 6    ; 10pp ppp     10pp ppp
;
;Note that the user may have expected the
;pin values to be 00pp ppp. The 2nd BCF
;caused RB7 to be latched as the pin value
;(high).
```
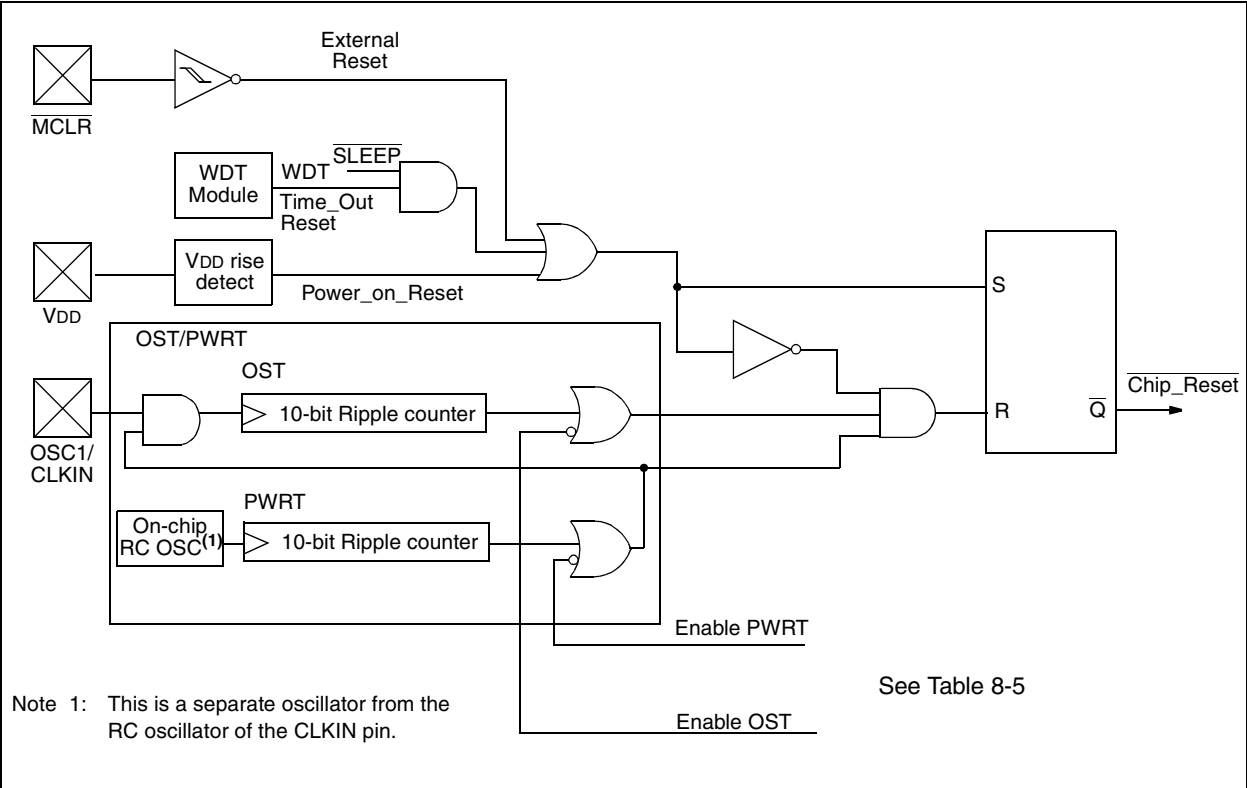
FIGURE 5-5: SUCCESSIVE I/O OPERATION

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FIGURE 6-5:   TIMER0 TIMING WITH EXTERNAL CLOCK

Ext. Clock Input or
Prescaler Out (Note 2)

Ext. Clock/Prescaler
Output After Sampling

Increment TMR0 (Q4)

TMR0

T0   T0 + 1   T0 + 2

(Note 3)

Note 1: Delay from clock input change to TMR0 increment is 3Tosc to 7Tosc. (Duration of Q = Tosc).
         Therefore, the error in measuring the interval between two edges on TMR0 input = ± 4Tosc max.
     2: External clock if no prescaler selected, Prescaler output otherwise.
     3: The arrows ↑ indicate where sampling occurs. A small clock pulse may be missed by sampling.

FIGURE 6-6:   BLOCK DIAGRAM OF THE TMR0/WDT PRESCALER

CLKOUT (= Fosc/4)

Data Bus

RA4/T0CKI
pin

T0SE

T0CS

MUX 0/1

MUX 1/0

PSA

SYNC
2
Cycles

TMR0 register

8

Set bit T0IF
on overflow

Watchdog
Timer

MUX 0/1

8-bit Prescaler

8

PSA

8 - to - 1MUX

PS2:PS0

WDT Enable bit

M U X 0/1

PSA

WDT
time-out

Note: T0CS, T0SE, PSA, PS2:PS0 are bits in the OPTION_REG register.

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FIGURE 8-8: **SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT**

Note 1: This is a separate oscillator from the RC oscillator of the CLKIN pin.

See Table 8-5

TABLE 8-3   RESET CONDITION FOR PROGRAM COUNTER AND THE STATUS REGISTER

Condition	Program Counter	STATUS Register
Power-on Reset	000h	`0001 1xxx`
$\overline{\text{MCLR}}$ Reset during normal operation	000h	`000u uuuu`
$\overline{\text{MCLR}}$ Reset during SLEEP	000h	`0001 0uuu`
WDT Reset (during normal operation)	000h	`0000 1uuu`
WDT Wake-up	PC + 1	`uuu0 0uuu`
Interrupt wake-up from SLEEP	PC + 1 [1]	`uuu1 0uuu`

Legend: `u` = unchanged, `x` = unknown.
Note 1:   When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

TABLE 8-4   RESET CONDITIONS FOR ALL REGISTERS

Register	Address	Power-on Reset	$\overline{\text{MCLR}}$ Reset during: – normal operation – SLEEP WDT Reset during normal operation	Wake-up from SLEEP: – through interrupt – through WDT Time-out
W	—	`xxxx xxxx`	`uuuu uuuu`	`uuuu uuuu`
INDF	00h	`---- ----`	`---- ----`	`---- ----`
TMR0	01h	`xxxx xxxx`	`uuuu uuuu`	`uuuu uuuu`
PCL	02h	`0000h`	`0000h`	PC + 1 [2]
STATUS	03h	`0001 1xxx`	`000q quuu` [3]	`uuuq quuu` [3]
FSR	04h	`xxxx xxxx`	`uuuu uuuu`	`uuuu uuuu`
PORTA	05h	`---x xxxx`	`---u uuuu`	`---u uuuu`
PORTB	06h	`xxxx xxxx`	`uuuu uuuu`	`uuuu uuuu`
EEDATA	08h	`xxxx xxxx`	`uuuu uuuu`	`uuuu uuuu`
EEADR	09h	`xxxx xxxx`	`uuuu uuuu`	`uuuu uuuu`
PCLATH	0Ah	`---0 0000`	`---0 0000`	`---u uuuu`
INTCON	0Bh	`0000 000x`	`0000 000u`	`uuuu uuuu` [1]
INDF	80h	`---- ----`	`---- ----`	`---- ----`
OPTION_REG	81h	`1111 1111`	`1111 1111`	`uuuu uuuu`
PCL	82h	`0000h`	`0000h`	PC + 1
STATUS	83h	`0001 1xxx`	`000q quuu` [3]	`uuuq quuu` [3]
FSR	84h	`xxxx xxxx`	`uuuu uuuu`	`uuuu uuuu`
TRISA	85h	`---1 1111`	`---1 1111`	`---u uuuu`
TRISB	86h	`1111 1111`	`1111 1111`	`uuuu uuuu`
EECON1	88h	`---0 x000`	`---0 q000`	`---0 uuuu`
EECON2	89h	`---- ----`	`---- ----`	`---- ----`
PCLATH	8Ah	`---0 0000`	`---0 0000`	`---u uuuu`
INTCON	8Bh	`0000 000x`	`0000 000u`	`uuuu uuuu` [1]

Legend: `u` = unchanged,   `x` = unknown,   `-` = unimplemented bit read as '0',
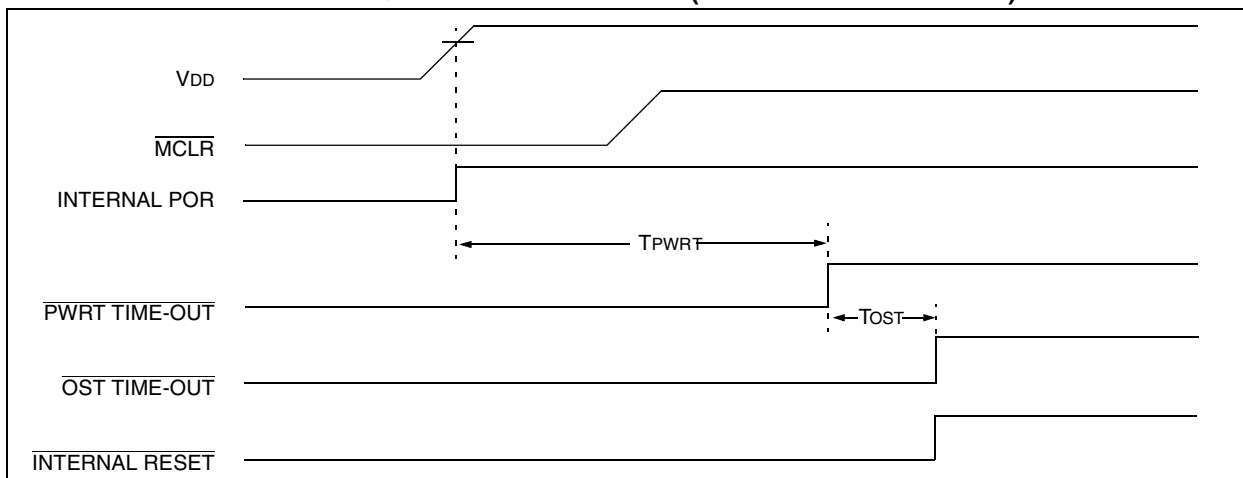`q` = value depends on condition.
Note 1:   One or more bits in INTCON will be affected (to cause wake-up).
2:   When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).
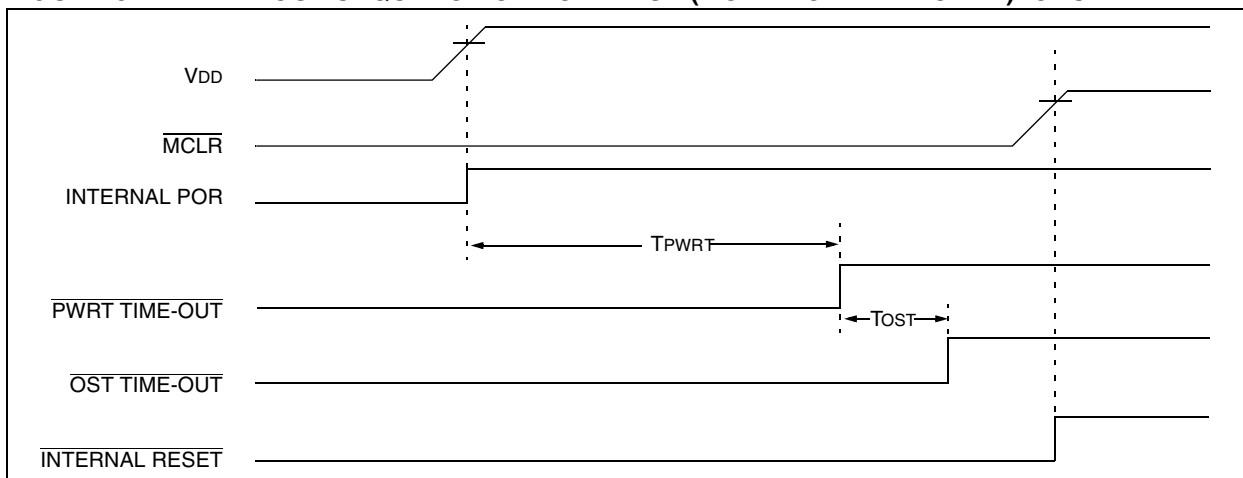3:   Table 8-3 lists the reset value for each specific condition.

FIGURE 8-10: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): CASE 1

FIGURE 8-11: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): CASE 2

8.7 Time-out Sequence and Power-down Status Bits (TO/PD)

On power-up (Figure 8-10, Figure 8-11, Figure 8-12 and Figure 8-13) the time-out sequence is as follows: First PWRT time-out is invoked after a POR has expired. Then the OST is activated. The total time-out will vary based on oscillator configuration and PWRTE configuration bit status. For example, in RC mode with the PWRT disabled, there will be no time-out at all.

TABLE 8-5 TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up		Wake-up from SLEEP
	PWRT Enabled	**PWRT Disabled**	
XT, HS, LP	72 ms + 1024TOSC	1024TOSC	1024TOSC
RC	72 ms	—	—

Since the time-outs occur from the POR reset pulse, if $\overline{MCLR}$ is kept low long enough, the time-outs will expire. Then bringing $\overline{MCLR}$ high, execution will begin immediately (Figure 8-10). This is useful for testing purposes or to synchronize more than one PIC16F8X device when operating in parallel.

Table 8-6 shows the significance of the $\overline{TO}$ and $\overline{PD}$ bits. Table 8-3 lists the reset conditions for some special registers, while Table 8-4 lists the reset conditions for all the registers.

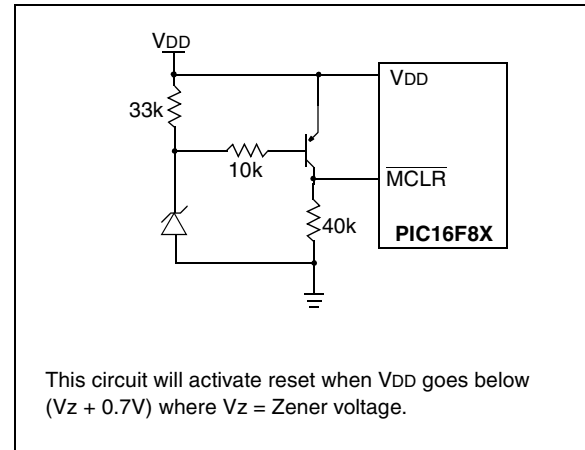**TABLE 8-6 STATUS BITS AND THEIR SIGNIFICANCE**

$\overline{TO}$	$\overline{PD}$	Condition
1	1	Power-on Reset
0	x	Illegal, $\overline{TO}$ is set on $\overline{POR}$
x	0	Illegal, $\overline{PD}$ is set on $\overline{POR}$
0	1	WDT Reset (during normal operation)
0	0	WDT Wake-up
1	1	$\overline{MCLR}$ Reset during normal operation
1	0	$\overline{MCLR}$ Reset during SLEEP or interrupt wake-up from SLEEP

8.8 Reset on Brown-Out

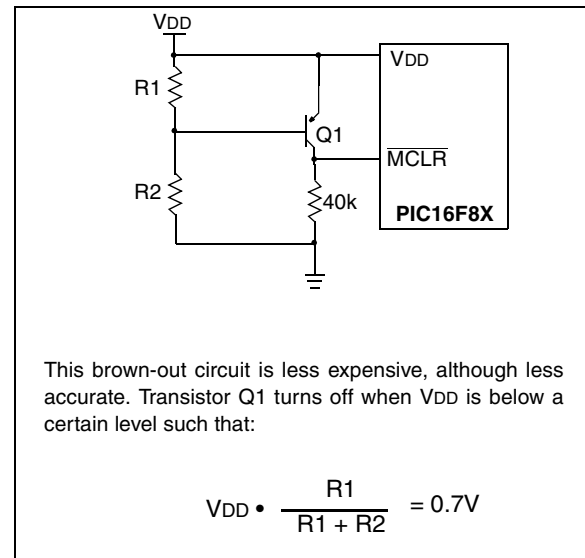A brown-out is a condition where device power (VDD) dips below its minimum value, but not to zero, and then recovers. The device should be reset in the event of a brown-out.

To reset a PIC16F8X device when a brown-out occurs, external brown-out protection circuits may be built, as shown in Figure 8-14 and Figure 8-15.

FIGURE 8-14: BROWN-OUT PROTECTION CIRCUIT 1

This circuit will activate reset when VDD goes below (Vz + 0.7V) where Vz = Zener voltage.

FIGURE 8-15: BROWN-OUT PROTECTION CIRCUIT 2

This brown-out circuit is less expensive, although less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$VDD \cdot \frac{R1}{R1 + R2} = 0.7V$$

NOP	No Operation
Syntax:	[*label*] NOP
Operands:	None
Operation:	No operation
Status Affected:	None

Encoding:

00	0000	0xx0	0000

Description:	No operation.
Words:	1
Cycles:	1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	No-Operation	No-Operation	No-Operation

Example   NOP

OPTION	Load Option Register
Syntax:	[*label*] OPTION
Operands:	None
Operation:	(W) → OPTION
Status Affected:	None

Encoding:

00	0000	0110	0010

Description:	The contents of the W register are loaded in the OPTION register. This instruction is supported for code compatibility with PIC16C5X products. Since OPTION is a readable/writable register, the user can directly address it.
Words:	1
Cycles:	1
Example	

To maintain upward compatibility with future PIC16CXX products, do not use this instruction.

RETFIE	Return from Interrupt
Syntax:	[*label*] RETFIE
Operands:	None
Operation:	TOS → PC, 1 → GIE
Status Affected:	None

Encoding:

00	0000	0000	1001

Description:	Return from Interrupt. Stack is POPed and Top of Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a two cycle instruction.
Words:	1
Cycles:	2

Q Cycle Activity:

	Q1	Q2	Q3	Q4
1st Cycle	Decode	No-Operation	Set the GIE bit	Pop from the Stack
2nd Cycle	No-Operation	No-Operation	No-Operation	No-Operation

Example   RETFIE

After Interrupt
    PC   =   TOS
    GIE =   1

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RETLW	**Return with Literal in W**
Syntax:	[*label*] RETLW k
Operands:	0 ≤ k ≤ 255
Operation:	k → (W); TOS → PC
Status Affected:	None
Encoding:	

11	01xx	kkkk	kkkk

Description:	The W register is loaded with the eight bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two cycle instruction.
Words:	1
Cycles:	2

Q Cycle Activity:

	Q1	Q2	Q3	Q4
1st Cycle	Decode	Read literal 'k'	No-Operation	Write to W, Pop from the Stack
2nd Cycle	No-Operation	No-Operation	No-Operation	No-Operation

Example

```
CALL TABLE  ;W contains table
            ;offset value
•           ;W now has table value
•
•
TABLE ADDWF PC  ;W = offset
RETLW k1  ;Begin table
RETLW k2  ;
•
•
•
RETLW kn  ; End of table
```

Before Instruction
    W   =   0x07
After Instruction
    W   =   value of k8

RETURN	**Return from Subroutine**
Syntax:	[*label*] RETURN
Operands:	None
Operation:	TOS → PC
Status Affected:	None
Encoding:	

00	0000	0000	1000

Description:	Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two cycle instruction.
Words:	1
Cycles:	2

Q Cycle Activity:

	Q1	Q2	Q3	Q4
1st Cycle	Decode	No-Operation	No-Operation	Pop from the Stack
2nd Cycle	No-Operation	No-Operation	No-Operation	No-Operation

Example   RETURN

After Interrupt
            PC   =   TOS

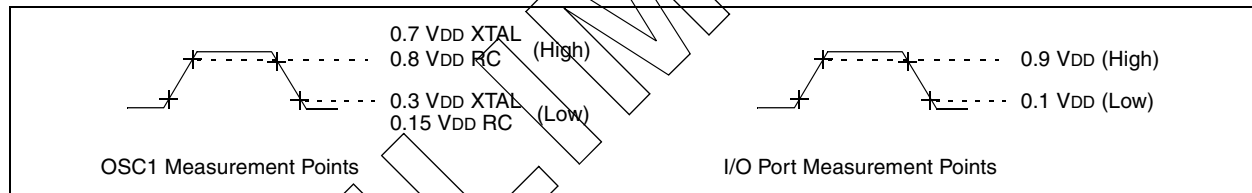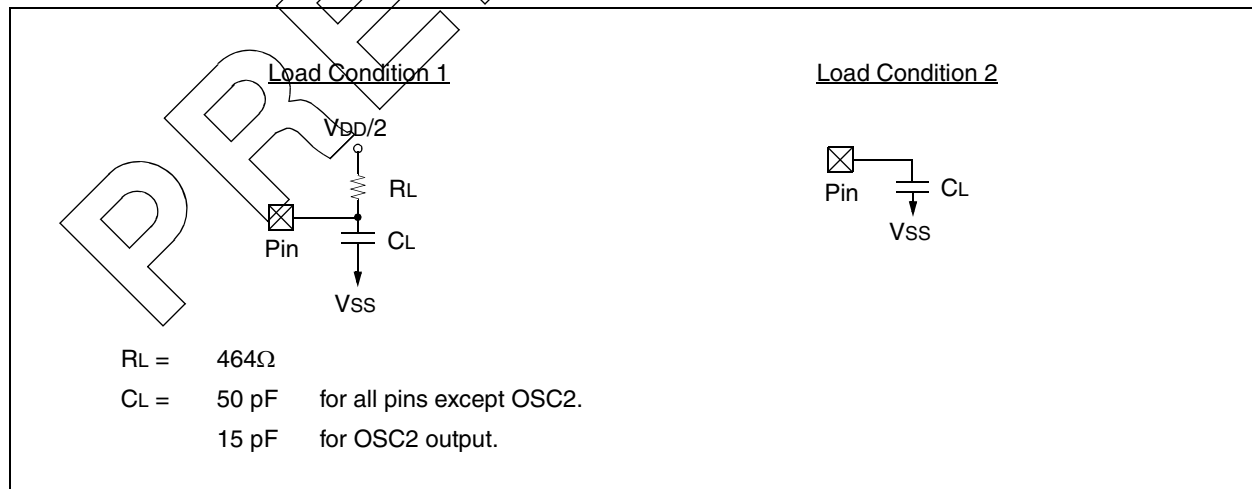**TABLE 10-2   TIMING PARAMETER SYMBOLOGY**

The timing parameter symbols have been created fol-
lowing one of the following formats:

1. TppS2ppS
2. TppS

T				
F	Frequency		T	Time

Lowercase symbols (pp) and their meanings:

pp				
2	to		os,osc	OSC1
ck	CLKOUT		ost	oscillator start-up timer
cy	cycle time		pwrt	power-up timer
io	I/O port		rbt	RBx pins
inp	INT pin		t0	T0CKI
mc	MCLR		wdt	watchdog timer

Uppercase symbols and their meanings:

S				
F	Fall		P	Period
H	High		R	Rise
I	Invalid (Hi-impedance)		V	Valid
L	Low		Z	High Impedance

FIGURE 10-1:   PARAMETER MEASUREMENT INFORMATION

All timings are measure between high and low mea-
surement points as indicated in the figures below.

OSC1 Measurement Points   I/O Port Measurement Points

FIGURE 10-2:   LOAD CONDITIONS

Load Condition 1

Load Condition 2

R_L =   464Ω

C_L =   50 pF   for all pins except OSC2.

15 pF   for OSC2 output.

FIGURE 10-5: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING
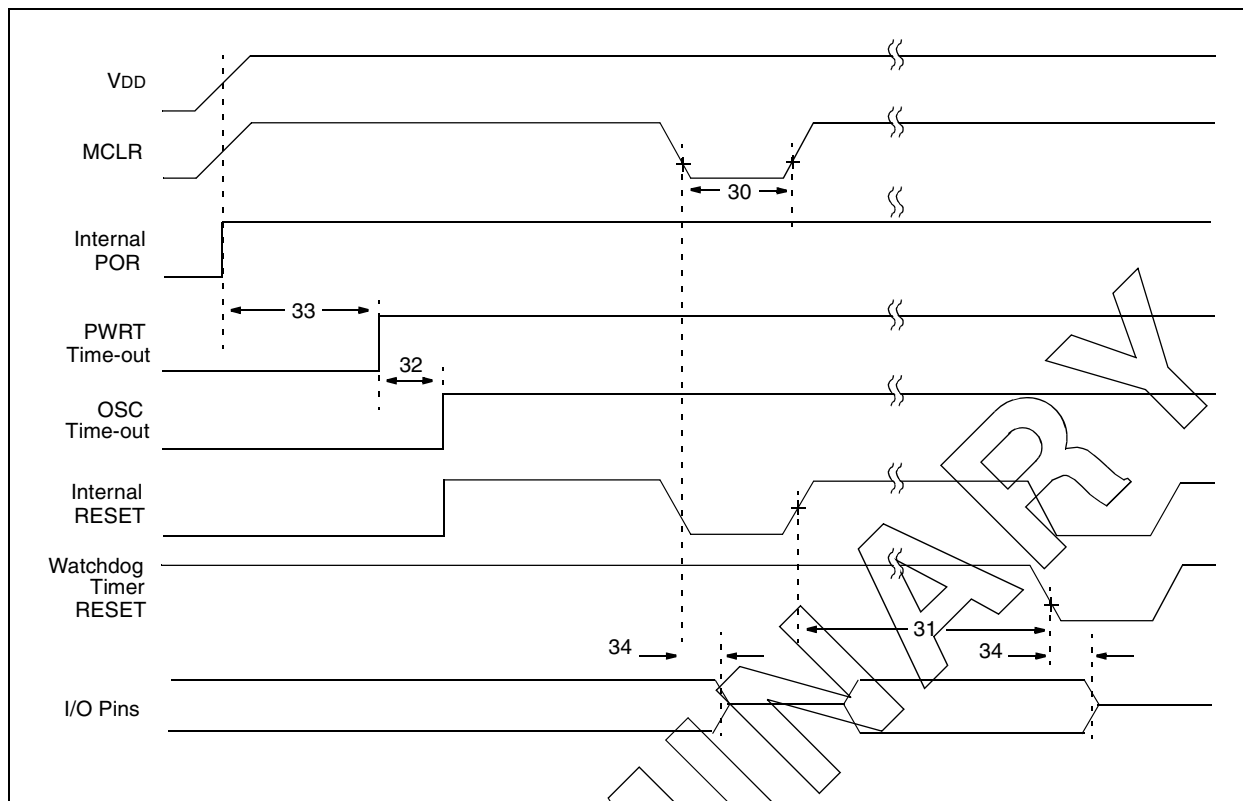
TABLE 10-5   RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmcL	MCLR Pulse Width (low)	1000 *	—	—	ns	2.0V ≤ VDD ≤ 6.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7 *	18	33 *	ms	VDD = 5.0V
32	Tost	Oscillation Start-up Timer Period		1024TOSC		ms	TOSC = OSC1 period
33	Tpwrt	Power-up Timer Period	28 *	72	132 *	ms	VDD = 5.0V
34	TIOZ	I/O Hi-impedance from MCLR Low or reset	—	—	100 *	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

11.1 DC CHARACTERISTICS: PIC16CR84, PIC16CR83 (Commercial, Industrial)

DC Characteristics Power Supply Pins			Standard Operating Conditions (unless otherwise stated) Operating temperature 0°C $\leq T_A \leq$ +70°C (commercial) -40°C $\leq T_A \leq$ +85°C (industrial)				
Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D001	V_{DD}	Supply Voltage	4.0	—	6.0	V	XT, RC and LP osc configuration
D001A			4.5	—	5.5	V	HS osc configuration
D002	V_{DR}	RAM Data Retention Voltage[1]	1.5*	—	—	V	Device in SLEEP mode
D003	V_{POR}	V_{DD} start voltage to ensure internal Power-on Reset signal	—	Vss	—	V	See section on Power-on Reset for details
D004	S_{VDD}	V_{DD} rise rate to ensure internal Power-on Reset signal	0.05*	—	—	V/ms	See section on Power-on Reset for details
	I_{DD}	Supply Current[2]					RC and XT osc configuration[4]
D010			—	1.8	4.5	mA	F_{OSC} = 4.0 MHz, V_{DD} = 5.5V
D010A			—	7.3	10	mA	F_{OSC} = 4.0 MHz, V_{DD} = 5.5V (During EEPROM programming)
D013			—	5	10	mA	HS osc configuration (PIC16CR84-10) F_{OSC} = 10 MHz, V_{DD} = 5.5V
D020	I_{PD}	Power-down Current[3]	—	7.0	28	μA	V_{DD} = 4.0V, WDT enabled, industrial
D021			—	1.0	14	μA	V_{DD} = 4.0V, WDT disabled, commercial
D021A			—	1.0	16	μA	V_{DD} = 4.0V, WDT disabled, industrial

*   These parameters are characterized but not tested.

†   Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which V_{DD} can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.
The test conditions for all I_{DD} measurements in active operation mode are:
OSC1=external square wave, from rail to rail; all I/O pins tristated, pulled to V_{DD}, T0CKI = V_{DD},
$\overline{MCLR}$ = V_{DD}; WDT enabled/disabled as specified.

3: The power down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to V_{DD} and V_{SS}.

4: For RC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula I_R = V_{DD}/2Rext (mA) with Rext in kOhm.

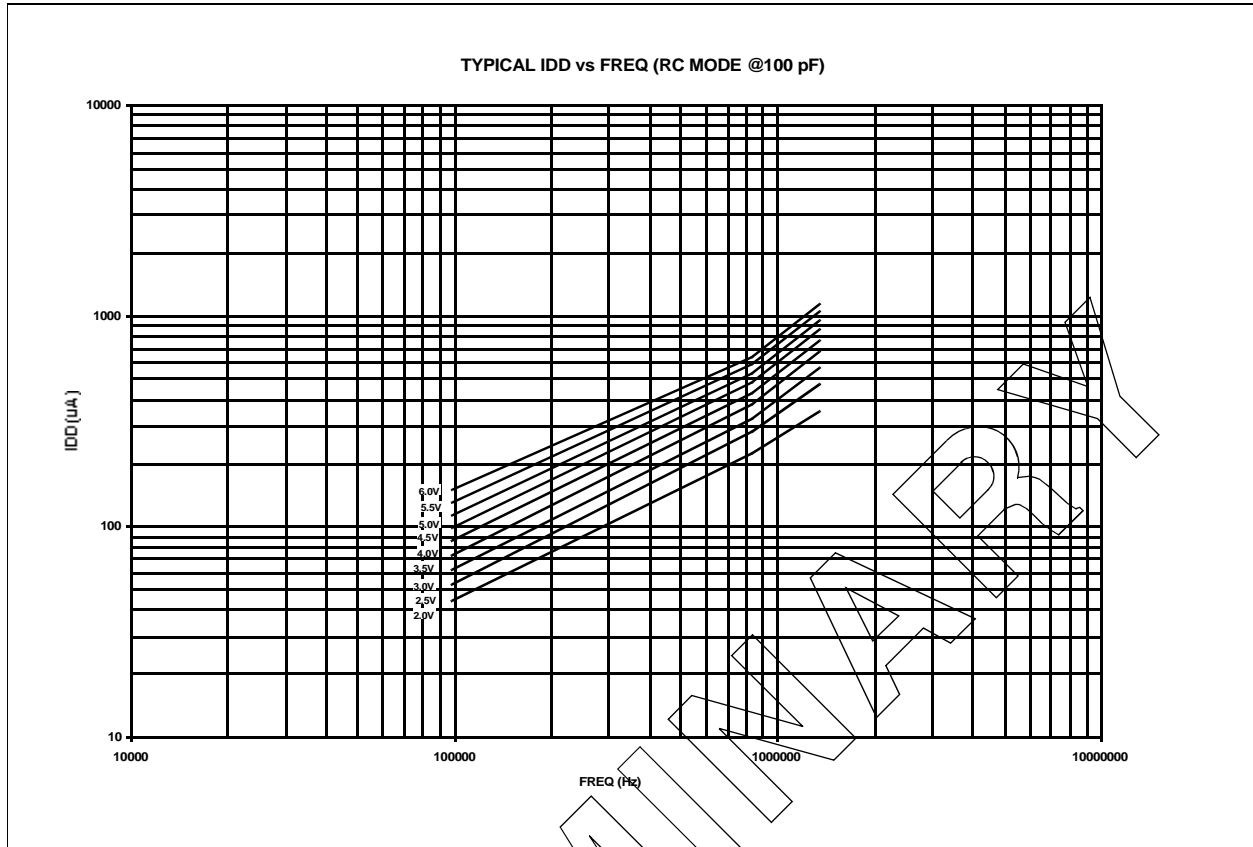**FIGURE 12-11: TYPICAL I_DD vs. FREQUENCY (RC MODE @100PF, 25°C)**

TYPICAL IDD vs FREQ (RC MODE @100 pF)

PIC16F8X

FIGURE 12-21: TYPICAL DATA MEMORY ERASE/WRITE CYCLE TIME VS. VDD

Shaded area is beyond recommended range.
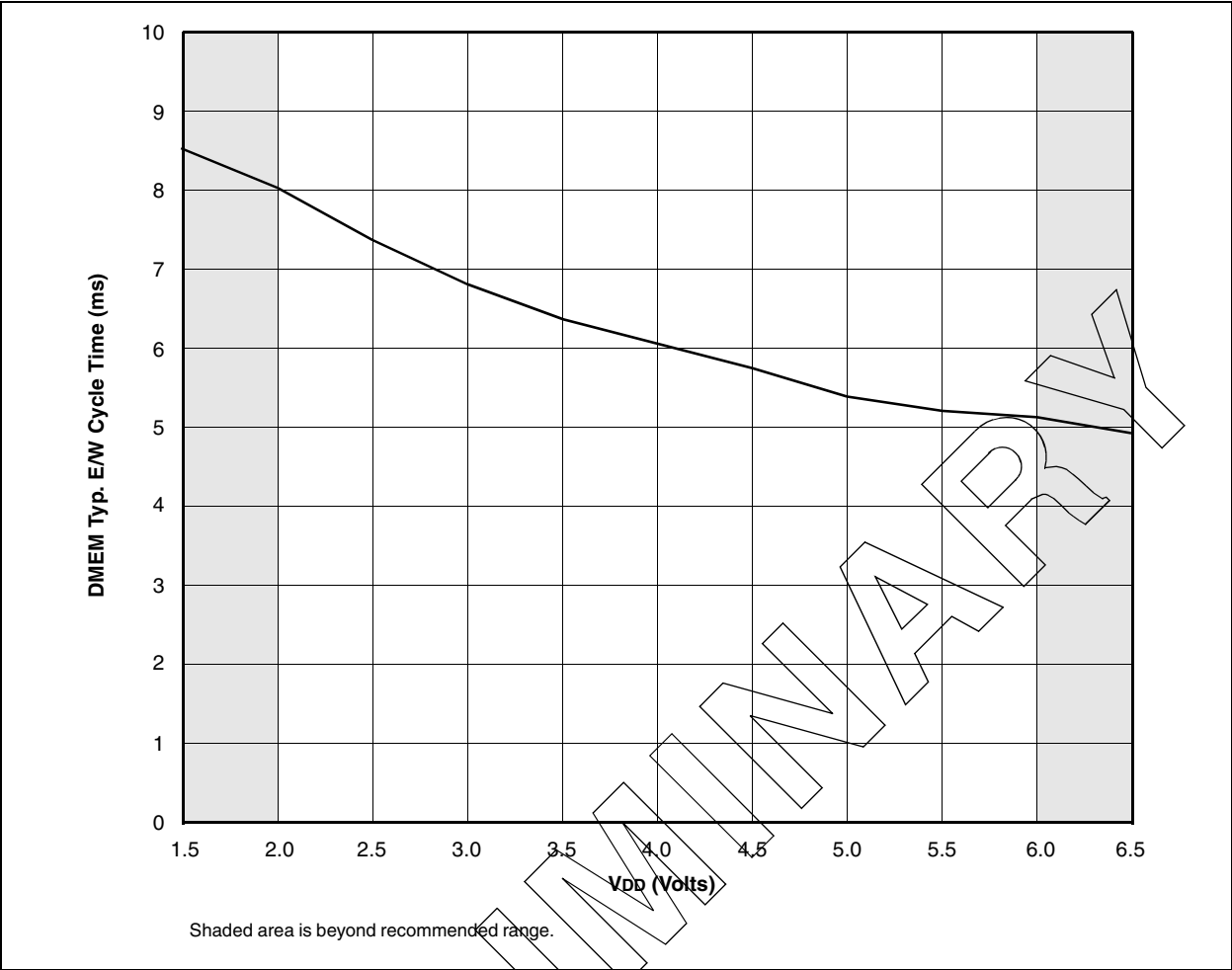
TABLE 12-2 INPUT CAPACITANCE*

Pin Name	Typical Capacitance (pF)	
	18L PDIP	18L SOIC
PORTA	5.0	4.3
PORTB	5.0	4.3
MCLR	17.0	17.0
OSC1/CLKIN	4.0	3.5
OSC2/CLKOUT	4.3	3.5
T0CKI	3.2	2.8

* All capacitance values are typical at 25°C. A part to part variation of ±25% (three standard deviations) should be taken into account.

13.0 PACKAGING INFORMATION

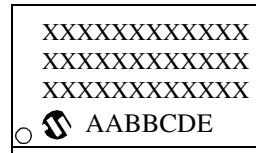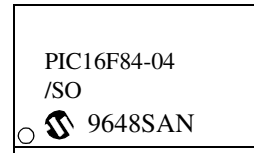### 13.1 Package Marking Information

18L PDIP

```
XXXXXXXXXXXXXXXXX
XXXXXXXXXXXXXXXXX
     AABBCDE
```

Example

```
     PIC16F84-04I/P
       9632SAW
```

18L SOIC

```
XXXXXXXXXXX
XXXXXXXXXXX
XXXXXXXXXXX
    AABBCDE
```

**Example**

```
PIC16F84-04
/SO
     9648SAN
```
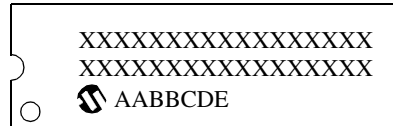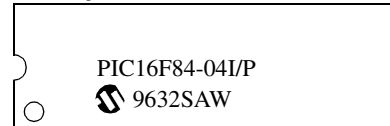
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

Package Type: K04-051 18-Lead Plastic Small Outline (SO) – Wide, 300 mil

> **Note:**   For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
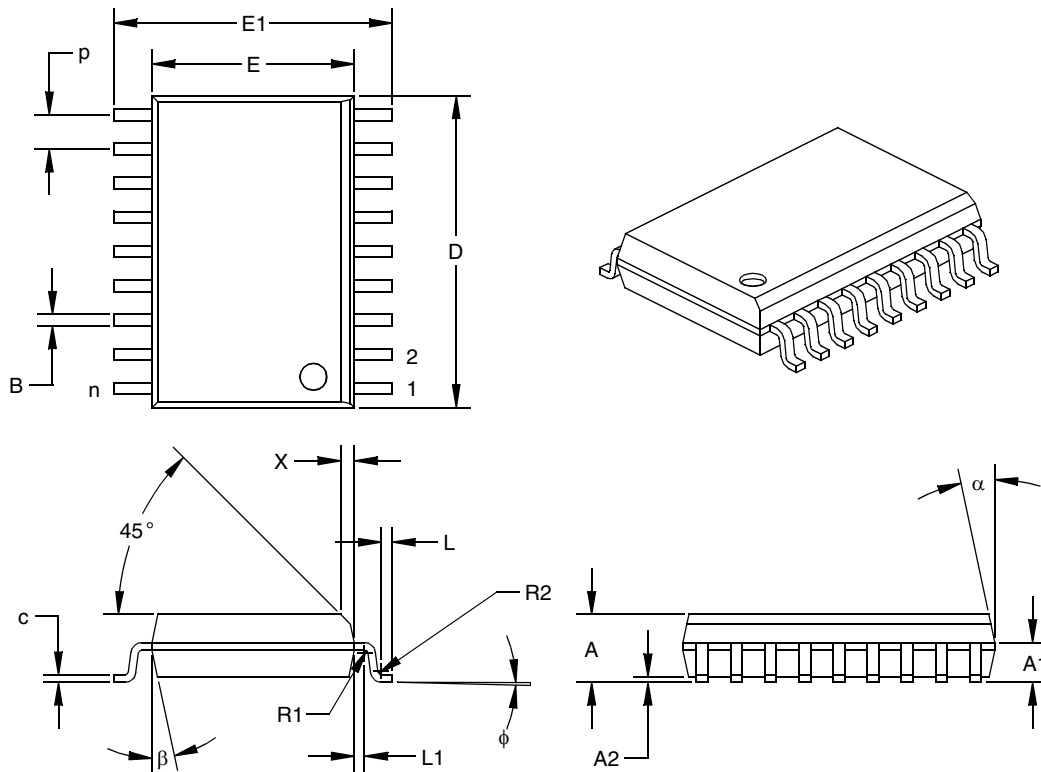
Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	p		0.050			1.27	
Number of Pins	n		18			18	
Overall Pack. Height	A	0.093	0.099	0.104	2.36	2.50	2.64
Shoulder Height	A1	0.048	0.058	0.068	1.22	1.47	1.73
Standoff	A2	0.004	0.008	0.011	0.10	0.19	0.28
Molded Package Length	D‡	0.450	0.456	0.462	11.43	11.58	11.73
Molded Package Width	E‡	0.292	0.296	0.299	7.42	7.51	7.59
Outside Dimension	E1	0.394	0.407	0.419	10.01	10.33	10.64
Chamfer Distance	X	0.010	0.020	0.029	0.25	0.50	0.74
Shoulder Radius	R1	0.005	0.005	0.010	0.13	0.13	0.25
Gull Wing Radius	R2	0.005	0.005	0.010	0.13	0.13	0.25
Foot Length	L	0.011	0.016	0.021	0.28	0.41	0.53
Foot Angle	φ	0	4	8	0	4	8
Radius Centerline	L1	0.010	0.015	0.020	0.25	0.38	0.51
Lead Thickness	c	0.009	0.011	0.012	0.23	0.27	0.30
Lower Lead Width	B†	0.014	0.017	0.019	0.36	0.42	0.48
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

*   Controlling Parameter.

†   Dimension "B" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B."

‡   Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

PIC16F8X PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-XX	X	/XX	XXX
Device	Frequency Range	Temperature Range	Package	Pattern

Device	PIC16F8X[2], PIC16F8XT[3] PIC16LF8X[2], PIC16LF8XT[3] PIC16F8XA[2], PIC16F8XAT[3] PIC16LF8XA[2], PIC16LF8XAT[3] PIC16CR8X[2], PIC16CR8XT[3] PIC16LCR8X[2], PIC16LCR8XT[3]
Frequency Range	04 = 4 MHz 10 = 10 MHz 20 = 20 MHz
Temperature Range	b[1] = 0°C to +70°C (Commercial) I = -40°C to +85°C (Industrial)
Package	P = PDIP SO = SOIC (Gull Wing, 300 mil body) SS = SSOP
Pattern	3-digit Pattern Code for QTP, ROM (blank otherwise)

Examples:

a) PIC16F84 -04/P 301 = Commercial temp., PDIP package, 4 MHz, normal V$_{DD}$ limits, QTP pattern #301.

b) PIC16LF84 - 04I/SO = Industrial temp., SOIC package, 200 kHz, Extended V$_{DD}$ limits.

c) PIC16CR84 - 10I/P = ROM program memory, Industrial temp., PDIP package, 10MHz, normal V$_{DD}$ limits.

Note 1: b = blank

2: F = Standard V$_{DD}$ range
LF = Extended V$_{DD}$ range
CR = ROM Version, Standard V$_{DD}$ range
LCR = ROM Version, Extended V$_{DD}$ range

3: T = in tape and reel - SOIC, SSOP packages only.

SALES AND SUPPORT

Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office.

2. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

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11/29/12