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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	4MHz
Connectivity	-
Peripherals	POR, WDT
Number of I/O	13
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	64 x 8
RAM Size	68 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 6V
Data Converters	-
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	18-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f84-04-p

TABLE 3-1 PIC16F8X PINOUT DESCRIPTION

Pin Name	DIP No.	SOIC No.	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	16	16	I	ST/CMOS ⁽³⁾	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	15	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
MCLR	4	4	I/P	ST	Master clear (reset) input/programming voltage input. This pin is an active low reset to the device.
RA0	17	17	I/O	TTL	<p>PORTA is a bi-directional I/O port.</p> <p>Can also be selected to be the clock input to the TMR0 timer/counter. Output is open drain type.</p>
RA1	18	18	I/O	TTL	
RA2	1	1	I/O	TTL	
RA3	2	2	I/O	TTL	
RA4/T0CKI	3	3	I/O	ST	
RB0/INT	6	6	I/O	TTL/ST ⁽¹⁾	<p>PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.</p> <p>RB0/INT can also be selected as an external interrupt pin.</p> <p>Interrupt on change pin.</p> <p>Interrupt on change pin.</p> <p>Interrupt on change pin. Serial programming clock.</p> <p>Interrupt on change pin. Serial programming data.</p>
RB1	7	7	I/O	TTL	
RB2	8	8	I/O	TTL	
RB3	9	9	I/O	TTL	
RB4	10	10	I/O	TTL	
RB5	11	11	I/O	TTL	
RB6	12	12	I/O	TTL/ST ⁽²⁾	
RB7	13	13	I/O	TTL/ST ⁽²⁾	
VSS	5	5	P	—	Ground reference for logic and I/O pins.
VDD	14	14	P	—	Positive supply for logic and I/O pins.

Legend: I = input O = output I/O = Input/Output P = power
 — = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
 2: This buffer is a Schmitt Trigger input when used in serial programming mode.
 3: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

4.0 MEMORY ORGANIZATION

There are two memory blocks in the PIC16F8X. These are the program memory and the data memory. Each block has its own bus, so that access to each block can occur during the same oscillator cycle.

The data memory can further be broken down into the general purpose RAM and the Special Function Registers (SFRs). The operation of the SFRs that control the "core" are described here. The SFRs used to control the peripheral modules are described in the section discussing each individual peripheral module.

The data memory area also contains the data EEPROM memory. This memory is not directly mapped into the data memory, but is indirectly mapped. That is, an indirect address pointer specifies the address of the data EEPROM memory to read/write. The 64 bytes of data EEPROM memory have the address range 0h-3Fh. More details on the EEPROM memory can be found in Section 7.0.

4.1 Program Memory Organization

The PIC16FXX has a 13-bit program counter capable of addressing an 8K x 14 program memory space. For the PIC16F83 and PIC16CR83, the first 512 x 14 (0000h-01FFh) are physically implemented (Figure 4-1). For the PIC16F84 and PIC16CR84, the first 1K x 14 (0000h-03FFh) are physically implemented (Figure 4-2). Accessing a location above the physically implemented address will cause a wrap-around. For example, for the PIC16F84 locations 20h, 420h, 820h, C20h, 1020h, 1420h, 1820h, and 1C20h will be the same instruction.

The reset vector is at 0000h and the interrupt vector is at 0004h.

FIGURE 4-1: PROGRAM MEMORY MAP AND STACK - PIC16F83/CR83

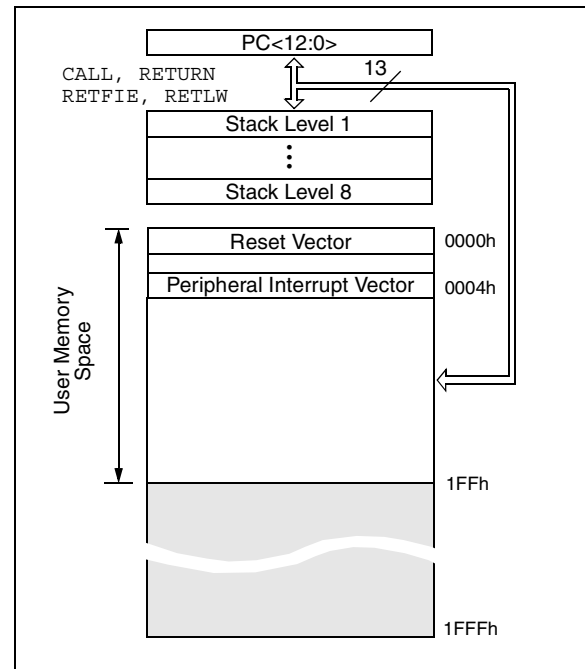
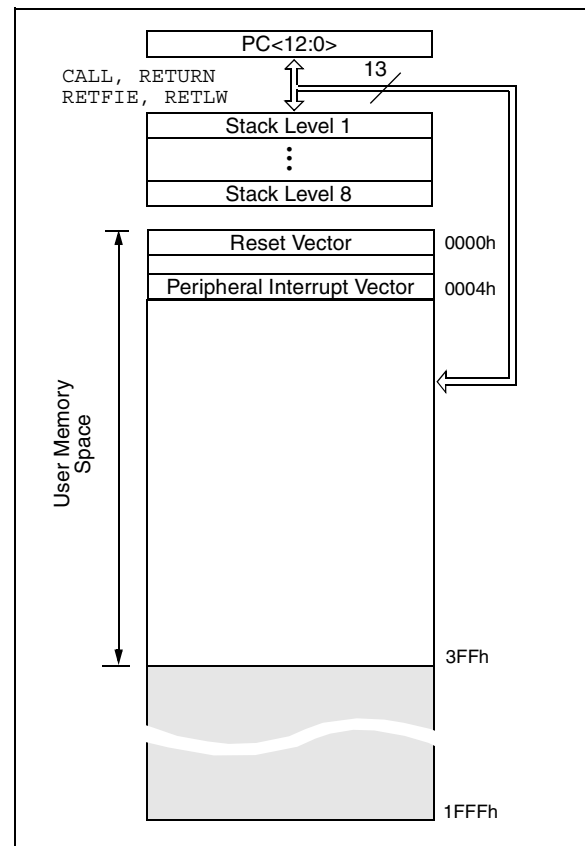


FIGURE 4-2: PROGRAM MEMORY MAP AND STACK - PIC16F84/CR84



5.3 I/O Programming Considerations

5.3.1 BI-DIRECTIONAL I/O PORTS

Any instruction which writes, operates internally as a read followed by a write operation. The `BCF` and `BSF` instructions, for example, read the register into the CPU, execute the bit operation and write the result back to the register. Caution must be used when these instructions are applied to a port with both inputs and outputs defined. For example, a `BSF` operation on bit5 of `PORTB` will cause all eight bits of `PORTB` to be read into the CPU. Then the `BSF` operation takes place on bit5 and `PORTB` is written to the output latches. If another bit of `PORTB` is used as a bi-directional I/O pin (i.e., bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit0 is switched into output mode later on, the content of the data latch is unknown.

Reading the port register, reads the values of the port pins. Writing to the port register writes the value to the port latch. When using read-modify-write instructions (i.e., `BCF`, `BSF`, etc.) on a port, the value of the port pins is read, the desired operation is done to this value, and this value is then written to the port latch.

A pin actively outputting a Low or High should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output current may damage the chip.

5.3.2 SUCCESSIVE OPERATIONS ON I/O PORTS

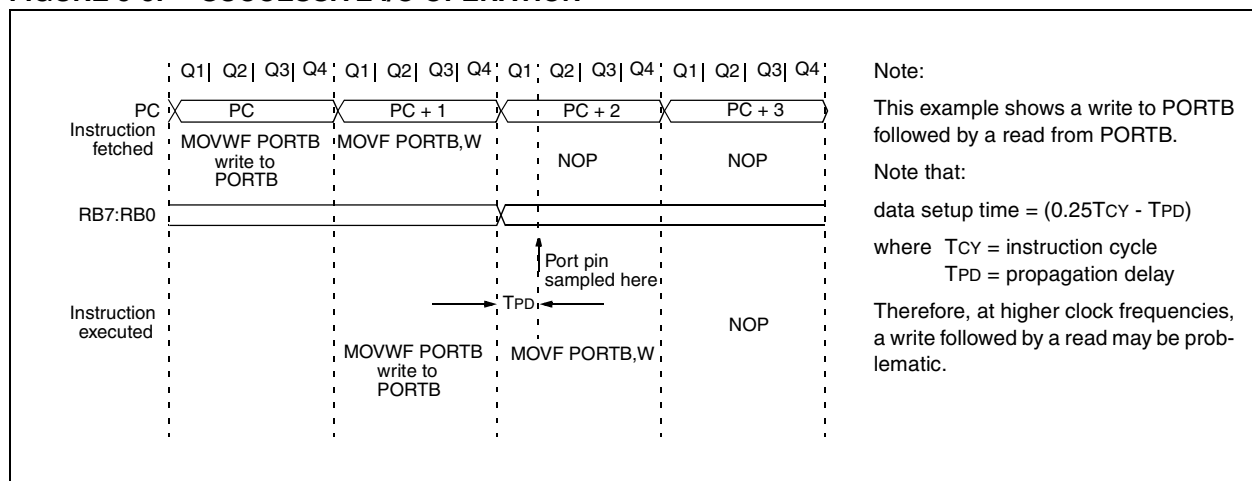
The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 5-5). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should be such that the pin voltage stabilizes (load dependent) before the next instruction which causes that file to be read into the CPU is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a `NOP` or another instruction not accessing this I/O port.

Example 5-1 shows the effect of two sequential read-modify-write instructions (e.g., `BCF`, `BSF`, etc.) on an I/O port.

EXAMPLE 5-1: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

```
;Initial PORT settings: PORTB<7:4> Inputs
;                       PORTB<3:0> Outputs
;PORTB<7:6> have external pull-ups and are
;not connected to other circuitry
;
;
;                       PORT latch  PORT pins
;                       -----
;
; BCF PORTB, 7          ; 01pp ppp   11pp ppp
; BCF PORTB, 6          ; 10pp ppp   11pp ppp
; BSF STATUS, RP0      ;
; BCF TRISB, 7          ; 10pp ppp   11pp ppp
; BCF TRISB, 6          ; 10pp ppp   10pp ppp
;
;Note that the user may have expected the
;pin values to be 00pp ppp. The 2nd BCF
;caused RB7 to be latched as the pin value
;(high).
```

FIGURE 5-5: SUCCESSIVE I/O OPERATION



PIC16F8X

NOTES:

7.0 DATA EEPROM MEMORY

The EEPROM data memory is readable and writable during normal operation (full VDD range). This memory is not directly mapped in the register file space. Instead it is indirectly addressed through the Special Function Registers. There are four SFRs used to read and write this memory. These registers are:

- EECON1
- EECON2
- EEDATA
- EEADR

EEDATA holds the 8-bit data for read/write, and EEADR holds the address of the EEPROM location being accessed. PIC16F8X devices have 64 bytes of data EEPROM with an address range from 0h to 3Fh.

The EEPROM data memory allows byte read and write. A byte write automatically erases the location and writes the new data (erase before write). The EEPROM

data memory is rated for high erase/write cycles. The write time is controlled by an on-chip timer. The write-time will vary with voltage and temperature as well as from chip to chip. Please refer to AC specifications for exact limits.

When the device is code protected, the CPU may continue to read and write the data EEPROM memory. The device programmer can no longer access this memory.

7.1 EEADR

The EEADR register can address up to a maximum of 256 bytes of data EEPROM. Only the first 64 bytes of data EEPROM are implemented.

The upper two bits are address decoded. This means that these two bits must always be '0' to ensure that the address is in the 64 byte memory space.

FIGURE 7-1: EECON1 REGISTER (ADDRESS 88h)

U	U	U	R/W-0	R/W-x	R/W-0	R/S-0	R/S-x
—	—	—	EEIF	WRERR	WREN	WR	RD
bit7							bit0

R = Readable bit
W = Writable bit
S = Settable bit
U = Unimplemented bit, read as '0'
- n = Value at POR reset

bit 7:5 **Unimplemented:** Read as '0'

bit 4 **EEIF:** EEPROM Write Operation Interrupt Flag bit
1 = The write operation completed (must be cleared in software)
0 = The write operation is not complete or has not been started

bit 3 **WRERR:** EEPROM Error Flag bit
1 = A write operation is prematurely terminated (any MCLR reset or any WDT reset during normal operation)
0 = The write operation completed

bit 2 **WREN:** EEPROM Write Enable bit
1 = Allows write cycles
0 = Inhibits write to the data EEPROM

bit 1 **WR:** Write Control bit
1 = initiates a write cycle. (The bit is cleared by hardware once write is complete. The WR bit can only be set (not cleared) in software.
0 = Write cycle to the data EEPROM is complete

bit 0 **RD:** Read Control bit
1 = Initiates an EEPROM read (read takes one cycle. RD is cleared in hardware. The RD bit can only be set (not cleared) in software).
0 = Does not initiate an EEPROM read

8.4 Power-on Reset (POR)

A Power-on Reset pulse is generated on-chip when VDD rise is detected (in the range of 1.2V - 1.7V). To take advantage of the POR, just tie the $\overline{\text{MCLR}}$ pin directly (or through a resistor) to VDD. This will eliminate external RC components usually needed to create Power-on Reset. A minimum rise time for VDD must be met for this to operate properly. See Electrical Specifications for details.

When the device starts normal operation (exits the reset condition), device operating parameters (voltage, frequency, temperature, ...) must be met to ensure operation. If these conditions are not met, the device must be held in reset until the operating conditions are met.

For additional information, refer to Application Note AN607, "Power-up Trouble Shooting."

The POR circuit does not produce an internal reset when VDD declines.

8.5 Power-up Timer (PWRT)

The Power-up Timer (PWRT) provides a fixed 72 ms nominal time-out (TPWRT) from POR (Figure 8-10, Figure 8-11, Figure 8-12 and Figure 8-13). The Power-up Timer operates on an internal RC oscillator. The chip is kept in reset as long as the PWRT is active. The PWRT delay allows the VDD to rise to an acceptable level (Possible exception shown in Figure 8-13).

A configuration bit, PWRTE, can enable/disable the PWRT. See either Figure 8-1 or Figure 8-2 for the operation of the PWRTE bit for a particular device.

The power-up time delay TPWRT will vary from chip to chip due to VDD, temperature, and process variation. See DC parameters for details.

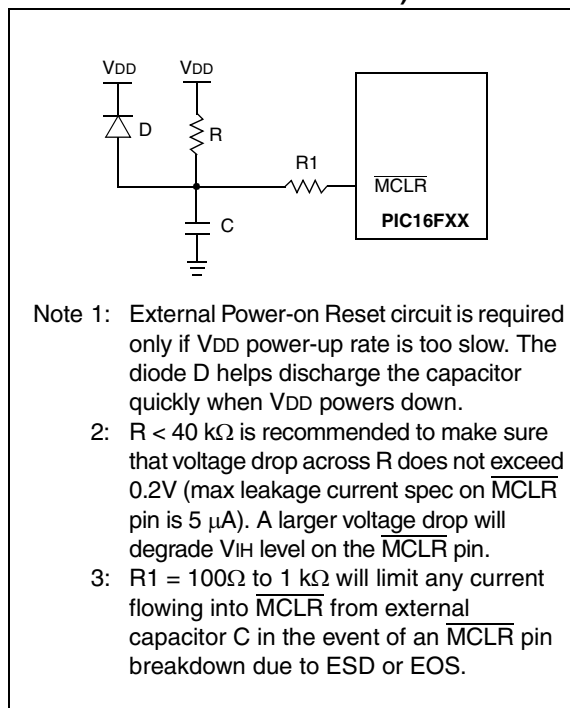
8.6 Oscillator Start-up Timer (OST)

The Oscillator Start-up Timer (OST) provides a 1024 oscillator cycle delay (from OSC1 input) after the PWRT delay ends (Figure 8-10, Figure 8-11, Figure 8-12 and Figure 8-13). This ensures the crystal oscillator or resonator has started and stabilized.

The OST time-out (TOST) is invoked only for XT, LP and HS modes and only on Power-on Reset or wake-up from SLEEP.

When VDD rises very slowly, it is possible that the TPWRT time-out and TOST time-out will expire before VDD has reached its final value. In this case (Figure 8-13), an external power-on reset circuit may be necessary (Figure 8-9).

FIGURE 8-9: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



8.7 Time-out Sequence and Power-down Status Bits (TO/PD)

On power-up (Figure 8-10, Figure 8-11, Figure 8-12 and Figure 8-13) the time-out sequence is as follows: First PWRT time-out is invoked after a POR has expired. Then the OST is activated. The total time-out will vary based on oscillator configuration and PWRT configuration bit status. For example, in RC mode with the PWRT disabled, there will be no time-out at all.

TABLE 8-5 TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up		Wake-up from SLEEP
	PWRT Enabled	PWRT Disabled	
XT, HS, LP	72 ms + 1024TOSC	1024TOSC	1024TOSC
RC	72 ms	—	—

Since the time-outs occur from the POR reset pulse, if $\overline{\text{MCLR}}$ is kept low long enough, the time-outs will expire. Then bringing $\overline{\text{MCLR}}$ high, execution will begin immediately (Figure 8-10). This is useful for testing purposes or to synchronize more than one PIC16F8X device when operating in parallel.

Table 8-6 shows the significance of the $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits. Table 8-3 lists the reset conditions for some special registers, while Table 8-4 lists the reset conditions for all the registers.

TABLE 8-6 STATUS BITS AND THEIR SIGNIFICANCE

$\overline{\text{TO}}$	$\overline{\text{PD}}$	Condition
1	1	Power-on Reset
0	x	Illegal, $\overline{\text{TO}}$ is set on POR
x	0	Illegal, $\overline{\text{PD}}$ is set on POR
0	1	WDT Reset (during normal operation)
0	0	WDT Wake-up
1	1	$\overline{\text{MCLR}}$ Reset during normal operation
1	0	$\overline{\text{MCLR}}$ Reset during SLEEP or interrupt wake-up from SLEEP

8.8 Reset on Brown-Out

A brown-out is a condition where device power (V_{DD}) dips below its minimum value, but not to zero, and then recovers. The device should be reset in the event of a brown-out.

To reset a PIC16F8X device when a brown-out occurs, external brown-out protection circuits may be built, as shown in Figure 8-14 and Figure 8-15.

FIGURE 8-14: BROWN-OUT PROTECTION CIRCUIT 1

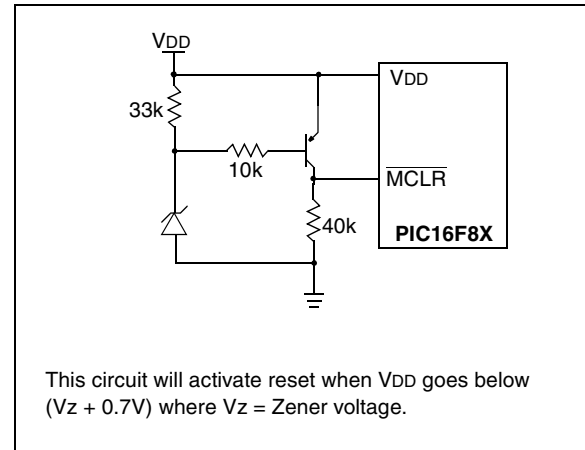
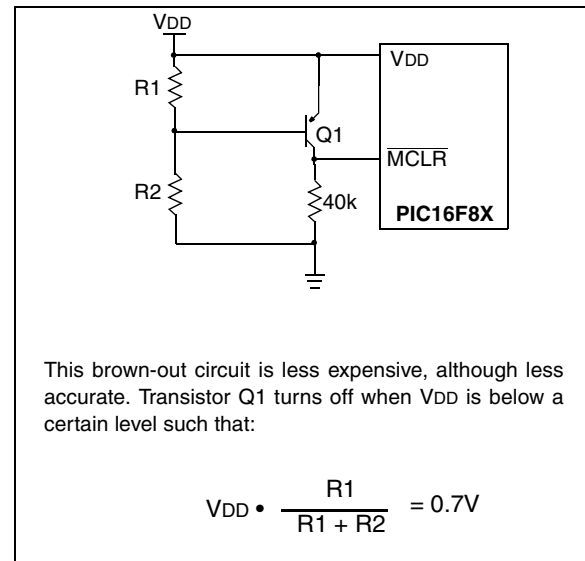


FIGURE 8-15: BROWN-OUT PROTECTION CIRCUIT 2



8.11 Watchdog Timer (WDT)

The Watchdog Timer is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins of the device has been stopped, for example, by execution of a `SLEEP` instruction. During normal operation a WDT time-out generates a device RESET. If the device is in `SLEEP` mode, a WDT Wake-up causes the device to wake-up and continue with normal operation. The WDT can be permanently disabled by programming configuration bit `WDTE` as a '0' (Section 8.1).

8.11.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). The time-out periods vary with temperature, V_{DD} and process variations from part to

part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the `OPTION_REG` register. Thus, time-out periods up to 2.3 seconds can be realized.

The `CLRWDT` and `SLEEP` instructions clear the WDT and the postscaler (if assigned to the WDT) and prevent it from timing out and generating a device RESET condition.

The \overline{TO} bit in the `STATUS` register will be cleared upon a WDT time-out.

8.11.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken into account that under worst case conditions (V_{DD} = Min., Temperature = Max., max. WDT prescaler) it may take several seconds before a WDT time-out occurs.

FIGURE 8-18: WATCHDOG TIMER BLOCK DIAGRAM

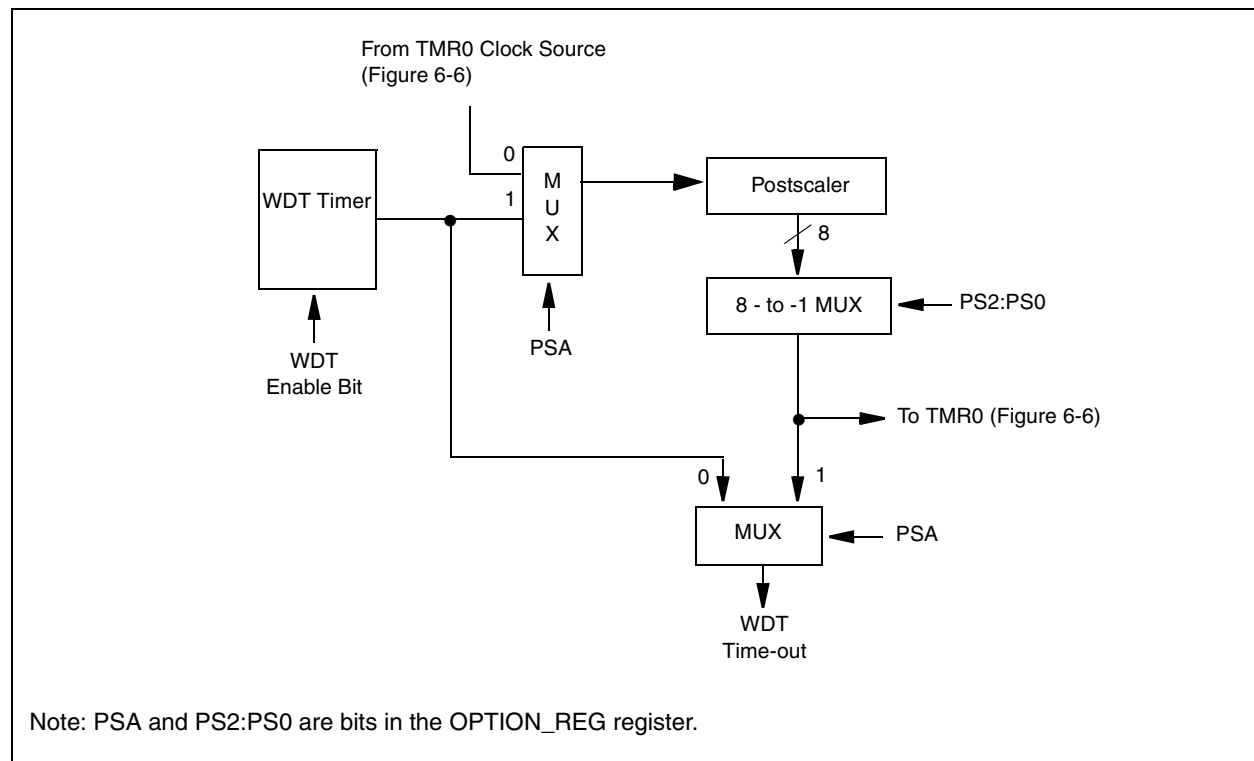


TABLE 8-7 SUMMARY OF REGISTERS ASSOCIATED WITH THE WATCHDOG TIMER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other resets
2007h	Config. bits	(2)	(2)	(2)	(2)	PWRTE ⁽¹⁾	WDTE	FOSC1	FOSC0	(2)	
81h	OPTION_REG	RBPV	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: x = unknown. Shaded cells are not used by the WDT.

Note 1: See Figure 8-1 and Figure 8-2 for operation of the PWRTE bit.

2: See Figure 8-1, Figure 8-2 and Section 8.13 for operation of the Code and Data protection bits.

8.12 Power-down Mode (SLEEP)

A device may be powered down (SLEEP) and later powered up (Wake-up from SLEEP).

8.12.1 SLEEP

The Power-down mode is entered by executing the `SLEEP` instruction.

If enabled, the Watchdog Timer is cleared (but keeps running), the \overline{PD} bit (STATUS<3>) is cleared, the \overline{TO} bit (STATUS<4>) is set, and the oscillator driver is turned off. The I/O ports maintain the status they had before the `SLEEP` instruction was executed (driving high, low, or hi-impedance).

For the lowest current consumption in SLEEP mode, place all I/O pins at either at VDD or VSS, with no external circuitry drawing current from the I/O pins, and disable external clocks. I/O pins that are hi-impedance inputs should be pulled high or low externally to avoid switching currents caused by floating inputs. The T0CKI input should also be at VDD or VSS. The contribution from on-chip pull-ups on PORTB should be considered.

The \overline{MCLR} pin must be at a logic high level (V_{IHMC}).

It should be noted that a RESET generated by a WDT time-out does not drive the \overline{MCLR} pin low.

8.12.2 WAKE-UP FROM SLEEP

The device can wake-up from SLEEP through one of the following events:

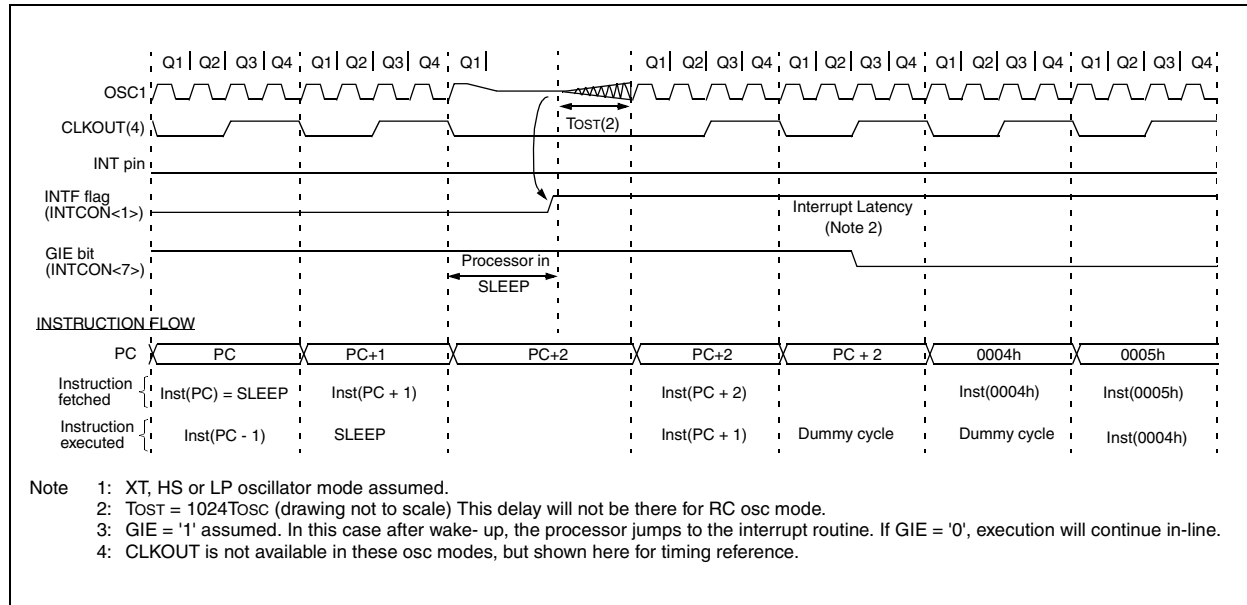
1. External reset input on \overline{MCLR} pin.
2. WDT Wake-up (if WDT was enabled).
3. Interrupt from RB0/INT pin, RB port change, or data EEPROM write complete.

Peripherals cannot generate interrupts during SLEEP, since no on-chip Q clocks are present.

The first event (\overline{MCLR} reset) will cause a device reset. The two latter events are considered a continuation of program execution. The \overline{TO} and \overline{PD} bits can be used to determine the cause of a device reset. The \overline{PD} bit, which is set on power-up, is cleared when SLEEP is invoked. The \overline{TO} bit is cleared if a WDT time-out occurred (and caused wake-up).

While the `SLEEP` instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up occurs regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the `SLEEP` instruction. If the GIE bit is set (enabled), the device executes the instruction after the `SLEEP` instruction and then branches to the interrupt address (0004h). In cases where the execution of the instruction following `SLEEP` is not desirable, the user should have a `NOP` after the `SLEEP` instruction.

FIGURE 8-19: WAKE-UP FROM SLEEP THROUGH INTERRUPT



PIC16F8X

TABLE 9-2 PIC16FXX INSTRUCTION SET

Mnemonic, Operands	Description	Cycles	14-Bit Opcode				Status Affected	Notes	
			MSb		LSb				
BYTE-ORIENTED FILE REGISTER OPERATIONS									
ADDWF f, d	Add W and f	1	00	0111	dfff	ffff	C,DC,Z	1,2	
ANDWF f, d	AND W with f	1	00	0101	dfff	ffff	Z	1,2	
CLRF f	Clear f	1	00	0001	1fff	ffff	Z	2	
CLRWF -	Clear W	1	00	0001	0xxx	xxxx	Z		
COMF f, d	Complement f	1	00	1001	dfff	ffff	Z	1,2	
DECF f, d	Decrement f	1	00	0011	dfff	ffff	Z	1,2	
DECFSZ f, d	Decrement f, Skip if 0	1(2)	00	1011	dfff	ffff		1,2,3	
INCF f, d	Increment f	1	00	1010	dfff	ffff	Z	1,2	
INCFSZ f, d	Increment f, Skip if 0	1(2)	00	1111	dfff	ffff		1,2,3	
IORWF f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	1,2	
MOVF f, d	Move f	1	00	1000	dfff	ffff	Z	1,2	
MOVWF f	Move W to f	1	00	0000	1fff	ffff			
NOP -	No Operation	1	00	0000	0xx0	0000			
RLF f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	C	1,2	
RRF f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	C	1,2	
SUBWF f, d	Subtract W from f	1	00	0010	dfff	ffff	C,DC,Z	1,2	
SWAPF f, d	Swap nibbles in f	1	00	1110	dfff	ffff		1,2	
XORWF f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	1,2	
BIT-ORIENTED FILE REGISTER OPERATIONS									
BCF f, b	Bit Clear f	1	01	00bb	bfff	ffff		1,2	
BSF f, b	Bit Set f	1	01	01bb	bfff	ffff		1,2	
BTFSC f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff	ffff		3	
BTFSS f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff	ffff		3	
LITERAL AND CONTROL OPERATIONS									
ADDLW k	Add literal and W	1	11	111x	kkkk	kkkk	C,DC,Z		
ANDLW k	AND literal with W	1	11	1001	kkkk	kkkk	Z		
CALL k	Call subroutine	2	10	0kkk	kkkk	kkkk			
CLRWDT -	Clear Watchdog Timer	1	00	0000	0110	0100	$\overline{TO}, \overline{PD}$		
GOTO k	Go to address	2	10	1kkk	kkkk	kkkk			
IORLW k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z		
MOVLW k	Move literal to W	1	11	00xx	kkkk	kkkk			
RETFIE -	Return from interrupt	2	00	0000	0000	1001			
RETLW k	Return with literal in W	2	11	01xx	kkkk	kkkk			
RETURN -	Return from Subroutine	2	00	0000	0000	1000			
SLEEP -	Go into standby mode	1	00	0000	0110	0011	$\overline{TO}, \overline{PD}$		
SUBLW k	Subtract W from literal	1	11	110x	kkkk	kkkk	C,DC,Z		
XORLW k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z		

Note 1: When an I/O register is modified as a function of itself (e.g., MOVF PORTB, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 Module.

3: If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

NOP		No Operation			
Syntax:	[<i>label</i>] NOP				
Operands:	None				
Operation:	No operation				
Status Affected:	None				
Encoding:	00	0000	0xx0	0000	
Description:	No operation.				
Words:	1				
Cycles:	1				
Q Cycle Activity:	Q1	Q2	Q3	Q4	
	Decode	No-Operation	No-Operation	No-Operation	
Example	NOP				

RETFIE		Return from Interrupt							
Syntax:	[<i>label</i>] RETFIE								
Operands:	None								
Operation:	TOS → PC, 1 → GIE								
Status Affected:	None								
Encoding:	<table border="1"><tr><td>00</td><td>0000</td><td>0000</td><td>1001</td></tr></table>					00	0000	0000	1001
00	0000	0000	1001						
Description:	Return from Interrupt. Stack is POPed and Top of Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a two cycle instruction.								
Words:	1								
Cycles:	2								
Q Cycle Activity:	Q1	Q2	Q3	Q4					
1st Cycle	Decode	No-Operation	Set the GIE bit	Pop from the Stack					
2nd Cycle	No-Operation	No-Operation	No-Operation	No-Operation					
Example	RETFIE								

After Interrupt
PC = TOS
GIE = 1

OPTION	Load Option Register				
Syntax:	[<i>label</i>] OPTION				
Operands:	None				
Operation:	(W) → OPTION				
Status Affected:	None				
Encoding:	<table><tr><td>00</td><td>0000</td><td>0110</td><td>0010</td></tr></table>	00	0000	0110	0010
00	0000	0110	0010		
Description:	<p>The contents of the W register are loaded in the OPTION register. This instruction is supported for code compatibility with PIC16C5X products. Since OPTION is a readable/writable register, the user can directly address it.</p>				
Words:	1				
Cycles:	1				
Example	<div><p>To maintain upward compatibility with future PIC16CXX products, do not use this instruction.</p></div>				

FIGURE 10-4: CLKOUT AND I/O TIMING

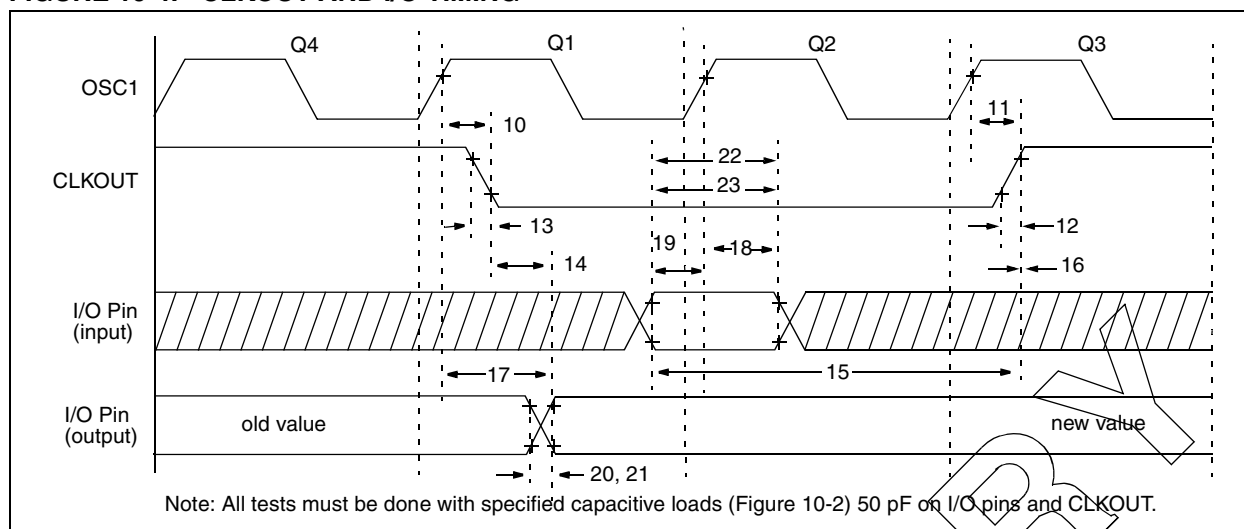


TABLE 10-4 CLKOUT AND I/O TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
10	TosH2ckL	OSC1↑ to CLKOUT↓		15	30 *	ns	Note 1
10A				15	120 *	ns	Note 1
11	TosH2ckH	OSC1↑ to CLKOUT↑		15	30 *	ns	Note 1
11A				15	120 *	ns	Note 1
12	TckR	CLKOUT rise time		15	30 *	ns	Note 1
12A				15	100 *	ns	Note 1
13	TckF	CLKOUT fall time		15	30 *	ns	Note 1
13A				15	100 *	ns	Note 1
14	TckL2ioV	CLKOUT ↓ to Port out valid			0.5TCY + 20 *	ns	Note 1
15	TioV2ckH	Port in valid before CLKOUT ↑	0.30TCY + 30 *			ns	Note 1
			0.30TCY + 80 *			ns	Note 1
16	TckH2iol	Port in hold after CLKOUT ↑	0 *			ns	Note 1
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid			125 *	ns	
					250 *	ns	
18	TosH2iol	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	10 *			ns	
			10 *			ns	
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	-75 *			ns	
			-175 *			ns	
20	TioR	Port output rise time		10	35 *	ns	
20A				10	70 *	ns	
21	TioF	Port output fall time		10	35 *	ns	
21A				10	70 *	ns	
22	Tinp	INT pin high or low time	20 *			ns	
22A			55 *			ns	
23	Trbp	RB7:RB4 change INT high or low time	Tosc §			ns	
23A			Tosc §			ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ By design

Note 1: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

11.4 DC CHARACTERISTICS: PIC16CR84, PIC16CR83 (Commercial, Industrial) PIC16LCR84, PIC16LCR83 (Commercial, Industrial)

DC Characteristics All Pins Except Power Supply Pins			Standard Operating Conditions (unless otherwise stated) Operating temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (commercial) $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial) Operating voltage V_{DD} range as described in DC spec Section 11.1 and Section 11.2.				
Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D100	COSC2	Capacitive Loading Specs on Output Pins OSC2 pin	—	—	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101	CIO	All I/O pins and OSC2 (RC mode)	—	—	50	pF	
D120	Ed	Data EEPROM Memory Endurance	1M	10M	—	E/W	25°C at 5V V_{MIN} = Minimum operating voltage
D121	VDRW	V_{DD} for read/write	V_{MIN}	—	6.0	V	
D122	TDEW	Erase/Write cycle time	—	10	20*	ms	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

TABLE 11-2 TIMING PARAMETER SYMBOLOGY

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

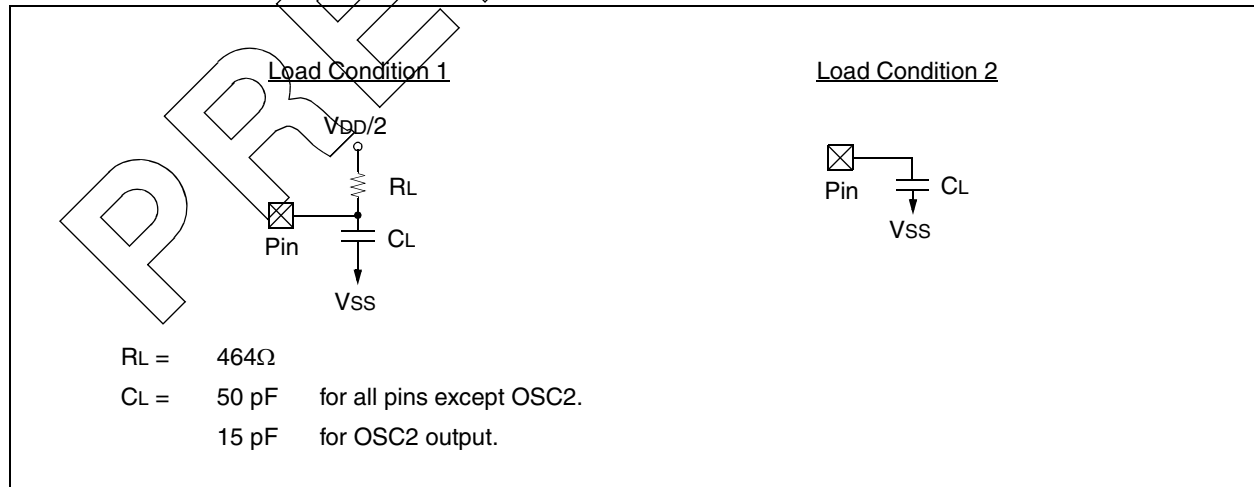
T		T	
F	Frequency	T	Time
Lowercase symbols (pp) and their meanings:			
pp		os,osc	OSC1
2	to	ost	oscillator start-up timer
ck	CLKOUT	pwrt	power-up timer
cy	cycle time	rbt	RBx pins
io	I/O port	t0	T0CKI
inp	INT pin	wdt	watchdog timer
mc	MCLR		
Uppercase symbols and their meanings:			
S		P	Period
F	Fall	R	Rise
H	High	V	Valid
I	Invalid (Hi-impedance)	Z	High Impedance
L	Low		

FIGURE 11-1: PARAMETER MEASUREMENT INFORMATION

All timings are measure between high and low measurement points as indicated in the figures below.



FIGURE 11-2: LOAD CONDITIONS



12.0 DC & AC CHARACTERISTICS GRAPHS/TABLES

The graphs and tables provided in this section are for **design guidance** and are **not tested or guaranteed**.

In some graphs or tables, the data presented are **outside specified operating range** (i.e., outside specified V_{DD} range). This is for **information only** and devices are guaranteed to operate properly only within the specified range.

The data presented in this section is a **statistical summary** of data collected on units from different lots over a period of time and matrix samples. 'Typical' represents the mean of the distribution at 25°C, while 'max' or 'min' represents (mean + 3 σ) and (mean - 3 σ) respectively, where σ is standard deviation.

FIGURE 12-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE

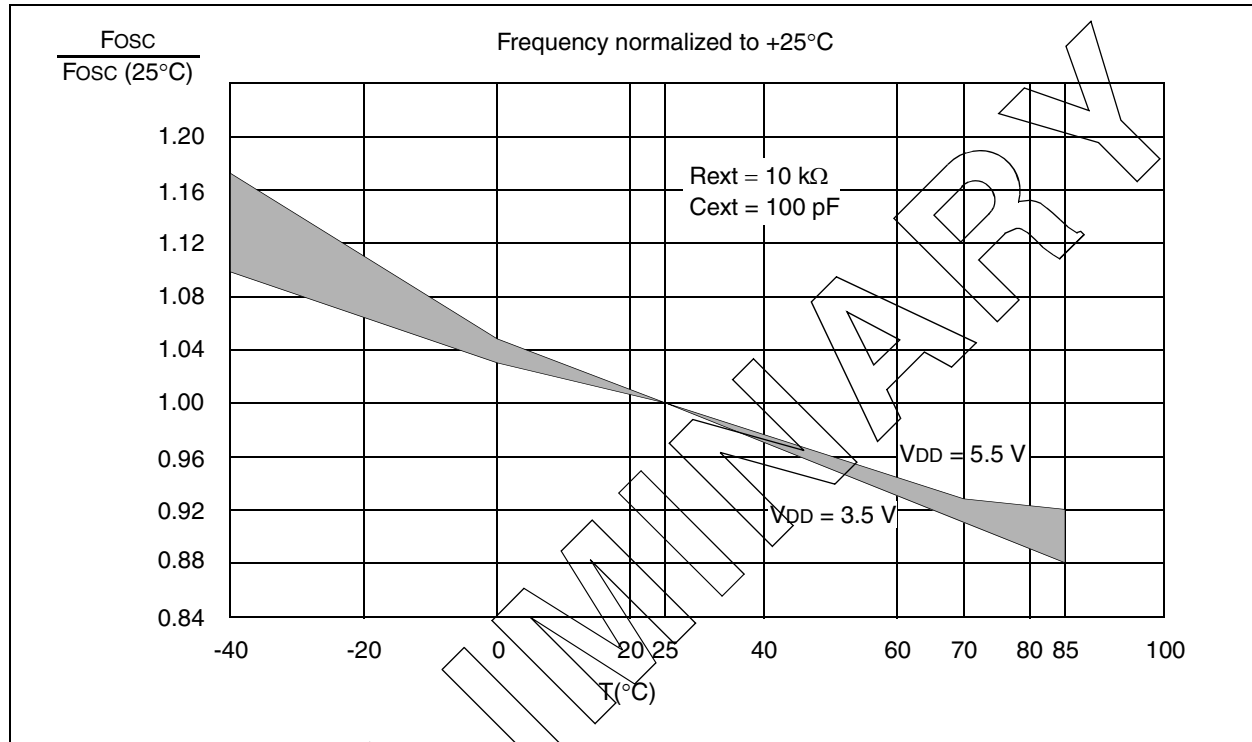


TABLE 12-1 RC OSCILLATOR FREQUENCIES*

Cext	Rext	Average Fosc @ 5V, 25°C	
			Part to Part Variation
20 pF	5 k	4.61 MHz	± 25%
	10 k	2.66 MHz	± 24%
	100 k	311 kHz	± 39%
100 pF	5 k	1.34 MHz	± 21%
	10 k	756 kHz	± 18%
	100 k	82.8 kHz	± 28%
300 pF	5 k	428 kHz	± 13%
	10 k	243 kHz	± 13%
	100 k	26.2 kHz	± 23%

* Measured on DIP packages. The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is ± 3 standard deviation from average value for full V_{DD} range.

FIGURE 12-3: TYPICAL RC OSCILLATOR FREQUENCY vs. V_{DD} , $C_{EXT} = 100$ pF

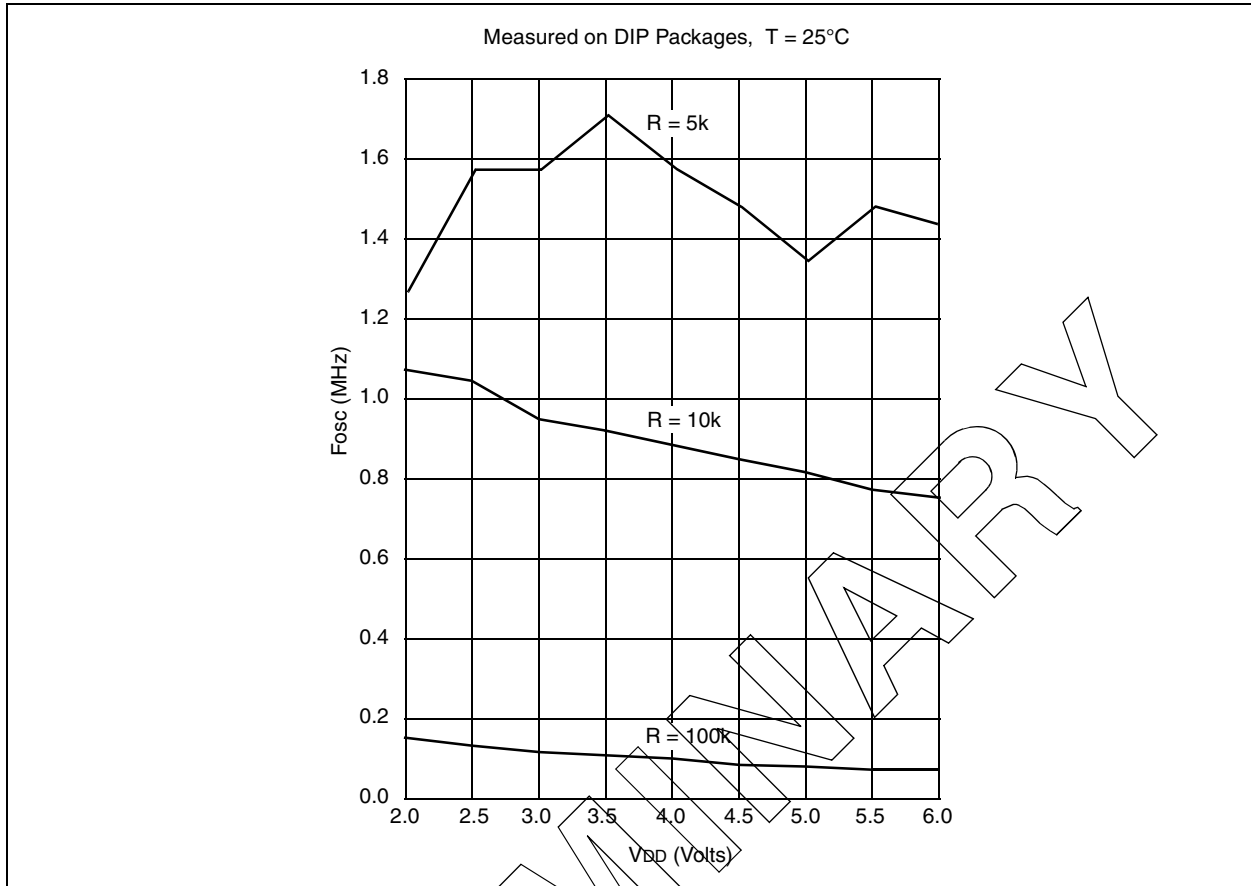


FIGURE 12-4: TYPICAL RC OSCILLATOR FREQUENCY vs. V_{DD} , $C_{EXT} = 300$ pF

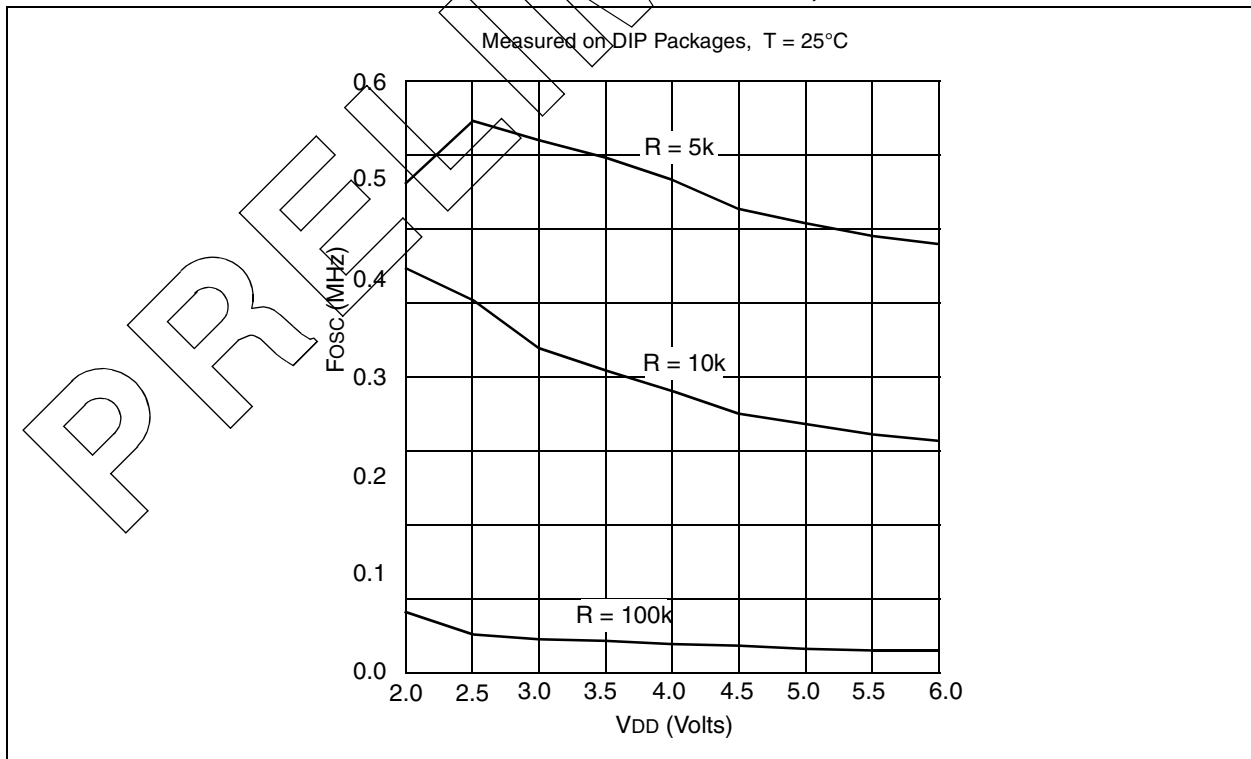


FIGURE 12-21: TYPICAL DATA MEMORY ERASE/WRITE CYCLE TIME VS. VDD

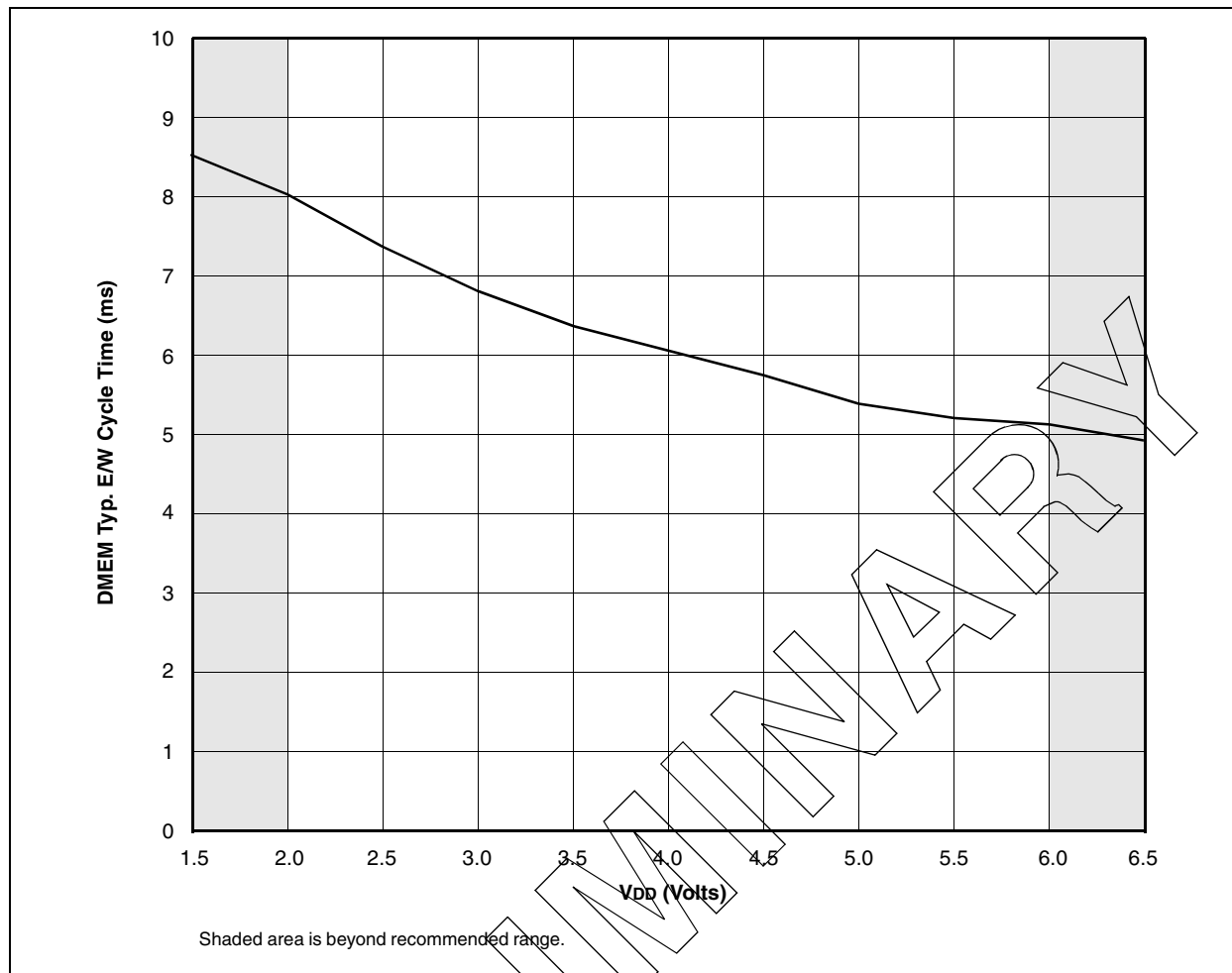


TABLE 12-2 INPUT CAPACITANCE*

Pin Name	Typical Capacitance (pF)	
	18L PDIP	18L SOIC
PORTA	5.0	4.3
PORTB	5.0	4.3
MCLR	17.0	17.0
OSC1/CLKIN	4.0	3.5
OSC2/CLKOUT	4.3	3.5
T0CKI	3.2	2.8

* All capacitance values are typical at 25°C. A part to part variation of $\pm 25\%$ (three standard deviations) should be taken into account.

APPENDIX A: FEATURE IMPROVEMENTS - FROM PIC16C5X TO PIC16F8X

The following is the list of feature improvements over the PIC16C5X microcontroller family:

1. Instruction word length is increased to 14 bits. This allows larger page sizes both in program memory (2K now as opposed to 512 before) and the register file (128 bytes now versus 32 bytes before).
2. A PC latch register (PCLATH) is added to handle program memory paging. PA2, PA1 and PA0 bits are removed from the status register and placed in the option register.
3. Data memory paging is redefined slightly. The STATUS register is modified.
4. Four new instructions have been added: RETURN, RETFIE, ADDLW, and SUBLW. Two instructions, TRIS and OPTION, are being phased out although they are kept for compatibility with PIC16C5X.
5. OPTION and TRIS registers are made addressable.
6. Interrupt capability is added. Interrupt vector is at 0004h.
7. Stack size is increased to 8 deep.
8. Reset vector is changed to 0000h.
9. Reset of all registers is revisited. Five different reset (and wake-up) types are recognized. Registers are reset differently.
10. Wake up from SLEEP through interrupt is added.
11. Two separate timers, the Oscillator Start-up Timer (OST) and Power-up Timer (PWRT), are included for more reliable power-up. These timers are invoked selectively to avoid unnecessary delays on power-up and wake-up.
12. PORTB has weak pull-ups and interrupt on change features.
13. T0CKI pin is also a port pin (RA4/T0CKI).
14. FSR is a full 8-bit register.
15. "In system programming" is made possible. The user can program PIC16CXX devices using only five pins: VDD, VSS, VPP, RB6 (clock) and RB7 (data in/out).

APPENDIX B: CODE COMPATIBILITY - FROM PIC16C5X TO PIC16F8X

To convert code written for PIC16C5X to PIC16F8X, the user should take the following steps:

1. Remove any program memory page select operations (PA2, PA1, PA0 bits) for CALL, GOTO.
2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
3. Eliminate any data memory page switching. Redefine data variables for reallocation.
4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
5. Change reset vector to 0000h.

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www.microchip.com

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The web site and file transfer site provide a variety of services. Users may download files for the latest Development Tools, Data Sheets, Application Notes, User's Guides, Articles and Sample Programs. A variety of Microchip specific business information is also available, including listings of Microchip sales offices, distributors and factory representatives. Other data available for consideration is:

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- Microchip Consultant Program Member Listing
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- Conferences for products, Development Systems, technical information and more
- Listing of seminars and events

PIC16F8X

NOTES: