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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	56800E
Core Size	16-Bit
Speed	120MHz
Connectivity	SCI, SPI, SSI
Peripherals	DMA, POR, WDT
Number of I/O	47
Program Memory Size	80KB (40K x 16)
Program Memory Type	SRAM
EEPROM Size	-
RAM Size	24K x 16
Voltage - Supply (Vcc/Vdd)	1.62V ~ 1.98V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/dsp56857bue

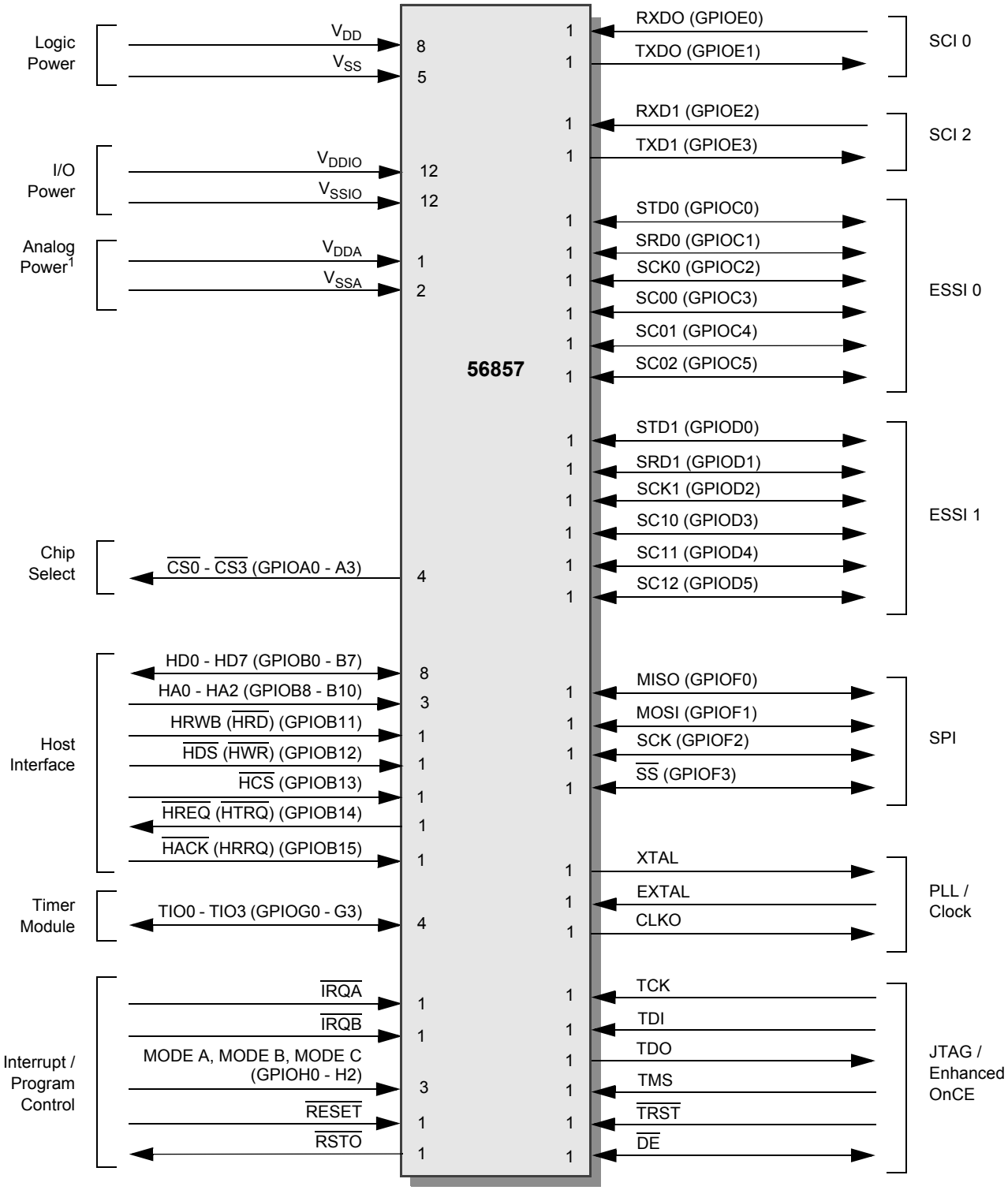


Figure 2-1 56857 Signals Identified by Functional Group[2]

1. Specifically for PLL, OSC, and POR.
2. Alternate pin functions are shown in parentheses.

Table 3-1 56857 Signal and Package Information for the 100-pin LQFP (Continued)

Pin No.	Signal Name	Type	Description
18	V_{SSA}	V_{SSA}	**Analog Ground (V_{SSA})**—This pin supplies an analog ground.
19	V_{SSA}		
55	$\overline{CS0}$ GPIOA0	**Output** **Input**/Output	**External Chip Select ($\overline{CS0}$)**—This pin is used as a dedicated GPIO. **Port A GPIO (0)**—This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
56	$\overline{CS1}$ GPIOA1	**Output** **Input**/Output	**External Chip Select ($\overline{CS1}$)**—This pin is used as a dedicated GPIO. **Port A GPIO (1)**—This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
57	$\overline{CS2}$ GPIOA2	**Output** **Input**/Output	**External Chip Select ($\overline{CS2}$)**—This pin is used as a dedicated GPIO. **Port A GPIO (2)**—This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
58	$\overline{CS3}$ GPIOA3	**Output** **Input**/Output	**External Chip Select ($\overline{CS3}$)**—This pin is used as a dedicated GPIO. **Port A GPIO (3)**—This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
22	HD0 GPIOB0	**Input** Input/Output	**Host Address (HD0)—**This input provides the address selection for HI registers. This pin is disconnected internally. **Port B GPIO (0)**—This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
23	HD1 GPIOB1	**Input** Input/Output	**Host Address (HD1)—**This input provides the address selection for HI registers. This pin is disconnected internally. **Port B GPIO (1)**—This pin is a General Purpose I/O (GPIO) pins when not configured for host port usage.
24	HD2 GPIOB2	**Input** Input/Output	**Host Address (HD2)—**This input provides the address selection for HI registers. This pin is disconnected internally. **Port B GPIO (2)**—This pin is a General Purpose I/O (GPIO) pins when not configured for host port usage.

Table 3-1 56857 Signal and Package Information for the 100-pin LQFP (Continued)

Pin No.	Signal Name	Type	Description
29	HD3	**Input**	**Host Address (HD3)—**This input provides the address selection for HI registers. This pin is disconnected internally.
	GPIOB3	Input/Output	**Port B GPIO (3)**—This pin is a General Purpose I/O (GPIO) pins when not configured for host port usage.
30	HD4	**Input**	**Host Address (HD4)—**This input provides the address selection for HI registers. This pin is disconnected internally.
	GPIOB4	Input/Output	**Port B GPIO (4)**—This pin is a General Purpose I/O (GPIO) pins when not configured for host port usage.
31	HD5	**Input**	**Host Address (HD5)—**This input provides the address selection for HI registers. This pin is disconnected internally.
	GPIOB5	Input/Output	**Port B GPIO (5)**—This pin is a General Purpose I/O (GPIO) pins when not configured for host port usage.
32	HD6	**Input**	**Host Address (HD6)—**This input provides the address selection for HI registers. This pin is disconnected internally.
	GPIOB6	Input/Output	**Port B GPIO (6)**—This pin is a General Purpose I/O (GPIO) pins when not configured for host port usage.
33	HD7	**Input**	**Host Address (HD7)—**This input provides the address selection for HI registers. This pin is disconnected internally.
	GPIOB7	Input/Output	**Port B GPIO (7)**—This pin is a General Purpose I/O (GPIO) pins when not configured for host port usage.
62	HA0	**Input**	**Host Address (HA0)**—This input provides the address selection for HI registers. This pin is disconnected internally.
	GPIOB8	Input/Output	**Port B GPIO (8)**—This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.

Table 3-1 56857 Signal and Package Information for the 100-pin LQFP (Continued)

Pin No.	Signal Name	Type	Description
85	HREQ	**Open Drain Output**	**Host Request (HREQ)**—When the HI08 is programmed for HRMS=0 functionality (typically used on a single-data- strobe bus), this open drain output is used by the HI to request service from the host processor. The HREQ may be connected to an interrupt request pin of a host processor, a transfer request of a DMA controller, or a control input of external circuitry. These pins are disconnected internally.
	HTRQ	**Open Drain Output**	**Transmit Host Request (HTRQ)**—This signal is the Transmit Host Request output when the HI08 is programmed for HRMS=1 functionality and is typically used on a double-data-strobe bus.
	GPIOB14	Input/Output	**Port B GPIO (14)** —This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
86	HACK	**Input**	**Host Acknowledge (HACK)**—When the HI08 is programmed for HRMS=0 functionality (typically used on a single-data-strobe bus), this input has two functions: (1) provide a Host Acknowledge signal for DMA transfers or (2) to control handshaking and provide a Host Interrupt Acknowledge compatible with the MC68000 family processors. These pins are disconnected internally during reset.
	HRRQ	Open Drain Output	**Receive Host Request (HRRQ)**—This signal is the Receive Host Request output when the HI08 is programmed for HRMS=1 functionality and is typically used on a double-data-strobe bus.
	GPIOB15	Input/Output	**Port B GPIO (15)**—This pin is a General Purpose I/O (GPIO) pin when not configured for host port usage.
81	TIO0	**Input**/Output	**Timer Input/Output (TIO0)**—This pin can be independently configured to be either a timer input source or an output flag.
	GPIOG0	Input/Output	**Port G GPIO (0)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as an input or output pin.
79	TIO1	**Input**/Output	**Timer Input/Output (TIO1)**—This pin can be independently configured to be either a timer input source or an output flag.
	GPIOG1	Input/Output	**Port G GPIO (1)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as an input or output pin.
78	TIO2	**Input**/Output	**Timer Input/Output (TIO2)**—This pin can be independently configured to be either a timer input source or an output flag.
	GPIOG2	Input/Output	**Port G GPIO (2)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as an input or output pin.

Table 3-1 56857 Signal and Package Information for the 100-pin LQFP (Continued)

Pin No.	Signal Name	Type	Description
52	TXD0	**Output(Z)**	**Serial Transmit Data 0 (TXD0)**—This signal transmits data from the SCI 0 transmit data register.
	GPIOE1	Input/Output	**Port E GPIO (1)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.
74	RXD1	**Input**	**Serial Receive Data 1 (RXD1)**—This input receives byte-oriented serial data and transfers it to the SCI 1 receive shift register.
	GPIOE2	Input/Output	**Port E GPIO (2)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.
75	TXD1	**Output(Z)**	**Serial Transmit Data 1 (TXD1)**—This signal transmits data from the SCI 1 transmit data register.
	GPIOE3	Input/Output	**Port E GPIO (3)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.
92	STD0	Output	**ESSI Transmit Data (STD0)**—This output pin transmits serial data from the ESSI Transmitter Shift Register.
	GPIOC0	**Input**/Output	**Port C GPIO (0)**—This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
93	SRD0	Input	**ESSI Receive Data (SRD0)**—This input pin receives serial data and transfers the data to the ESSI Receive Shift Register.
	GPIOC1	**Input**/Output	**Port C GPIO (1)**—This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
94	SCK0	**Input**/Output	**ESSI Serial Clock (SCK0)**—This bidirectional pin provides the serial bit rate clock for the transmit section of the ESSI. The clock signal can be continuous or gated and can be used by both the transmitter and receiver in synchronous mode.
	GPIOC2	Input/Output	**Port C GPIO (2)**—This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
95	SC00	**Input**/Output	**ESSI Serial Control Pin 0 (SC00)**—The function of this pin is determined by the selection of either synchronous or asynchronous mode. For asynchronous mode, this pin will be used for the receive clock I/O. For synchronous mode, this pin is used either for transmitter1 output or for serial I/O flag 0.
	GPIOC3	Input/Output	**Port C GPIO (3)**—This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.

Table 3-1 56857 Signal and Package Information for the 100-pin LQFP (Continued)

Pin No.	Signal Name	Type	Description
96	SC01	**Input**/Output	**ESSI Serial Control Pin 1 (SC01)**—The function of this pin is determined by the selection of either synchronous or asynchronous mode. For asynchronous mode, this pin is the receiver frame sync I/O. For synchronous mode, this pin is used either for transmitter2 output or for serial I/O flag 1.
	GPIOC4	Input/Output	**Port C GPIO (4)**—This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
97	SC02	**Input**/Output	**ESSI Serial Control Pin 2 (SC02)**—This pin is used for frame sync I/O. SC02 is the frame sync for both the transmitter and receiver in synchronous mode and for the transmitter only in asynchronous mode. When configured as an output, this pin is the internally generated frame sync signal. When configured as an input, this pin receives an external frame sync signal for the transmitter (and the receiver in synchronous operation).
	GPIOC5	Input/Output	**Port C GPIO (5)**—This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
66	STD1	Output	**ESSI Transmit Data (STD1)**—This output pin transmits serial data from the ESSI Transmitter Shift Register.
	GPIOD0	**Input**/Output	**Port D GPIOD0**—This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
67	SRD1	Input	**ESSI Receive Data (SRD1)**—This input pin receives serial data and transfers the data to the ESSI Receive Shift Register.
	GPIOD1	**Input**/Output	**Port D GPIO (1)**—This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
68	SCK1	**Input**/Output	**ESSI Serial Clock (SCK1)**—This bidirectional pin provides the serial bit rate clock for the transmit section of the ESSI. The clock signal can be continuous or gated and can be used by both the transmitter and receiver in synchronous mode.
	GPIOD2	Input/Output	**Port D GPIO (2)**—This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.
69	SC10	**Input**/Output	**ESSI Serial Control Pin 0 (SC10)**—The function of this pin is determined by the selection of either synchronous or asynchronous mode. For asynchronous mode, this pin will be used for the receive clock I/O. For synchronous mode, this pin is used either for transmitter1 output or for serial I/O flag 0.
	GPIOD3	Input/Output	**Port D GPIO (3)**—This pin is a General Purpose I/O (GPIO) pin when the ESSI is not in use.

Table 4-1 Absolute Maximum Ratings

Characteristic	Symbol	Min	Max	Unit
Supply voltage, core	V_{DD}[1]	V_{SS} – 0.3	V_{SS} + 2.0	V
Supply voltage, IO Supply voltage, analog	V_{DDIO}[2] V_{DDIO}[2]	V_{SSIO} – 0.3 V_{SSA} – 0.3	V_{SSIO} + 4.0 V_{DDA} + 4.0	V
Digital input voltages Analog input voltages (XTAL, EXTAL)	V_{IN} V_{INA}	V_{SSIO} – 0.3 V_{SSA} – 0.3	V_{SSIO} + 5.5 V_{DDA} + 0.3	V
Current drain per pin excluding V_{DD}, GND	I	—	8	mA
Junction temperature	T_J	-40	120	°C
Storage temperature range	T_{STG}	-55	150	°C

1. V_{DD} must not exceed V_{DDIO}
2. V_{DDIO} and V_{DDA} must not differ by more that 0.5V

Table 4-2 Recommended Operating Conditions

Characteristic	Symbol	Min	Max	Unit
Supply voltage for Logic Power	V_{DD}	1.62	1.98	V
Supply voltage for I/O Power	V_{DDIO}	3.0	3.6	V
Supply voltage for Analog Power	V_{DDA}	3.0	3.6	V
Ambient operating temperature	T_A	-40	85	°C
PLL clock frequency[1]	f_{pll}	—	240	MHz
Operating Frequency[2]	f_{op}	—	120	MHz
Frequency of peripheral bus	f_{ipb}	—	60	MHz
Frequency of external clock	f_{clk}	—	240	MHz
Frequency of oscillator	f_{osc}	2	4	MHz
Frequency of clock via XTAL	f_{xtal}	—	240	MHz
Frequency of clock via EXTAL	f_{extal}	2	4	MHz

1. Assumes clock source is direct clock to EXTAL or crystal oscillator running 2-4MHz. PLL must be enabled, locked, and selected. The actual frequency depends on the source clock frequency and programming of the CGM module.
2. Master clock is derived from on of the following four sources:
   $f_{clk} = f_{xtal}$ when the source clock is the direct clock to EXTAL
   $f_{clk} = f_{pll}$ when PLL is selected
   $f_{clk} = f_{osc}$ when the source clock is the crystal oscillator and PLL is not selected
   $f_{clk} = f_{extal}$ when the source clock is the direct clock to EXTAL and PLL is not selected

Table 4-3 Thermal Characteristics[1]

Characteristic	100-pin LQFP		
	Symbol	Value	Unit
Thermal resistance junction-to-ambient (estimated)	θ_{JA}	41.2	°C/W
I/O pin power dissipation	$P_{I/O}$	User Determined	W
Power dissipation	P_D	$P_D = (I_{DD} \times V_{DD}) + P_{I/O}$	W
Maximum allowed P_D	P_{DMAX}	$(T_J - T_A) / R\theta_{JA}$ [2]	W

1. See **Section 6.1** for more detail.
2. TJ = Junction Temperature
   TA = Ambient Temperature

4.2 DC Electrical Characteristics

Table 4-4 DC Electrical Characteristics

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62$-1.98V, $V_{DDIO} = V_{DDA} = 3.0$–3.6V, $T_A = -40°$ to $+120°$C, $C_L \leq 50$pF, $f_{op} = 120$MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Input high voltage (XTAL/EXTAL)	V_{IHC}	$V_{DDA} - 0.8$	V_{DDA}	$V_{DDA} + 0.3$	V
Input low voltage (XTAL/EXTAL)	V_{ILC}	-0.3	—	0.5	V
Input high voltage	V_{IH}	2.0	—	5.5	V
Input low voltage	V_{IL}	-0.3	—	0.8	V
Input current low (pullups disabled)	I_{IL}	-1	—	1	µA
Input current high (pullups disabled)	I_{IH}	-1	—	1	µA
Output tri-state current low	I_{OZL}	-10	—	10	µA
Output tri-state current high	I_{OZH}	-10	—	10	µA
Output High Voltage	V_{OH}	$V_{DDIO} - 0.7$	—	—	V
Output Low Voltage	V_{OL}	—	—	0.4	V
Output High Current	I_{OH}	8	—	16	mA
Output Low Current	I_{OL}	8	—	16	mA
Input capacitance	C_{IN}	—	8	—	pF
Output capacitance	C_{OUT}	—	12	—	pF
V_{DD} supply current (Core logic, memories, peripherals)	I_{DD} [4]				
Run [1]		—	70	110	mA
Deep Stop[2]		—	0.05	10	mA
Light Stop[3]		—	5	14	mA

Table 4-4 DC Electrical Characteristics (Continued)

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62$-1.98V, $V_{DDIO} = V_{DDA} = 3.0$–3.6V, $T_A = -40°$ to $+120°$C, $C_L \leq 50$pF, $f_{op} = 120$MHz

Characteristic	Symbol	Min	Typ	Max	Unit
V_{DDIO} supply current (I/O circuity) Run[5] Deep Stop[2]	I_{DDIO}	—	 40 0	 50 1.5	 mA mA
V_{DDA} supply current (analog circuity) Deep Stop[2]	I_{DDA}	—	 60	 120	 μA
Low Voltage Interrupt[6]	V_{EI}	—	2.5	2.85	V
Low Voltage Interrupt Recovery Hysteresis	V_{EIH}	—	50	—	mV
Power on Reset[7]	POR	—	1.5	2.0	V

Note: Run (operating) I_{DD} measured using external square wave clock source (f_{osc} = 4MHz) into XTAL. All inputs 0.2V from rail; no DC loads; outputs unloaded. All ports configured as inputs; measured with all modules enabled. PLL set to 240MHz out.

1. Running Core, performing 50% NOP and 50% FIR. Clock at 120 MHz.
2. Deep Stop Mode - Operation frequency = 4 MHz, PLL set to 4 MHz, crystal oscillator and time of day module operating.
3. Light Stop Mode - Operation frequency = 120 MHz, PLL set to 240 MHz, crystal oscillator and time of day module operating.
4. I_{DD} includes current for core logic, internal memories, and all internal peripheral logic circuitry.
5. Running core and performing external memory access. Clock at 120 MHz.
6. When V_{DD} drops below V_{EI} max value, an interrupt is generated.
7. Power-on reset occurs whenever the digital supply drops below 1.8V. While power is ramping up, this signal remains active for as long as the internal 2.5V is below 1.8V no matter how long the ramp up rate is. The internally regulated voltage is typically 100 mV less than V_{DD} during ramp up until 2.5V is reached, at which time it self-regulates.

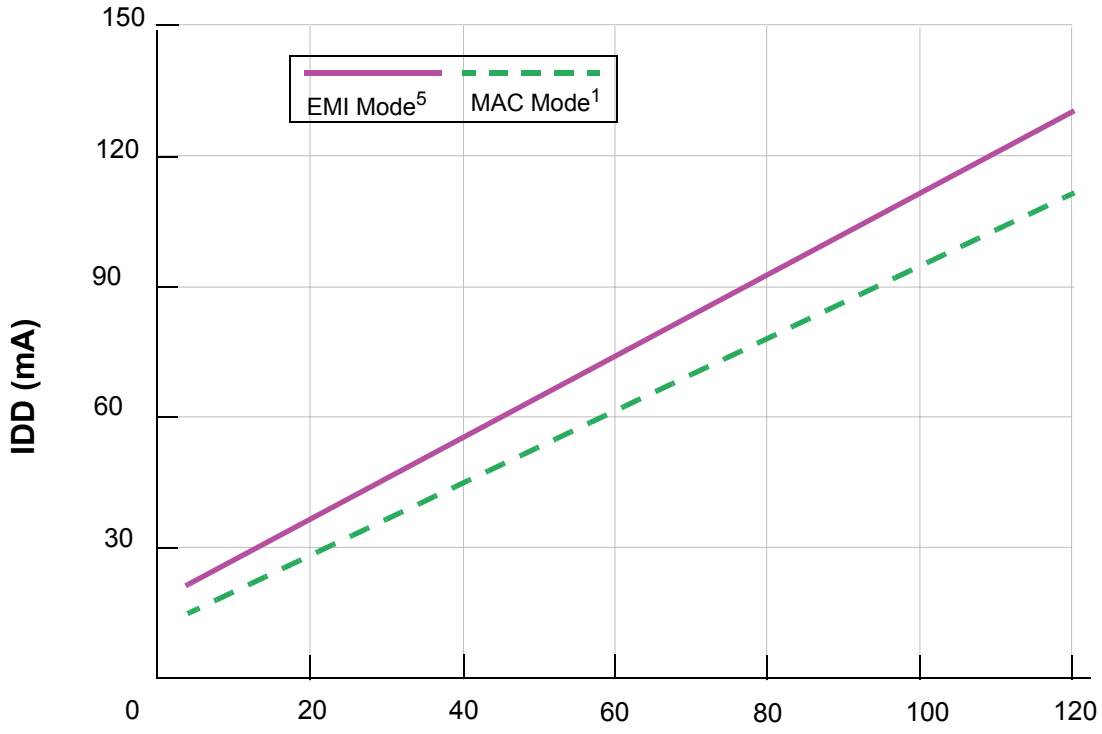
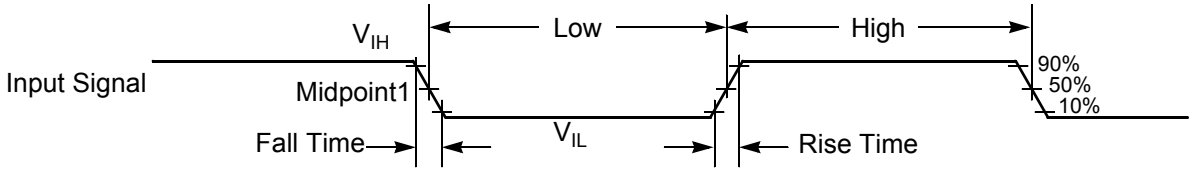


Figure 4-1 Maximum Run $I_{DDTOTAL}$ vs. Frequency (see Notes 1. and 5. in Table 4-4)

4.4 AC Electrical Characteristics

Timing waveforms in Section 4.4 are tested with a V_{IL} maximum of 0.8V and a V_{IH} minimum of 2.0V for all pins except XTAL, which is tested using the input levels in Section 4.2. In Figure 4-4 the levels of V_{IH} and V_{IL} for an input signal are shown.



Note: The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

Figure 4-4 Input Signal Measurement References

Figure 4-5 shows the definitions of the following signal states:

- Active state, when a bus or signal is driven, and enters a low impedance state
- Tri-stated, when a bus or signal is placed in a high impedance state
- Data Valid state, when a signal level has reached V_{OL} or V_{OH}
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}

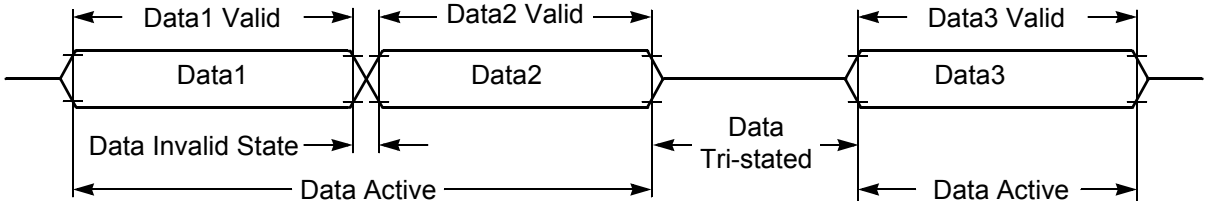


Figure 4-5 Signal States

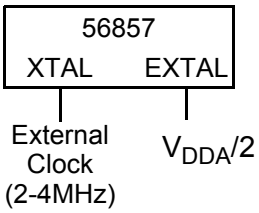


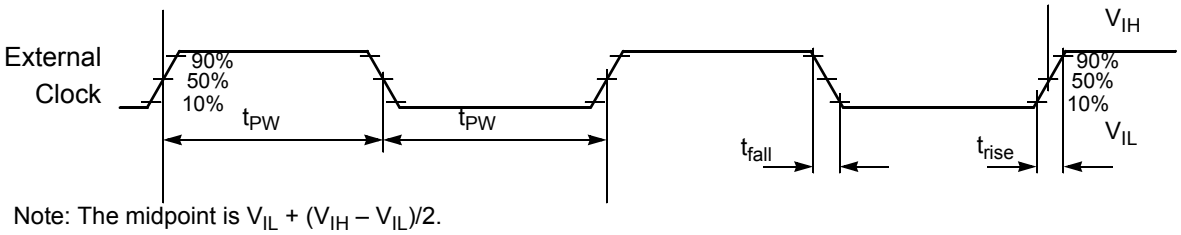
Figure 4-8 Connecting a Low Speed External Clock Signal using XTAL

Table 4-5 External Clock Operation Timing Requirements[4]

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62\text{-}1.98$V, $V_{DDIO} = V_{DDA} = 3.0\text{–}3.6$V, $T_A = -40°$ to $+120°$C, $C_L \leq 50$pF, $f_{op} = 120$MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation (external clock driver)[1]	f_{osc}	0	—	240	MHz
Clock Pulse Width[4]	t_{PW}	6.25	—	—	ns
External clock input rise time[2, 4]	t_{rise}	—	—	TBD	ns
External clock input fall time[3, 4]	t_{fall}	—	—	TBD	ns

1. See **Figure 4-7** for details on using the recommended connection of an external clock driver.
2. External clock input rise time is measured from 10% to 90%.
3. External clock input fall time is measured from 90% to 10%.
4. Parameters listed are guaranteed by design.



Note: The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

Figure 4-9 External Clock Timing

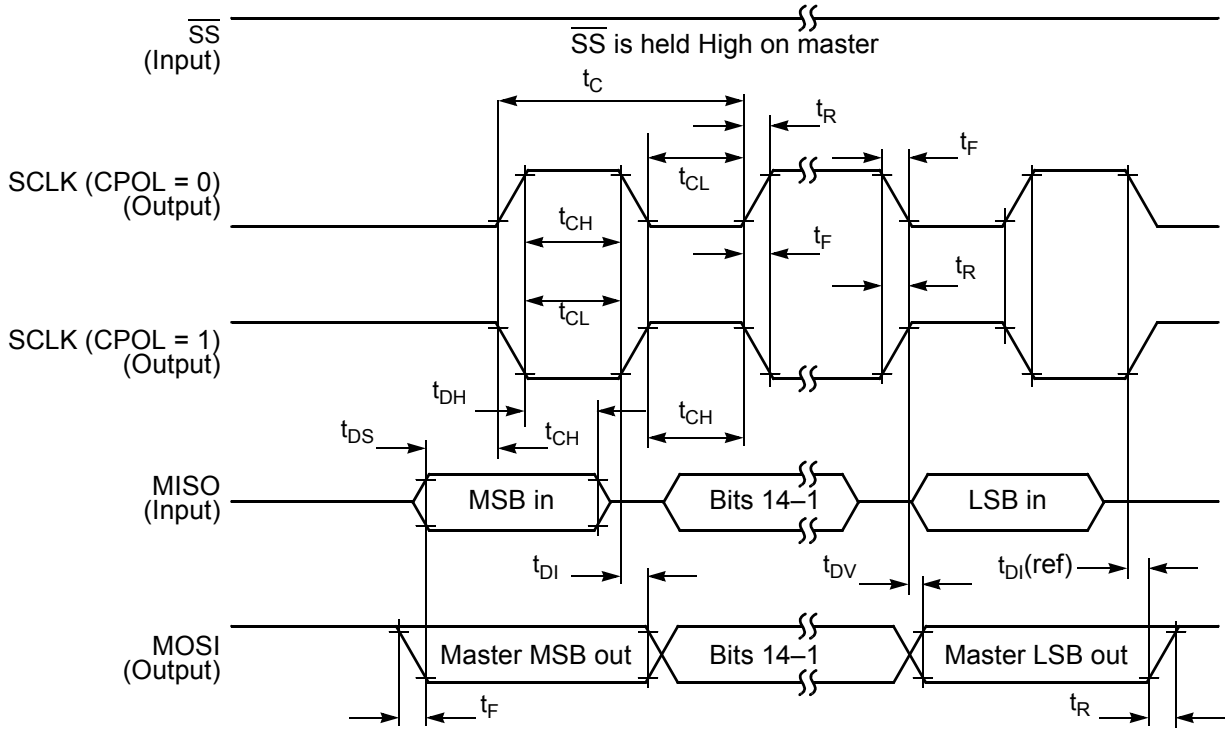


Figure 4-21 SPI Master Timing (CPHA = 0)

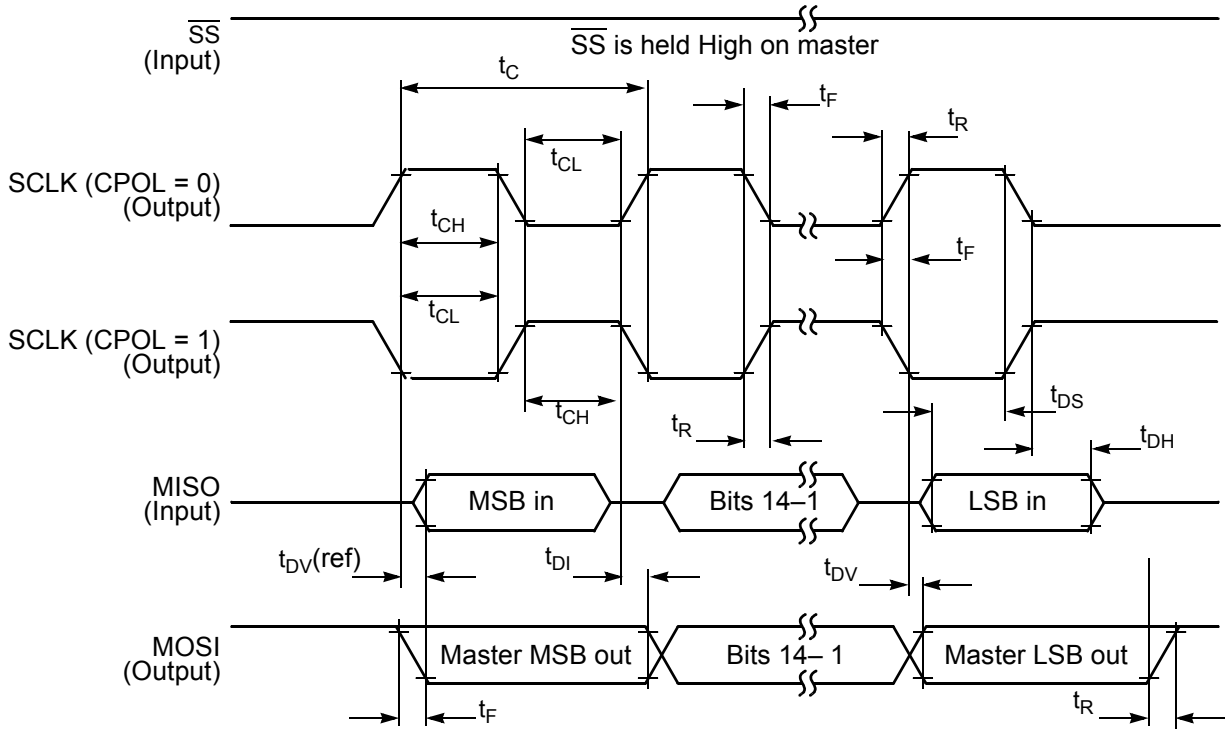


Figure 4-22 SPI Master Timing (CPHA = 1)

Table 4-11 ESSI Master Mode[1] Switching Characteristics (Continued)

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62\text{-}1.98$V, $V_{DDIO} = V_{DDA} = 3.0\text{–}3.6$V, $T_A = -40°$ to $+120°$C, $C_L \leq 50$pF, $f_{op} = 120$MHz

Parameter	Symbol	Min	Typ	Max	Units
Delay from SCK high to SC2 (bl) high - Master[5]	t_{TFSBHM}	-1.0	—	1.0	ns
Delay from SCK high to SC2 (wl) high - Master[5]	t_{TFSWHM}	-1.0	—	1.0	ns
Delay from SC0 high to SC1 (bl) high - Master[5]	t_{RFSBHM}	-1.0	—	1.0	ns
Delay from SC0 high to SC1 (wl) high - Master[5]	t_{RFSWHM}	-1.0	—	1.0	ns
Delay from SCK high to SC2 (bl) low - Master[5]	t_{TFSBLM}	-1.0	—	1.0	ns
Delay from SCK high to SC2 (wl) low - Master[5]	t_{TFSWLM}	-1.0	—	1.0	ns
Delay from SC0 high to SC1 (bl) low - Master[5]	t_{RFSBLM}	-1.0	—	1.0	ns
Delay from SC0 high to SC1 (wl) low - Master[5]	t_{RFSWLM}	-1.0	—	1.0	ns
SCK high to STD enable from high impedance - Master	t_{TXEM}	-0.1	—	2	ns
SCK high to STD valid - Master	t_{TXVM}	-0.1	—	2	ns
SCK high to STD not valid - Master	t_{TXNVM}	-0.1	—	—	ns
SCK high to STD high impedance - Master	t_{TXHIM}	-4	—	0	ns
SRD Setup time before SC0 low - Master	t_{SM}	4	—	—	ns
SRD Hold time after SC0 low - Master	t_{HM}	4	—	—	ns
Synchronous Operation (in addition to standard internal clock parameters)					
SRD Setup time before SCK low - Master	t_{TSM}	4	—	—	ns
SRD Hold time after SCK low - Master	t_{THM}	4	—	—	ns

1. Master mode is internally generated clocks and frame syncs
2. Max clock frequency is IP_clk/4 = 60MHz / 4 = 15MHz for an 120MHz part.
3. All the timings for the ESSI are given for a non-inverted serial clock polarity (TSCKP=0 in SCR2 and RSCKP=0 in SCSR) and a non-inverted frame sync (TFSI=0 in SCR2 and RFSI=0 in SCSR). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal SCK/SC0 and/or the frame sync SC2/SC1 in the tables and in the figures.
4. 50 percent duty cycle
5. bl = bit length; wl = word length

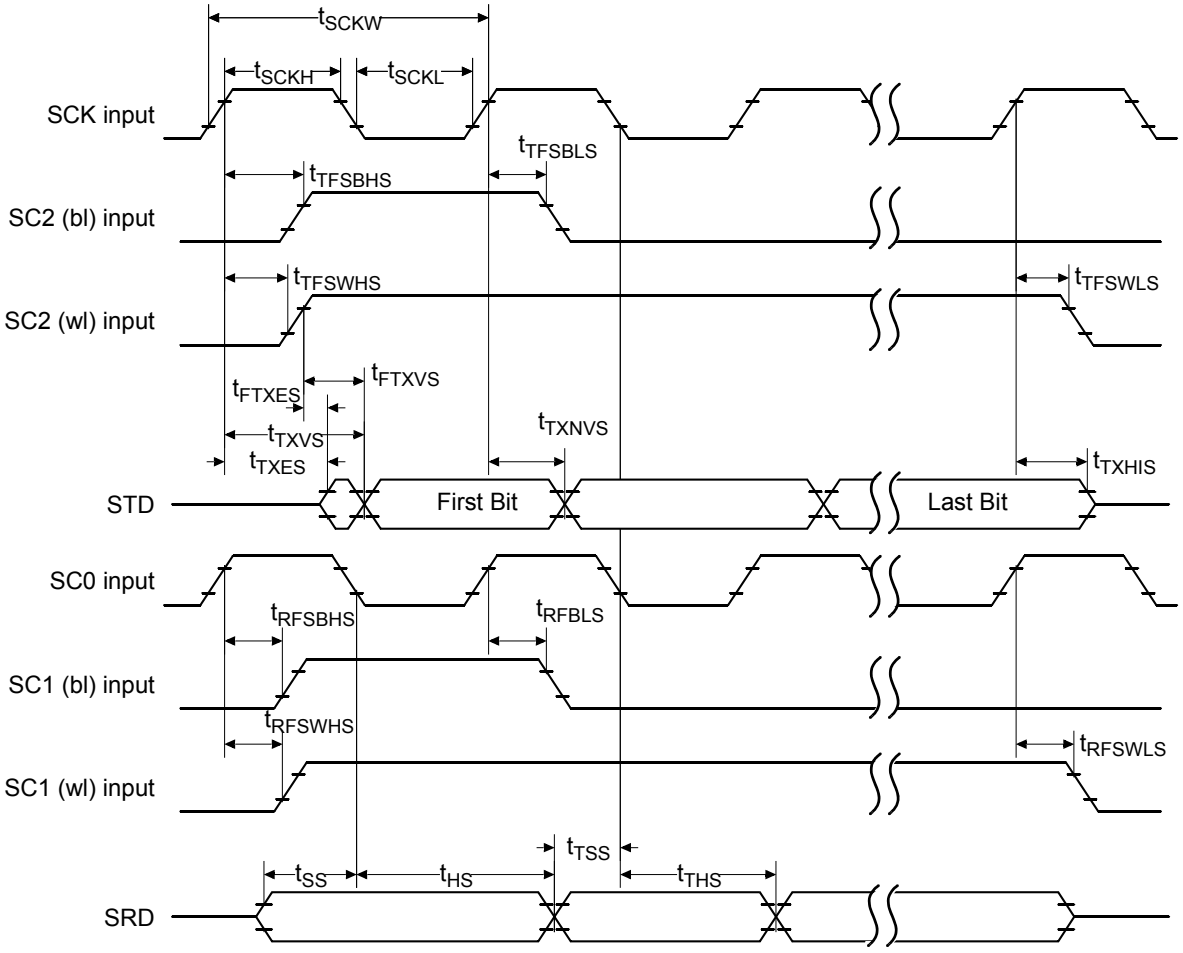


Figure 4-27 Slave Mode Clock Timing

4.11 Serial Communication Interface (SCI) Timing

Table 4-13 SCI Timing[4]

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62\text{-}1.98$V, $V_{DDIO} = V_{DDA} = 3.0\text{–}3.6$V, $T_A = -40°$ to $+120°$C, $C_L \leq 50$pF, $f_{op} = 120$MHz

Characteristic	Symbol	Min	Max	Unit
Baud Rate[1]	BR	—	$(f_{MAX})/(32)$	Mbps
RXD[2] Pulse Width	RXD_{PW}	0.965/BR	1.04/BR	ns
TXD[3] Pulse Width	TXD_{PW}	0.965/BR	1.04/BR	ns

1. f_{MAX} is the frequency of operation of the system clock in MHz.
2. The RXD pin in SCI0 is named RXD0 and the RXD pin in SCI1 is named RXD1.
3. The TXD pin in SCI0 is named TXD0 and the TXD pin in SCI1 is named TXD1.
4. Parameters listed are guaranteed by design.

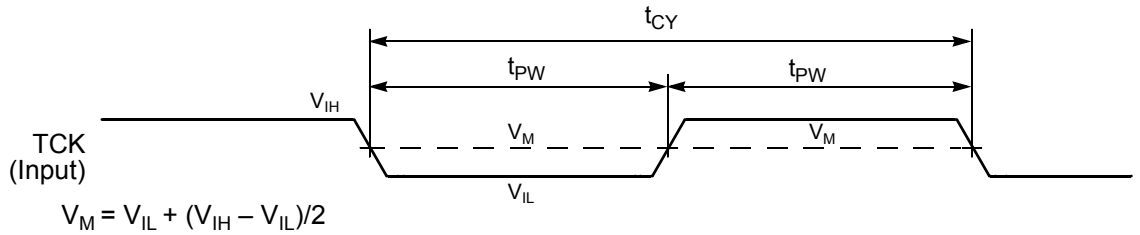


Figure 4-30 Test Clock Input Timing Diagram

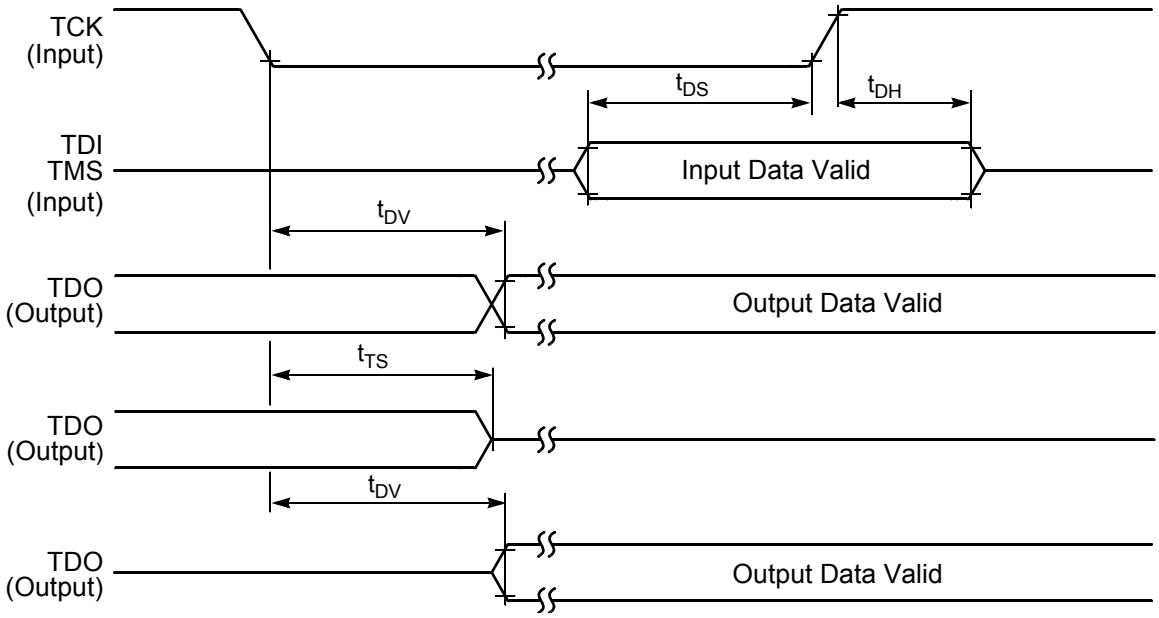


Figure 4-31 Test Access Port Timing Diagram

Figure 4-32 $\overline{\text{TRST}}$ Timing Diagram

Figure 4-33 Enhanced OnCE—Debug Event

4.13 GPIO Timing

Table 4-15 GPIO Timing[1, 2]

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62\text{-}1.98$V, $V_{DDIO} = V_{DDA} = 3.0\text{–}3.6$V, $T_A = -40°$ to $+120°$C, $C_L \leq 50$pF, $f_{op} = 120$MHz

Characteristic	Symbol	Min	Max	Unit
GPIO input period	P_{IN}	2T + 3	—	ns
GPIO input high/low period	P_{INHL}	1T + 3	—	ns
GPIO output period	P_{OUT}	2T - 3	—	ns
GPIO output high/low period	P_{OUTHL}	1T - 3	—	ns

1. In the formulas listed, T = clock cycle. For $f_{op} = 120$MHz operation and fipb = 60MHz, T = 8.33ns
2. Parameters listed are guaranteed by design.

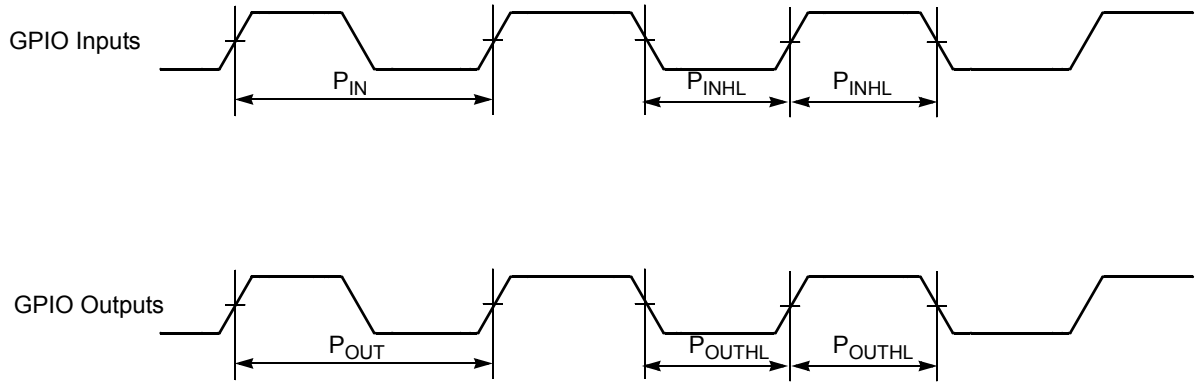


Figure 4-34 GPIO Timing

Part 5 Packaging

5.1 Package and Pin-Out Information 56857

This section contains package and pin-out information for the 100-pin LQFP configuration of the 56857.

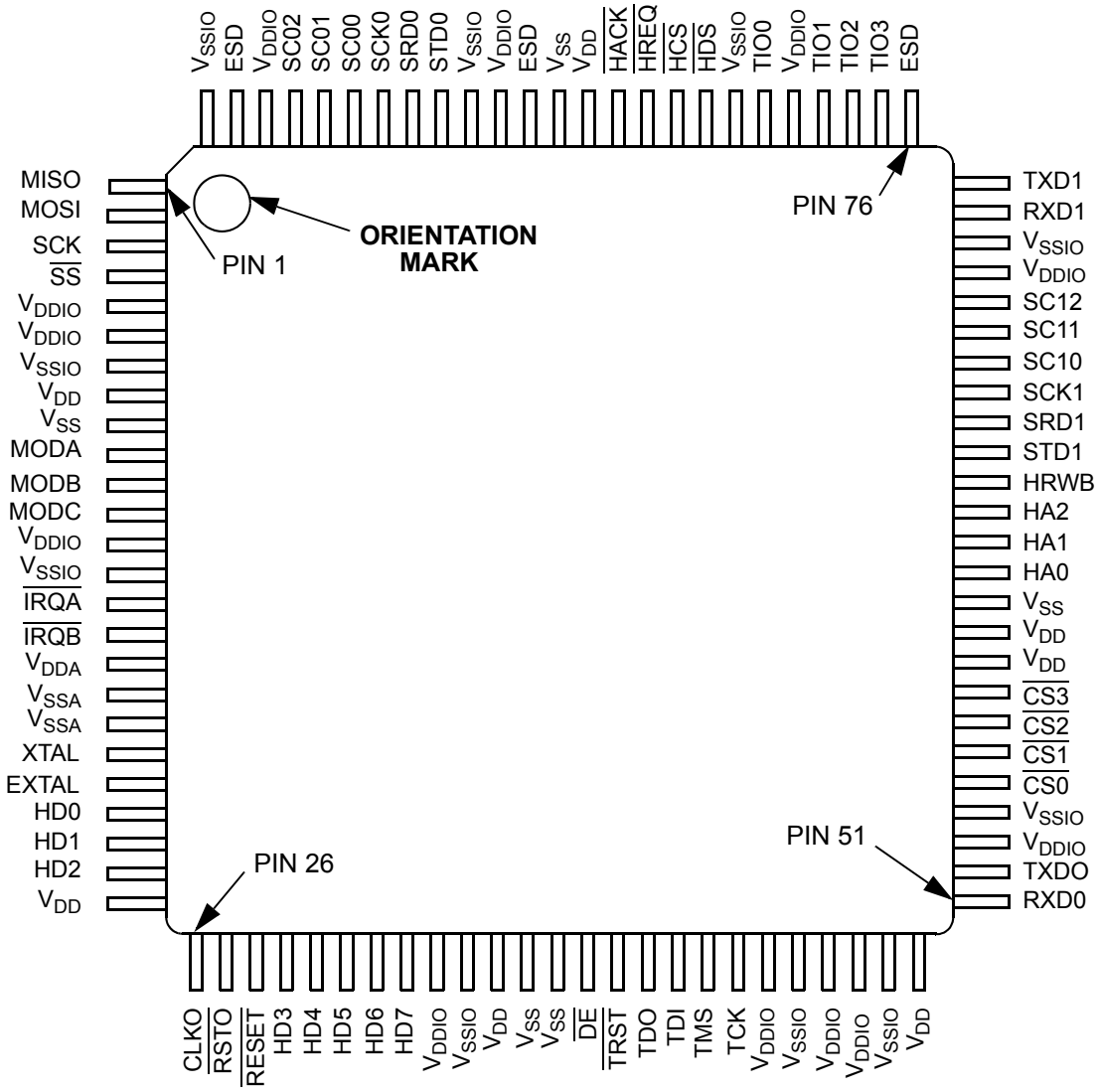


Figure 5-1 Top View, 56857 100-pin LQFP Package

Part 6 Design Considerations

6.1 Thermal Design Considerations

An estimation of the chip junction temperature, T_J, in °C can be obtained from the equation:

Equation 1: $T_J = T_A + (P_D \times R_{\theta JA})$

Where:

T_A = ambient temperature °C
$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W
P_D = power dissipation in package

Historically, thermal resistance has been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

Equation 2: $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

Where:

$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W
$R_{\theta JC}$ = package junction-to-case thermal resistance °C/W
$R_{\theta CA}$ = package case-to-ambient thermal resistance °C/W

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the Printed Circuit Board (PCB), or otherwise change the thermal dissipation capability of the area surrounding the device on the PCB. This model is most useful for ceramic packages with heat sinks; some 90% of the heat flow is dissipated through the case to the heat sink and out to the ambient environment. For ceramic packages, in situations where the heat flow is split between a path to the case and an alternate path through the PCB, analysis of the device thermal performance may need the additional modeling capability of a system level thermal simulation tool.

The thermal performance of plastic packages is more dependent on the temperature of the PCB to which the package is mounted. Again, if the estimations obtained from $R_{\theta JA}$ do not satisfactorily answer whether the thermal performance is adequate, a system level model may be appropriate.

A complicating factor is the existence of three common definitions for determining the junction-to-case thermal resistance in plastic packages:

- Measure the thermal resistance from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink. This is done to minimize temperature variation across the surface.
- Measure the thermal resistance from the junction to where the leads are attached to the case. This definition is approximately equal to a junction to board thermal resistance.
- Use the value obtained by the equation $(T_J - T_T)/P_D$ where T_T is the temperature of the package case determined by a thermocouple.

As noted above, the junction-to-case thermal resistances quoted in this data sheet are determined using the first definition. From a practical standpoint, that value is also suitable for determining the junction temperature from a case thermocouple reading in forced convection environments. In natural convection, using the junction-to-case thermal resistance to estimate junction temperature from a thermocouple reading on the case of the package will estimate a junction temperature slightly hotter than actual. Hence, the new thermal metric, Thermal Characterization Parameter, or Ψ_{JT}, has been defined to be $(T_J - T_T)/P_D$. This value gives a better estimate of the junction temperature in natural convection when using the surface temperature of the package. Remember that surface temperature readings of packages are subject to significant errors caused by inadequate attachment of the sensor to the surface and to errors caused by heat loss to the sensor. The recommended technique is to attach a 40-gauge thermocouple wire and bead to the top center of the package with thermally conductive epoxy.

6.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct operation:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the controller, and from the board ground to each V_{SS} (GND) pin.
- The minimum bypass requirement is to place six 0.01–0.1 µF capacitors positioned as close as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the ten V_{DD}/V_{SS} pairs, including V_{DDA}/V_{SSA}.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} (GND) pins are less than 0.5 inch per capacitor lead.
- Use at least a four-layer Printed Circuit Board (PCB) with two inner layers for V_{DD} and GND.
- Bypass the V_{DD} and GND layers of the PCB with approximately 100 µF, preferably with a high-grade capacitor such as a tantalum capacitor.
- Because the device's output signals have fast rise and fall times, PCB trace lengths should be minimal.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and GND circuits.
- All inputs must be terminated (i.e., not allowed to float) using CMOS levels.

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