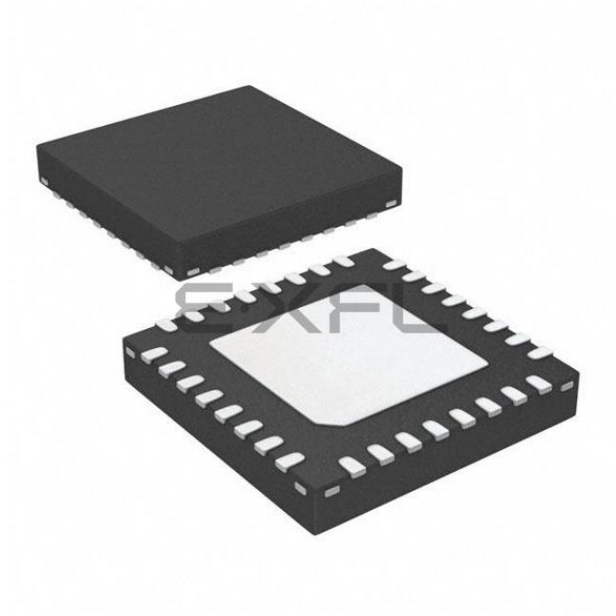

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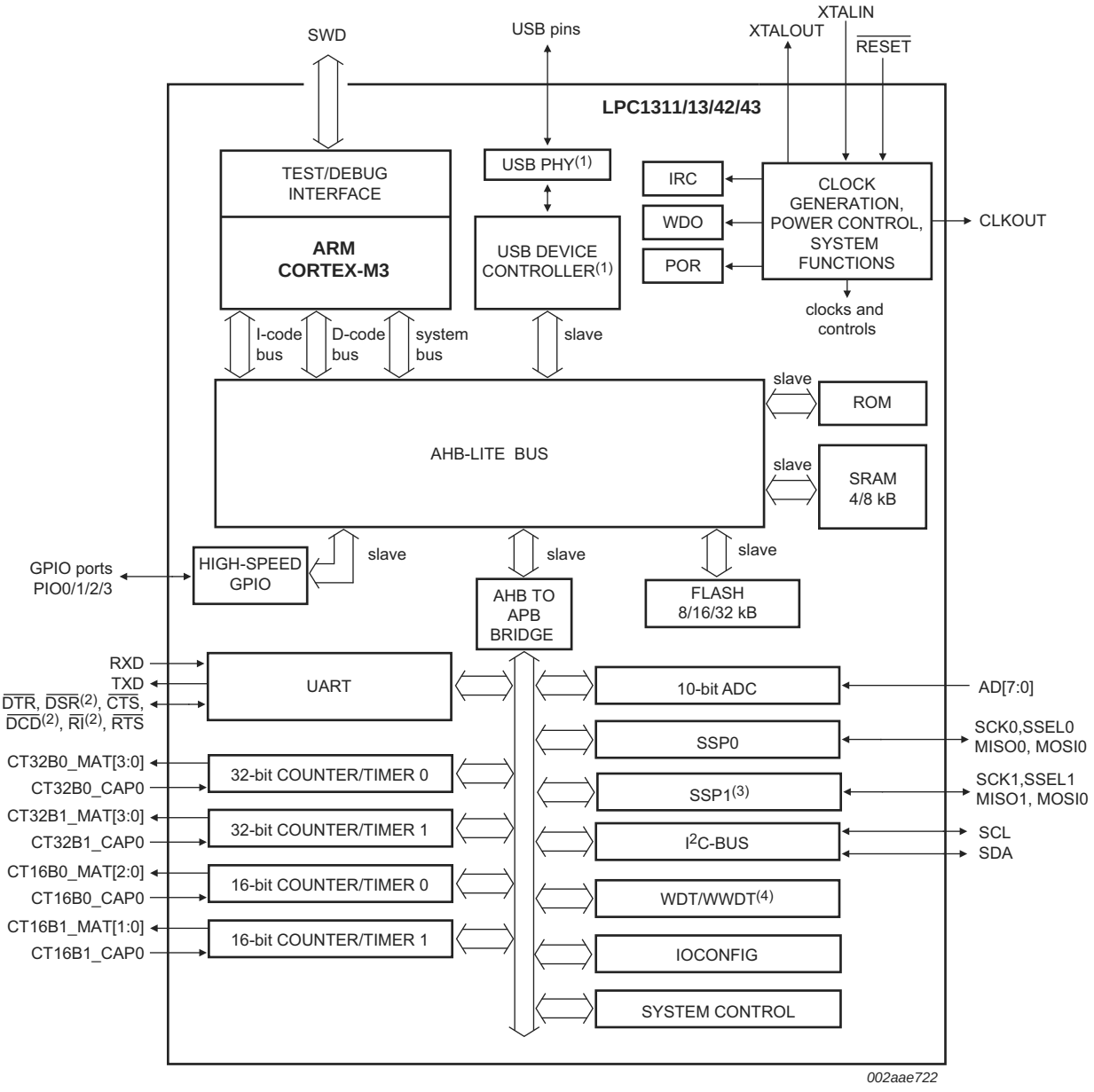
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	I²C, Microwire, SPI, SSI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	28
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VQFN Exposed Pad
Supplier Device Package	32-HVQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1311fhn33-01-55

Table 2. Ordering options for LPC1311/13/42/43 *…continued*

Type number	Flash	Total SRAM	USB	Power profiles	UART RS-485	I^2C/ Fast+	SSP	ADC channels	Pins	Package
LPC1342FHN33	16 kB	4 kB	Device	no	1	1	1	8	33	HVQFN33
LPC1342FBD48	16 kB	4 kB	Device	no	1	1	1	8	48	LQFP48
LPC1343FHN33	32 kB	8 kB	Device	no	1	1	1	8	33	HVQFN33
LPC1343FBD48	32 kB	8 kB	Device	no	1	1	1	8	48	LQFP48

5. Block diagram



(1) LPC1342/43 only.

(2) LQFP48 package only.

(3) On LPC1313FBD48/01 only.

(4) Windowed WatchDog Timer (WWDT) on LPC1311/01 and LPC1313/01 only.

Fig 1. Block diagram

6. Pinning information

6.1 Pinning

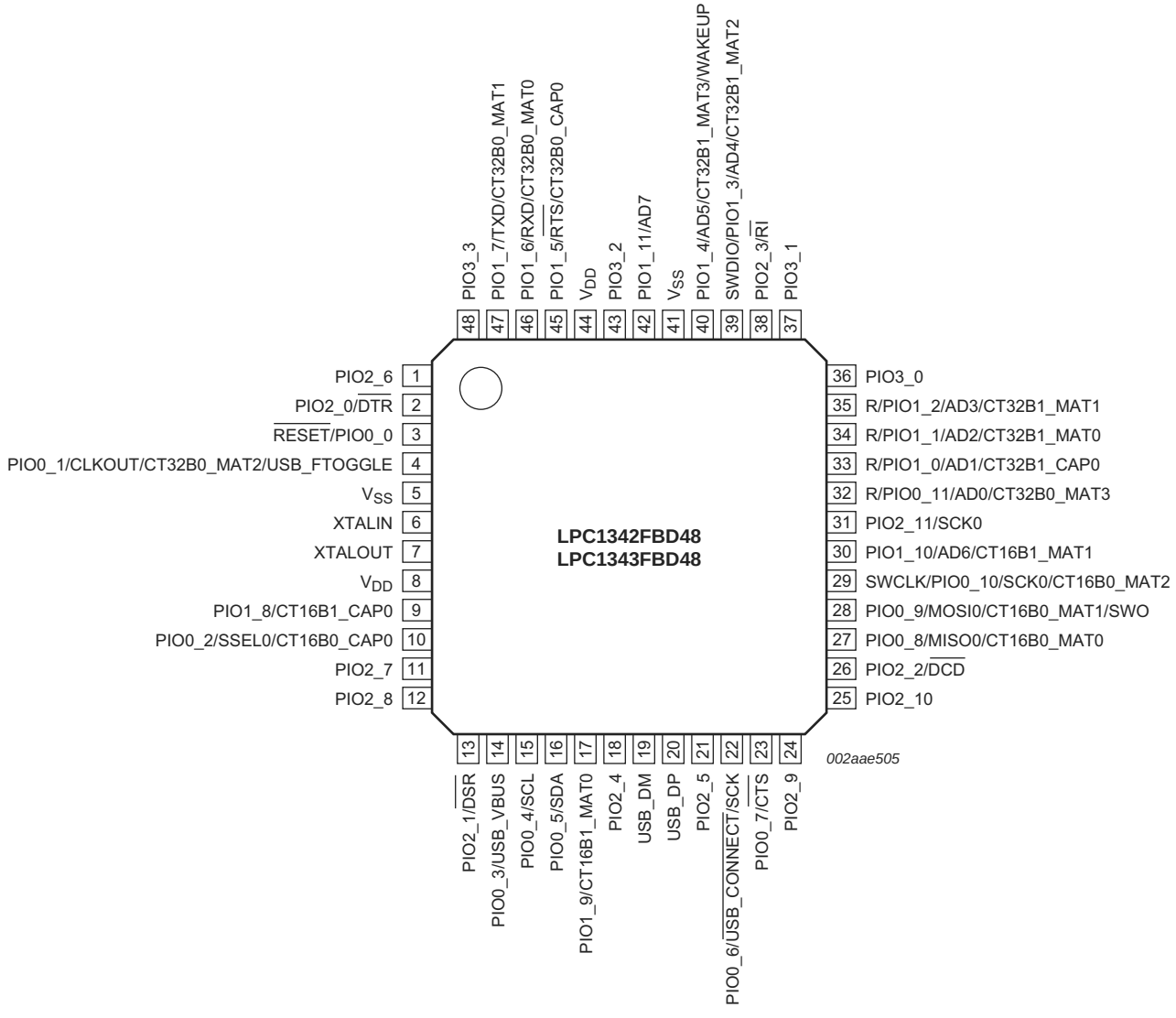
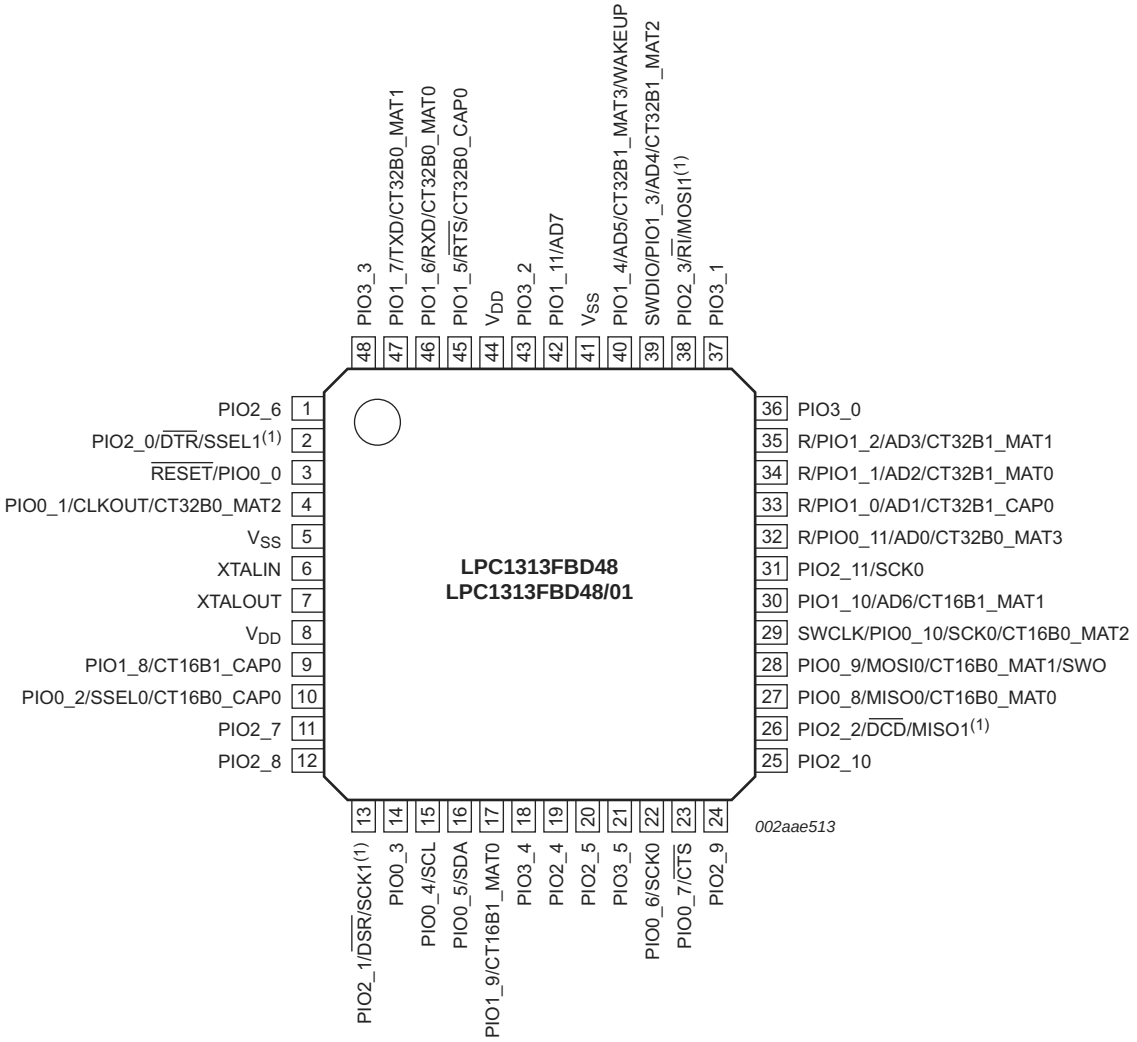


Fig 2. LPC1342/43 LQFP48 package



(1) SSP1 or UART function on LPC1313FBD48/01 only.

Fig 4. LPC1313 LQFP48 package

Table 4. LPC1311/13/42/43 HVQFN33 pin description table *…continued*

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
PIO1_7/TXD/ CT32B0_MAT1	32[3]	yes	I/O	I; PU	**PIO1_7 —** General purpose digital input/output pin.
			O	-	**TXD —** Transmitter output for UART.
			O	-	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
PIO1_8/ CT16B1_CAP0	7[3]	yes	I/O	I; PU	**PIO1_8 —** General purpose digital input/output pin.
			I	-	**CT16B1_CAP0 —** Capture input 0 for 16-bit timer 1.
PIO1_9/ CT16B1_MAT0	12[3]	yes	I/O	I; PU	**PIO1_9 —** General purpose digital input/output pin.
			O	-	**CT16B1_MAT0 —** Match output 0 for 16-bit timer 1.
PIO1_10/AD6/ CT16B1_MAT1	20[5]	yes	I/O	I; PU	**PIO1_10 —** General purpose digital input/output pin.
			I	-	**AD6 —** A/D converter, input 6.
			O	-	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
PIO1_11/AD7	27[5]	yes	I/O	I; PU	**PIO1_11 —** General purpose digital input/output pin.
			I	-	**AD7 —** A/D converter, input 7.
PIO2_0/$\overline{\text{DTR}}$	1[3]	yes	I/O	I; PU	**PIO2_0 —** General purpose digital input/output pin.
			O	-	**$\overline{\text{DTR}}$ —** Data Terminal Ready output for UART.
PIO3_2	28[3]	yes	I/O	I; PU	**PIO3_2 —** General purpose digital input/output pin.
PIO3_4	13[3]	no	I/O	I; PU	**PIO3_4 —** General purpose digital input/output pin (LPC1311/13 only).
PIO3_5	14[3]	no	I/O	I; PU	**PIO3_5 —** General purpose digital input/output pin (LPC1311/13 only).
USB_DM	13[6]	no	I/O	F	**USB_DM —** USB bidirectional D− line (LPC1342/43 only).
USB_DP	14[6]	no	I/O	F	**USB_DP —** USB bidirectional D+ line (LPC1342/43 only).
V_{DD}	6; 29	-	I	-	3.3 V supply voltage to the internal regulator, the external rail, and the ADC. Also used as the ADC reference voltage.
XTALIN	4[7]	-	I	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	5[7]	-	O	-	Output from the oscillator amplifier.
V_{SS}	33	-	-	-	Thermal pad. Connect to ground.

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled (for V_{DD} = 3.3 V, pin is pulled up to 2.6 V for parts LPC1311/13/42/43 and pulled up to 3.3 V for parts LPC1311/01 and LPC1313/01); IA = inactive, no pull-up/down enabled. F = floating; floating pins, if not used, should be tied to ground or power to minimize power consumption.

[2] 5 V tolerant pad. See Figure 37 for pad characteristics. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 36).

[4] I^2C-bus pads compliant with the I^2C-bus specification for I^2C standard mode and I^2C Fast-mode Plus.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled, and the pin is not 5 V tolerant (see Figure 36).

[6] Pad provides USB functions. It is designed in accordance with the USB specification, revision 2.0 (Full-speed and Low-speed mode only). This pad is not 5 V tolerant.

[7] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

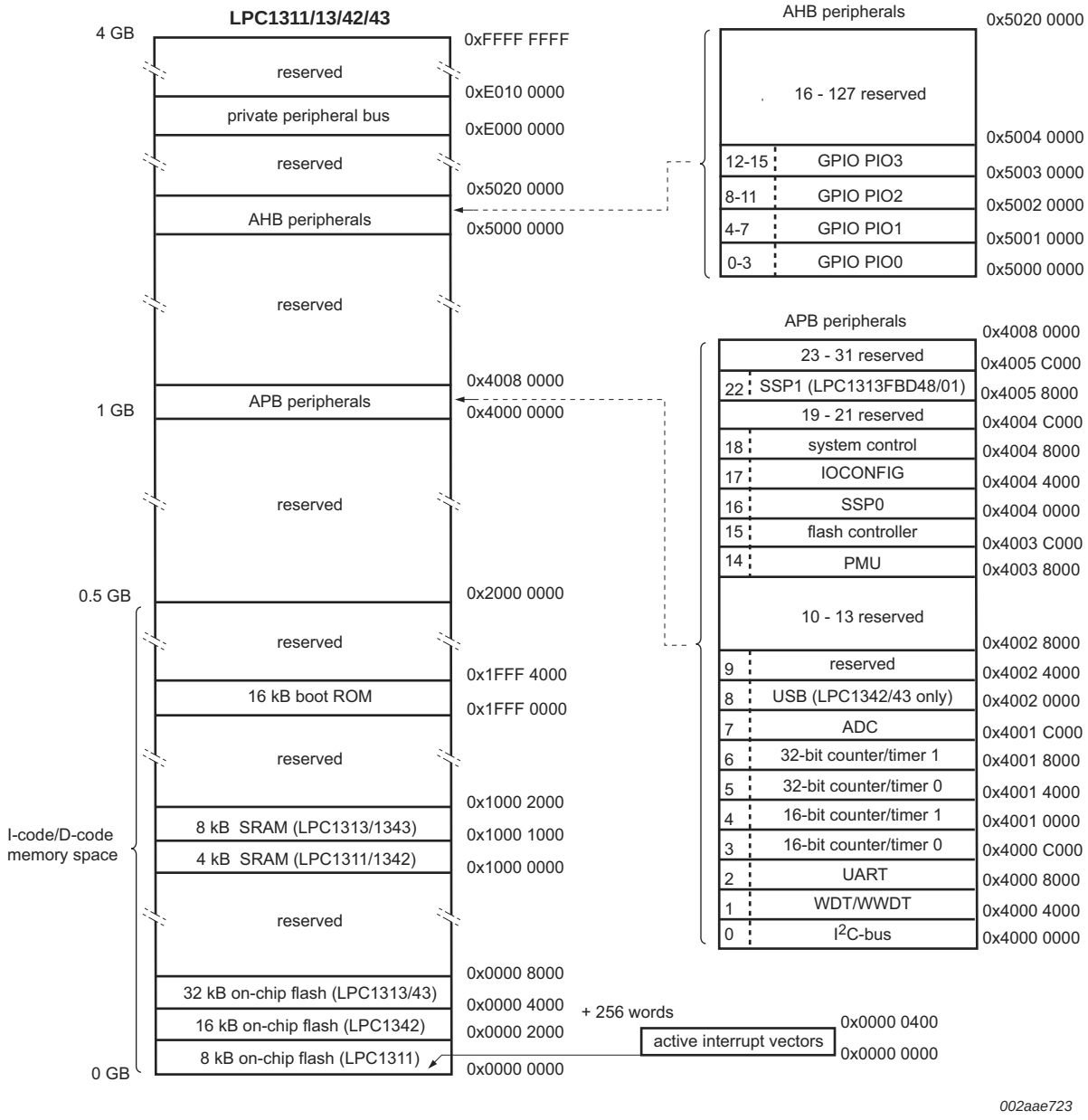
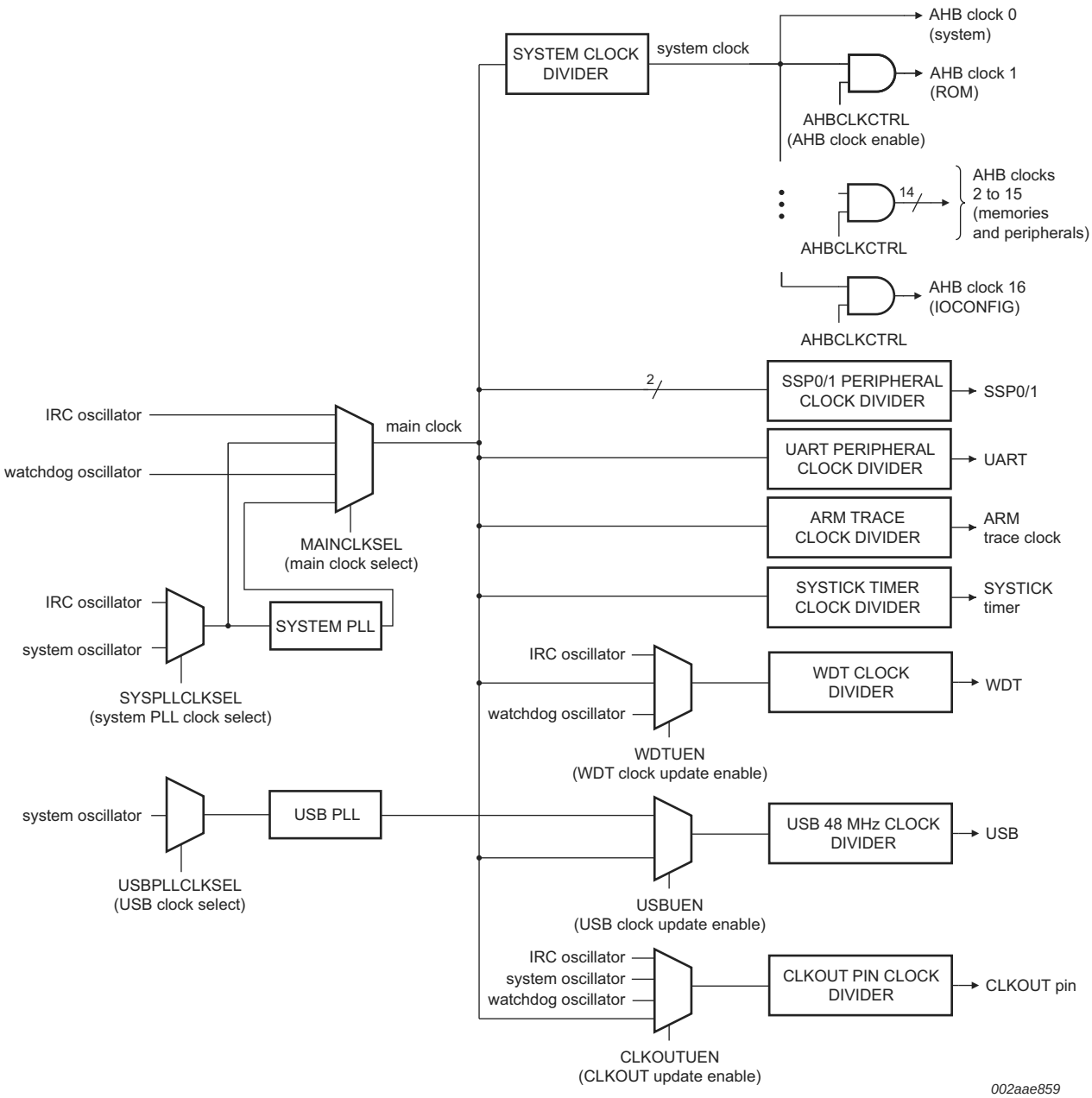


Fig 6. LPC1311/13/42/43 memory map

7.6 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is an integral part of the Cortex-M3. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.



The USB clock is available on LPC1342/43 only. SSP1 is available on LPC1313FBD48/01 only.

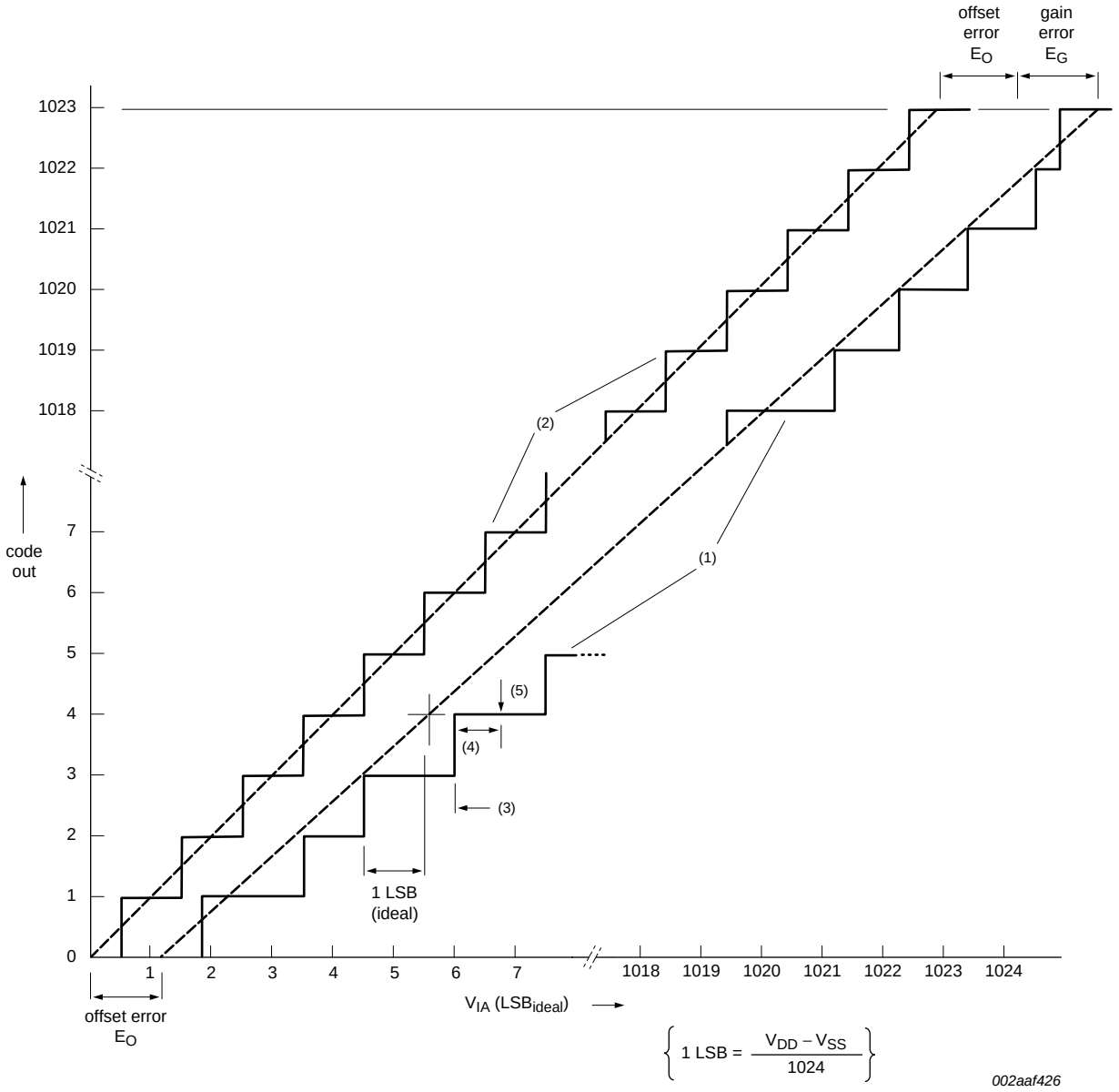
Fig 7. LPC1311/13/42/43 clocking generation block diagram

7.18.1.1 Internal RC oscillator

The IRC may be used as the clock source for the WDT, and/or as the clock that drives the system PLL and subsequently the CPU. The nominal IRC frequency is 12 MHz. The IRC is trimmed to 1 % accuracy over the entire voltage and temperature range.

Table 7. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	$2.5\ V \le V_{DD} \le 3.6\ V$; $I_{OH} = -4\ mA$		$V_{DD} - 0.4$	-	-	V
		$2.0\ V \le V_{DD} < 2.5\ V$; $I_{OH} = -3\ mA$		$V_{DD} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	$2.5\ V \le V_{DD} \le 3.6\ V$; $I_{OL} = 4\ mA$		-	-	0.4	V
		$2.0\ V \le V_{DD} < 2.5\ V$; $I_{OL} = 3\ mA$		-	-	0.4	V
I_{OH}	HIGH-level output current	$2.5\ V \le V_{DD} \le 3.6\ V$; $V_{OH} = V_{DD} - 0.4\ V$		−4	-	-	mA
		$2.0\ V \le V_{DD} < 2.5\ V$; $V_{OH} = V_{DD} - 0.4\ V$		−3	-	-	mA
I_{OL}	LOW-level output current	$2.5\ V \le V_{DD} \le 3.6\ V$; $V_{OL} = 0.4\ V$		4	-	-	mA
		$2.0\ V \le V_{DD} < 2.5\ V$; $V_{OL} = 0.4\ V$		3	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	$V_{OH} = 0\ V$	[15]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD}$	[15]	-	-	50	mA
I_{pd}	pull-down current	$V_I = 5\ V$		10	50	150	µA
I_{pu}	pull-up current	$V_I = 0\ V$		−15	−50	−85	µA
		$V_{DD} < V_I < 5\ V$		0	0	0	µA
High-drive output pin (PIO0_7); see Figure 19 and Figure 21							
I_{IL}	LOW-level input current	$V_I = 0\ V$; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled		-	0.5	10	nA
I_{OZ}	OFF-state output current	$V_O = 0\ V$; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled		-	0.5	10	nA
V_I	input voltage	pin configured to provide a digital function	[12][13] [14]	0	-	5.0	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	$2.5\ V \le V_{DD} \le 3.6\ V$; $I_{OH} = -20\ mA$		$V_{DD} - 0.4$	-	-	V
		$2.0\ V \le V_{DD} < 2.5\ V$; $I_{OH} = -12\ mA$		$V_{DD} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	$2.5\ V \le V_{DD} \le 3.6\ V$; $I_{OL} = 4\ mA$		-	-	0.4	V
		$2.0\ V \le V_{DD} < 2.5\ V$; $I_{OL} = 3\ mA$		-	-	0.4	V



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 8. ADC characteristics

9.1 BOD static characteristics for LPC1300 series

Remark: Applies to parts LPC1311/13/42/43 and all their packages.

Table 9. BOD static characteristics[1]
T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 0				
		assertion	-	1.69	-	V
		de-assertion	-	1.84	-	V
		interrupt level 1				
		assertion	-	2.29	-	V
		de-assertion	-	2.44	-	V
		interrupt level 2				
		assertion	-	2.59	-	V
		de-assertion	-	2.74	-	V
		interrupt level 3				
		assertion	-	2.87	-	V
		de-assertion	-	2.98	-	V
		reset level 0				
		assertion	-	1.49	-	V
		de-assertion	-	1.64	-	V

[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see *LPC13xx user manual*.

9.2 BOD static characteristics for LPC1300L series (LPC1311/01 and LPC1313/01)

Remark: Applies to parts LPC1311/01 and LPC1313/01 and all packages.

Table 10. BOD static characteristics[1]
T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 0				
		assertion	-	1.65	-	V
		de-assertion	-	1.80	-	V
		interrupt level 1				
		assertion	-	2.22	-	V
		de-assertion	-	2.35	-	V
		interrupt level 2				
		assertion	-	2.52	-	V
		de-assertion	-	2.66	-	V
		interrupt level 3				
		assertion	-	2.80	-	V
		de-assertion	-	2.90	-	V
		reset level 0				
		assertion	-	1.46	-	V
		de-assertion	-	1.63	-	V
		reset level 1				
		assertion	-	2.06	-	V
		de-assertion	-	2.15	-	V
		reset level 2				
		assertion	-	2.35	-	V
		de-assertion	-	2.43	-	V
		reset level 3				
		assertion	-	2.63	-	V
		de-assertion	-	2.71	-	V

[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see *LPC13xx user manual*.

9.3 Power consumption for LPC1300 series

Remark: Applies to parts LPC1311/13/42/43 and all their packages.

Power measurements in Active, Sleep, and Deep-sleep modes were performed under the following conditions (see *LPC13xx user manual*):

- Configure all pins as GPIO with pull-up resistor disabled in the IOCONFIG block.
- Configure GPIO pins as outputs using the GPIOnDIR registers.
- Write 0 to all GPIOnDATA registers to drive the outputs LOW.

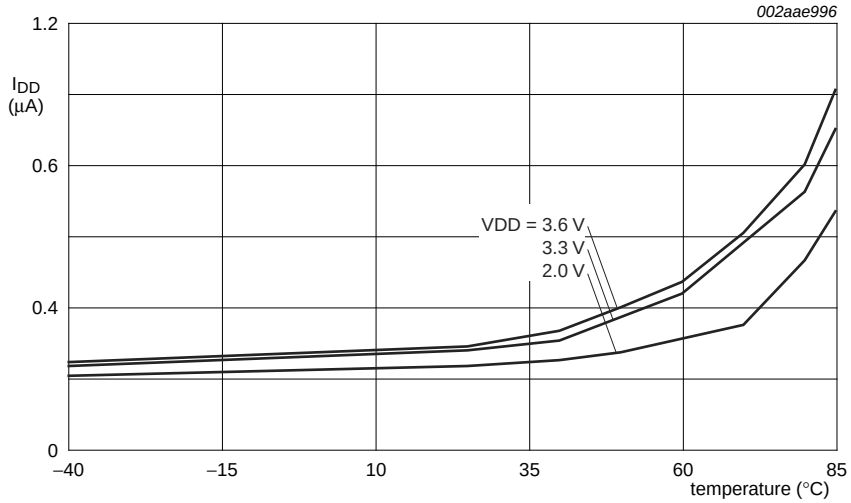


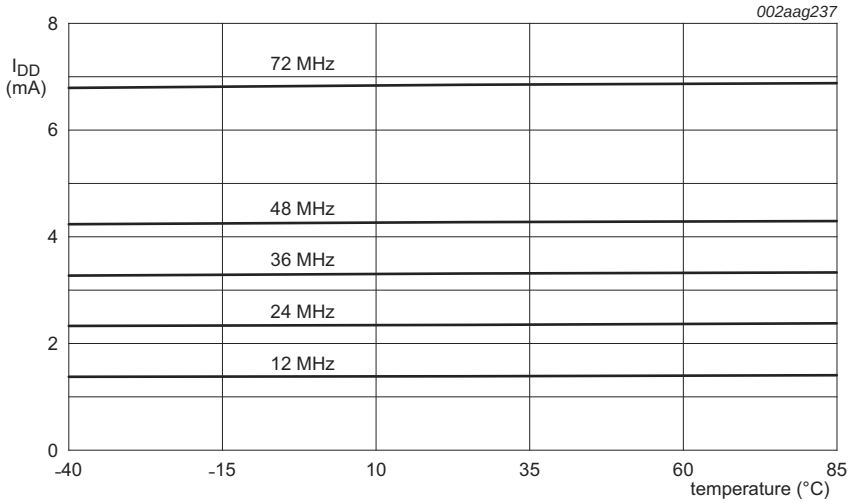
Fig 13. Typical supply current versus temperature in Deep power-down mode (LPC1311/13/42/43)

9.4 Power consumption for LPC1300L series (LPC1311/01 and LPC1313/01)

Remark: Applies to parts LPC1311/01 and LPC1313/01 and all their packages.

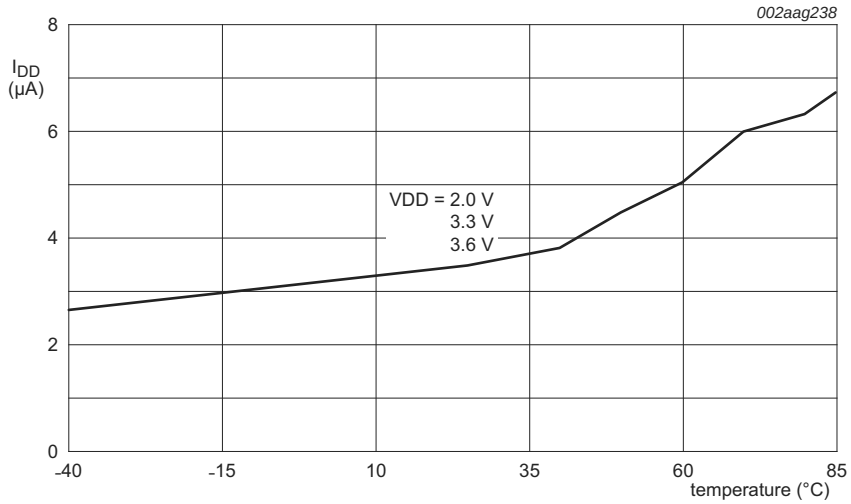
Power measurements in Active, Sleep, and Deep-sleep modes were performed under the following conditions (see *LPC13xx user manual*):

- Configure all pins as GPIO with pull-up resistor disabled in the IOCONFIG block.
- Configure GPIO pins as outputs using the GPIOnDIR registers.
- Write 0 to all GPIOnDATA registers to drive the outputs LOW.



Conditions: V_{DD} = 3.3 V; Sleep mode entered from flash; internal pull-up resistors disabled; system oscillator and system PLL enabled; IRC, BOD disabled; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; low-current mode.

Fig 16. Typical supply current versus temperature in Sleep mode (LPC1311/01 and LPC1313/01)



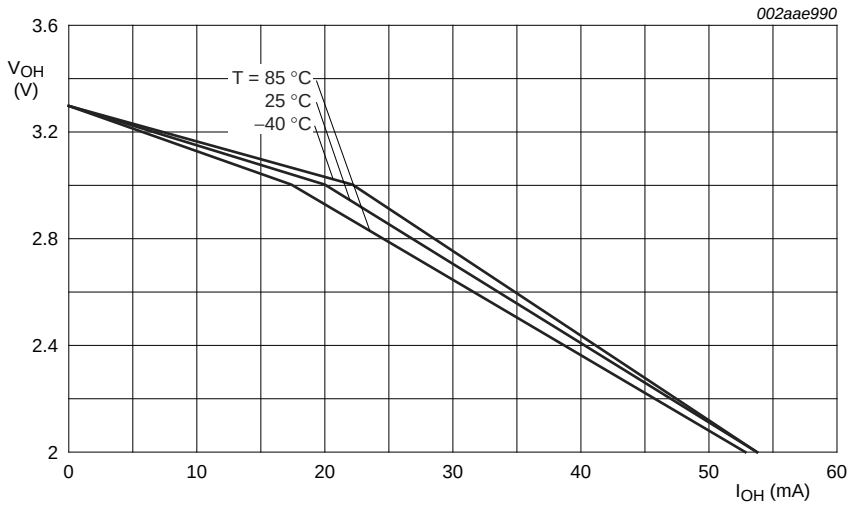
Conditions: BOD disabled; all oscillators and analog blocks turned off in the PDSLEEPCFG register; PDSLEEPCFG = 0x0000 0FFF.

Fig 17. Typical supply current versus temperature in Deep-sleep mode (analog blocks disabled, LPC1311/01 and LPC1313/01)

Table 11. Power consumption for individual analog and digital blocks *…continued*

Peripheral	Typical supply current in mA				Notes
	n/a	12 MHz	48 MHz	72 MHz	
GPIO	-	0.21	0.80	1.17	GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register.
IOCONFIG	-	0.00	0.02	0.02	-
I2C	-	0.03	0.12	0.17	-
ROM	-	0.04	0.15	0.22	-
SSP0	-	0.11	0.41	0.60	-
SSP1	-	0.11	0.41	0.60	On LPC1313FBD48/01 only.
UART	-	0.20	0.76	1.11	-
WDT	-	0.01	0.05	0.08	Main clock selected as clock source for the WDT.
USB	-	-	3.91	-	Main clock selected as clock source for the USB. USB_DP and USB_DM pulled LOW externally.
USB	-	1.84	4.19	5.71	Dedicated USB PLL selected as clock source for the USB. USB_DP and USB_DM pulled LOW externally.

9.6 Electrical pin characteristics



Conditions: V_{DD} = 3.3 V; on pin PIO0_7.

Fig 19. High-drive output: Typical HIGH-level output voltage V_{OH} versus HIGH-level output current I_{OH}.

10.3 External clock

Table 14. Dynamic characteristic: external clock
T_{amb} = –40 °C to +85 °C; V_{DD} over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
f_{osc}	oscillator frequency		1	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

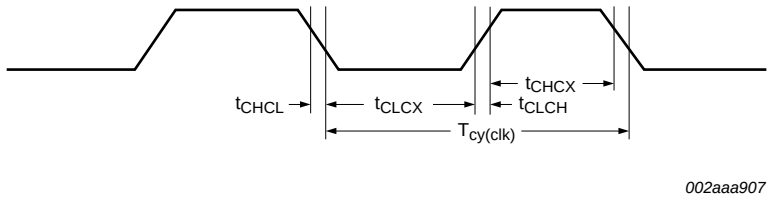


Fig 26. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

10.4 Internal oscillators

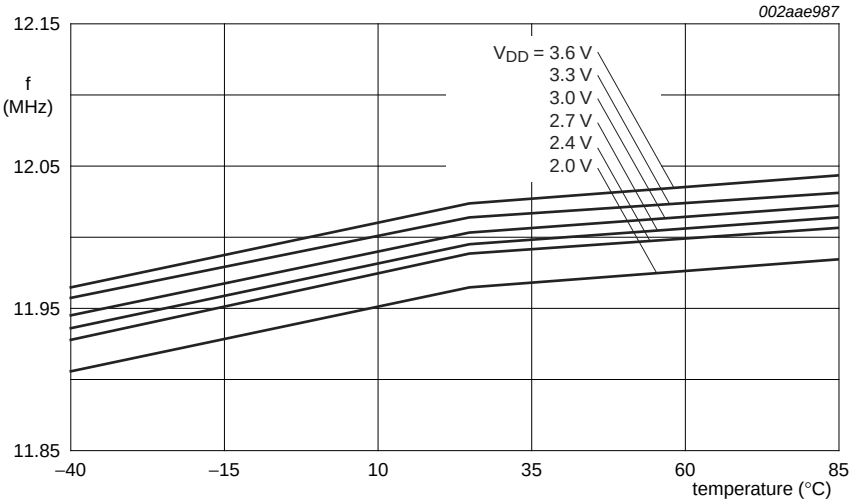
Table 15. Dynamic characteristics: IRC

T_{amb} = –40 °C to +85 °C; 2.7 V ≤ V_{DD} ≤ 3.6 V[1].

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	-	11.88	12	12.12	MHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.



Conditions: Frequency values are typical values. 12 MHz ± 1 % accuracy is guaranteed for 2.7 V ≤ V_{DD} ≤ 3.6 V and T_{amb} = –40 °C to +85 °C. Variations between parts may cause the IRC to fall outside the 12 MHz ± 1 % accuracy specification for voltages below 2.7 V.

Fig 27. Internal RC oscillator frequency f versus temperature

Table 16. Dynamic characteristics: Watchdog oscillator

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$f_{osc(int)}$	internal oscillator frequency	DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register;	[2][3]	-	7.8	-	kHz
		DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register	[2][3]	-	1700	-	kHz

[1] Typical ratings are not guaranteed. The values listed are at nominal supply voltages.

[2] The typical frequency spread over processing and temperature (T_{amb} = –40 °C to +85 °C) is ±40 %.

[3] See the *LPC13xx user manual.*

11.7 ElectroMagnetic Compatibility (EMC)

Radiated emission measurements according to the IEC61967-2 standard using the TEM-cell method are shown for the LPC1343FBD48 in Table 23.

Table 23. ElectroMagnetic Compatibility (EMC) for part LPC1343FBD48 (TEM-cell method)
V_{DD} = 3.3 V; T_{amb} = 25 °C.

Parameter	Frequency band	System clock =				Unit
		12 MHz	24 MHz	48 MHz	72 MHz	
Input clock: IRC (12 MHz)						
maximum peak level	150 kHz - 30 MHz	–6	–5	–7	–7	dBµV
	30 MHz - 150 MHz	–1	+3	+9	+13	dBµV
	150 MHz - 1 GHz	+3	+7	+15	+19	dBµV
IEC level[1]	-	O	N	M	L	-
Input clock: crystal oscillator (12 MHz)						
maximum peak level	150 kHz - 30 MHz	-5	–5	–7	–7	dBµV
	30 MHz - 150 MHz	0	+4	+9	+13	dBµV
	150 MHz - 1 GHz	3	+8	+15	+20	dBµV
IEC level[1]	-	O	N	M	L	-

[1] IEC levels refer to Appendix D in the IEC61967-2 Specification.

14. Abbreviations

Table 24. Abbreviations

Acronym	Description
A/D	Analog-to-Digital
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
EOP	End Of Packet
ETM	Embedded Trace Macrocell
FIFO	First-In, First-Out
GPIO	General Purpose Input/Output
HID	Human Interface Device
I/O	Input/Output
LSB	Least Significant Bit
MSC	Mass Storage Class
PHY	Physical Layer
PLL	Phase-Locked Loop
SE0	Single Ended Zero
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
SSP	Synchronous Serial Port
SoF	Start-of-Frame
TCM	Tightly-Coupled Memory
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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