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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	I ² C, Microwire, SPI, SSI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	28
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VQFN Exposed Pad
Supplier Device Package	32-HVQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1311fhn33-551

6. Pinning information

6.1 Pinning

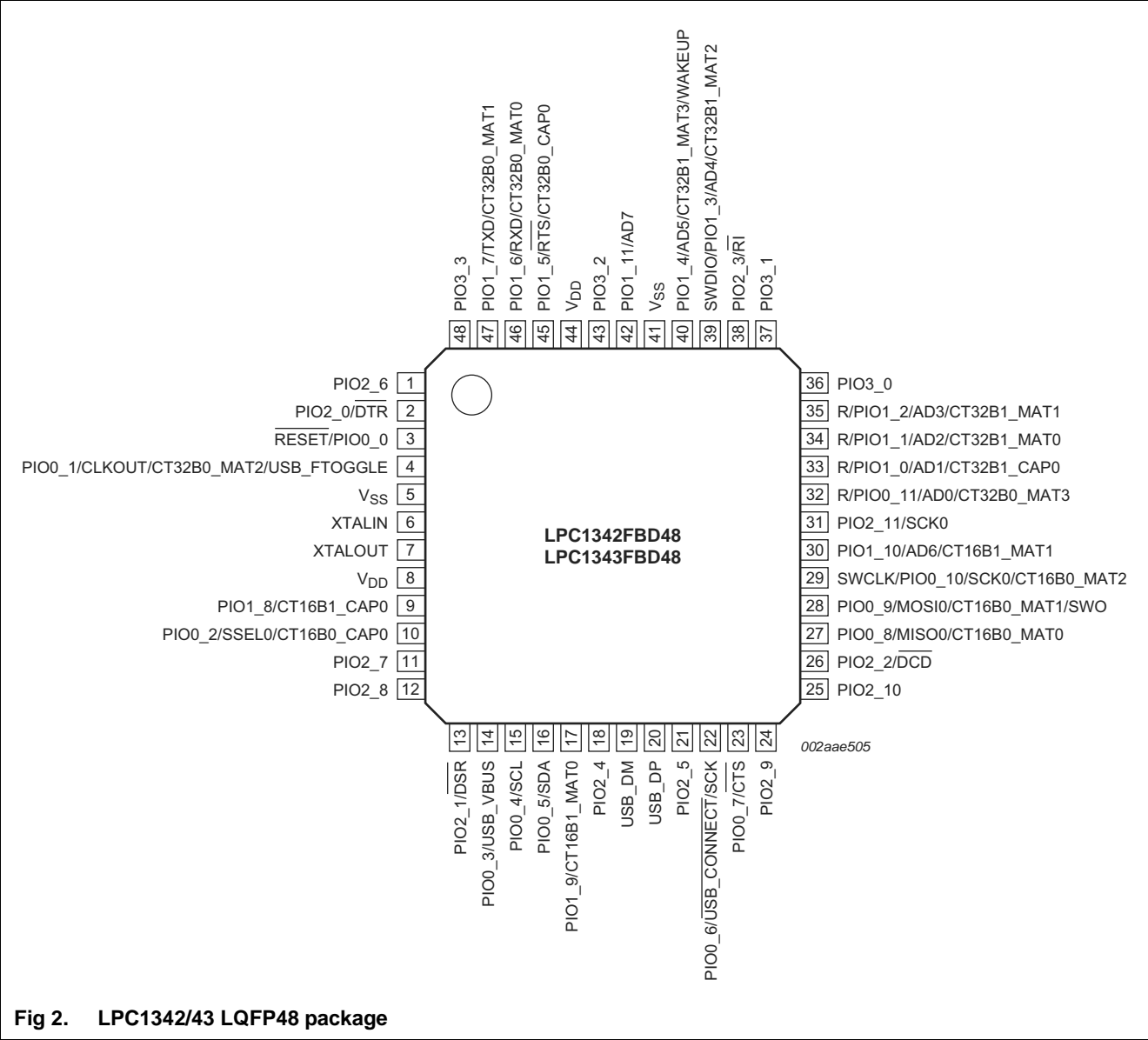


Fig 2. LPC1342/43 LQFP48 package

6.2 Pin description

Table 3. LPC1313/42/43 LQFP48 pin description table

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
RESET/PIO0_0	3 ^[2]	yes	I	I; PU	RESET — External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0.
			I/O	-	PIO0_0 — General purpose digital input/output pin with 10 ns glitch filter.
PIO0_1/CLKOUT/ CT32B0_MAT2/ USB_FTOGGLE	4 ^[3]	yes	I/O	I; PU	PIO0_1 — General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler or the USB device enumeration (USB on LPC1342/43 only, see description of PIO0_3).
			O	-	CLKOUT — Clockout pin.
			O	-	CT32B0_MAT2 — Match output 2 for 32-bit timer 0.
			O	-	USB_FTOGGLE — USB 1 ms Start-of-Frame signal (LPC1342/43 only).
PIO0_2/SSEL0/ CT16B0_CAP0	10 ^[3]	yes	I/O	I; PU	PIO0_2 — General purpose digital input/output pin.
			I/O	-	SSEL0 — Slave select for SSP0.
			I	-	CT16B0_CAP0 — Capture input 0 for 16-bit timer 0.
PIO0_3/USB_VBUS	14 ^[3]	yes	I/O	I; PU	PIO0_3 — General purpose digital input/output pin. LPC1342/43 only: A LOW level on this pin during reset starts the ISP command handler, a HIGH level starts the USB device enumeration.
			I	-	USB_VBUS — Monitors the presence of USB bus power (LPC1342/43 only).
PIO0_4/SCL	15 ^[4]	yes	I/O	I; IA	PIO0_4 — General purpose digital input/output pin (open-drain).
			I/O	-	SCL — I ² C-bus clock input/output (open-drain). High-current sink only if I ² C Fast-mode Plus is selected in the I/O configuration register.
PIO0_5/SDA	16 ^[4]	yes	I/O	I; IA	PIO0_5 — General purpose digital input/output pin (open-drain).
			I/O	-	SDA — I ² C-bus data input/output (open-drain). High-current sink only if I ² C Fast-mode Plus is selected in the I/O configuration register.
PIO0_6/ USB_CONNECT/ SCK0	22 ^[3]	yes	I/O	I; PU	PIO0_6 — General purpose digital input/output pin.
			O	-	USB_CONNECT — Signal used to switch an external 1.5 kΩ resistor under software control. Used with the SoftConnect USB feature (LPC1342/43 only).
			I/O	-	SCK0 — Serial clock for SSP0.
PIO0_7/CTS	23 ^[3]	yes	I/O	I; PU	PIO0_7 — General purpose digital input/output pin (high-current output driver).
			I	-	CTS — Clear To Send input for UART.
PIO0_8/MISO0/ CT16B0_MAT0	27 ^[3]	yes	I/O	I; PU	PIO0_8 — General purpose digital input/output pin.
			I/O	-	MISO0 — Master In Slave Out for SSP0.
			O	-	CT16B0_MAT0 — Match output 0 for 16-bit timer 0.

Table 3. LPC1313/42/43 LQFP48 pin description table ...continued

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
PIO0_9/MOSI0/ CT16B0_MAT1/ SWO	28 ^[3]	yes	I/O	I; PU	PIO0_9 — General purpose digital input/output pin.
			I/O	-	MOSI0 — Master Out Slave In for SSP0.
			O	-	CT16B0_MAT1 — Match output 1 for 16-bit timer 0.
			O	-	SWO — Serial wire trace output.
SWCLK/PIO0_10/ SCK0/CT16B0_MAT2	29 ^[3]	yes	I	I; PU	SWCLK — Serial wire clock.
			I/O	-	PIO0_10 — General purpose digital input/output pin.
			I/O	-	SCK0 — Serial clock for SSP0.
			O	-	CT16B0_MAT2 — Match output 2 for 16-bit timer 0.
R/PIO0_11/ AD0/CT32B0_MAT3	32 ^[5]	yes	-	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO0_11 — General purpose digital input/output pin.
			I	-	AD0 — A/D converter, input 0.
			O	-	CT32B0_MAT3 — Match output 3 for 32-bit timer 0.
R/PIO1_0/ AD1/CT32B1_CAP0	33 ^[5]	yes	-	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO1_0 — General purpose digital input/output pin.
			I	-	AD1 — A/D converter, input 1.
			I	-	CT32B1_CAP0 — Capture input 0 for 32-bit timer 1.
R/PIO1_1/ AD2/CT32B1_MAT0	34 ^[5]	yes	-	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO1_1 — General purpose digital input/output pin.
			I	-	AD2 — A/D converter, input 2.
			O	-	CT32B1_MAT0 — Match output 0 for 32-bit timer 1.
R/PIO1_2/ AD3/CT32B1_MAT1	35 ^[5]	yes	-	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO1_2 — General purpose digital input/output pin.
			I	-	AD3 — A/D converter, input 3.
			O	-	CT32B1_MAT1 — Match output 1 for 32-bit timer 1.
SWDIO/PIO1_3/ AD4/ CT32B1_MAT2	39 ^[5]	yes	I/O	I; PU	SWDIO — Serial wire debug input/output.
			I/O	-	PIO1_3 — General purpose digital input/output pin.
			I	-	AD4 — A/D converter, input 4.
			O	-	CT32B1_MAT2 — Match output 2 for 32-bit timer 1.
PIO1_4/AD5/ CT32B1_MAT3/ WAKEUP	40 ^[5]	yes	I/O	I; PU	PIO1_4 — General purpose digital input/output pin.
			I	-	AD5 — A/D converter, input 5.
			O	-	CT32B1_MAT3 — Match output 3 for 32-bit timer 1.
			I	-	WAKEUP — Deep power-down mode wake-up pin with 20 ns glitch filter. This pin must be pulled HIGH externally to enter Deep power-down mode and pulled LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.

Table 4. LPC1311/13/42/43 HVQFN33 pin description table

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
RESET/PIO0_0	2 ^[2]	yes	I	I; PU	RESET — External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0.
			I/O	-	PIO0_0 — General purpose digital input/output pin with 10 ns glitch filter.
PIO0_1/CLKOUT/CT32B0_MAT2/USB_FTOGGLE	3 ^[3]	yes	I/O	I; PU	PIO0_1 — General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler or the USB device enumeration (USB on LPC1342/43 only, see description of PIO0_3).
			O	-	CLKOUT — Clock out pin.
			O	-	CT32B0_MAT2 — Match output 2 for 32-bit timer 0.
			O	-	USB_FTOGGLE — USB 1 ms Start-of-Frame signal (LPC1342/43 only).
PIO0_2/SSEL0/CT16B0_CAP0	8 ^[3]	yes	I/O	I; PU	PIO0_2 — General purpose digital input/output pin.
			I/O	-	SSEL0 — Slave select for SSP0.
			I	-	CT16B0_CAP0 — Capture input 0 for 16-bit timer 0.
PIO0_3/USB_VBUS	9 ^[3]	yes	I/O	I; PU	PIO0_3 — General purpose digital input/output pin. LPC1342/43 only: A LOW level on this pin during reset starts the ISP command handler, a HIGH level starts the USB device enumeration.
			I	-	USB_VBUS — Monitors the presence of USB bus power (LPC1342/43 only).
PIO0_4/SCL	10 ^[4]	yes	I/O	I; IA	PIO0_4 — General purpose digital input/output pin (open-drain).
			I/O	-	SCL — I ² C-bus clock input/output (open-drain). High-current sink only if I ² C Fast-mode Plus is selected in the I/O configuration register.
PIO0_5/SDA	11 ^[4]	yes	I/O	I; IA	PIO0_5 — General purpose digital input/output pin (open-drain).
			I/O	-	SDA — I ² C-bus data input/output (open-drain). High-current sink only if I ² C Fast-mode Plus is selected in the I/O configuration register.
PIO0_6/USB_CONNECT/SCK0	15 ^[3]	yes	I/O	I; PU	PIO0_6 — General purpose digital input/output pin.
			O	-	USB_CONNECT — Signal used to switch an external 1.5 kΩ resistor under software control. Used with the SoftConnect USB feature (LPC1342/43 only).
			I/O	-	SCK0 — Serial clock for SSP0.
PIO0_7/CTS	16 ^[3]	yes	I/O	I; PU	PIO0_7 — General purpose digital input/output pin (high-current output driver).
			I	-	CTS — Clear To Send input for UART.
PIO0_8/MISO0/CT16B0_MAT0	17 ^[3]	yes	I/O	I; PU	PIO0_8 — General purpose digital input/output pin.
			I/O	-	MISO0 — Master In Slave Out for SSP0.
			O	-	CT16B0_MAT0 — Match output 0 for 16-bit timer 0.
PIO0_9/MOSI0/CT16B0_MAT1/SWO	18 ^[3]	yes	I/O	I; PU	PIO0_9 — General purpose digital input/output pin.
			I/O	-	MOSI0 — Master Out Slave In for SSP0.
			O	-	CT16B0_MAT1 — Match output 1 for 16-bit timer 0.
			O	-	SWO — Serial wire trace output.

7. Functional description

7.1 Architectural overview

The ARM Cortex-M3 includes three AHB-Lite buses: the system bus, the I-code bus, and the D-code bus (see [Figure 1](#)). The I-code and D-code core buses are faster than the system bus and are used similarly to TCM interfaces: one bus dedicated for instruction fetch (I-code) and one bus for data access (D-code). The use of two core buses allows for simultaneous operations if concurrent operations target different devices.

7.2 ARM Cortex-M3 processor

The ARM Cortex-M3 is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption. The ARM Cortex-M3 offers many new features, including a Thumb-2 instruction set, low interrupt latency, hardware multiply and divide, interruptible/continuable multiple load and store instructions, automatic state save and restore for interrupts, tightly integrated interrupt controller, and multiple core buses capable of simultaneous accesses.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM Cortex-M3 processor is described in detail in the *Cortex-M3 Technical Reference Manual* which is available on the official ARM website.

7.3 On-chip flash program memory

The LPC1311/13/42/43 contain 32 kB (LPC1313 and LPC1343), 16 kB (LPC1342), or 8 kB (LPC1311) of on-chip flash memory.

7.4 On-chip SRAM

The LPC1311/13/42/43 contain a total of 8 kB (LPC1343 and LPC1313) or 4 kB (LPC1342 and LPC1311) on-chip static RAM memory.

7.5 Memory map

The LPC1311/13/42/43 incorporate several distinct memory regions. [Figure 6](#) shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB peripheral area is 2 MB in size and is divided to allow for up to 128 peripherals. The APB peripheral area is 512 kB in size and is divided to allow for up to 32 peripherals. Each peripheral of either type is allocated 16 kB of space. This allows simplifying the address decoding for each peripheral.

The I²C-bus is bidirectional for inter-IC control using only two wires: a Serial Clock Line (SCL) and a Serial Data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I²C is a multi-master bus and can be controlled by more than one bus master connected to it.

7.12.1 Features

- The I²C-bus interface is a standard I²C-bus compliant interface with true open-drain pins. The I²C-bus interface also supports Fast-mode Plus with bit rates up to 1 Mbit/s.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I²C-bus can be used for test and diagnostic purposes.
- The I²C-bus controller supports multiple address recognition and a bus monitor mode.

7.13 10-bit ADC

The LPC1311/13/42/43 contains one ADC. It is a single 10-bit successive approximation ADC with eight channels.

7.13.1 Features

- 10-bit successive approximation ADC.
- Input multiplexing among 8 pins.
- Power-down mode.
- Measurement range 0 V to V_{DD}.
- 10-bit conversion time $\geq 2.44 \mu\text{s}$ (up to 400 kSamples/s).
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition of input pin or timer match signal.
- Individual result registers for each ADC channel to reduce interrupt overhead.

The vector table may be located anywhere within the bottom 1 GB of Cortex-M3 address space. The vector table must be located on a 256 word boundary.

7.20 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M3. Serial wire debug is supported.

9. Static characteristics

Table 7. Static characteristics

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
V_{DD}	supply voltage (core and external rail)		^[2] 2.0	3.3	3.6	V
LPC1300 series (LPC1311/13/42/43) power consumption						
I_{DD}	supply current	Active mode; $V_{DD} = 3.3\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; code while(1){} executed from flash;				
		system clock = 12 MHz	^{[3][4][5]} - ^{[6][7]}	4	-	mA
		system clock = 72 MHz	^{[4][5][6]} - ^{[8][7]}	17	-	mA
		Sleep mode; $V_{DD} = 3.3\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; system clock = 12 MHz	^{[3][4][5]} - ^{[6][7]}	2	-	mA
		Deep-sleep mode; $V_{DD} = 3.3\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$	^{[4][9][7]} -	30	-	μA
		Deep power-down mode; $V_{DD} = 3.3\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$	^[10] -	220	-	nA
LPC1300L series (LPC1311/01, LPC1313/01) power consumption in low-current mode^[11]						
I_{DD}	supply current	Active mode; $V_{DD} = 3.3\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; code while(1){} executed from flash;				
		system clock = 12 MHz	^{[3][4][5]} - ^{[6][7]}	2	-	mA
		system clock = 72 MHz	^{[4][5][6]} - ^{[8][7]}	13	-	mA
		Sleep mode; $V_{DD} = 3.3\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; system clock = 12 MHz	^{[3][4][5]} - ^{[6][7]}	1	-	mA
		Deep-sleep mode; $V_{DD} = 3.3\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$	^{[4][9][7]} -	2	-	μA
		Deep power-down mode; $V_{DD} = 3.3\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$	^[10] -	220	-	nA
Standard port pins and RESET pin; see Figure 21, Figure 22, Figure 23, Figure 24						
I_{IL}	LOW-level input current	$V_I = 0\text{ V}$; on-chip pull-up resistor disabled	-	0.5	10	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled	-	0.5	10	nA
I_{OZ}	OFF-state output current	$V_O = 0\text{ V}$; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled	-	0.5	10	nA
V_I	input voltage	pin configured to provide a digital function	^{[12][13]} 0 ^[14]	-	5.0	V

Table 7. Static characteristics ...continued
 $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, unless otherwise specified.

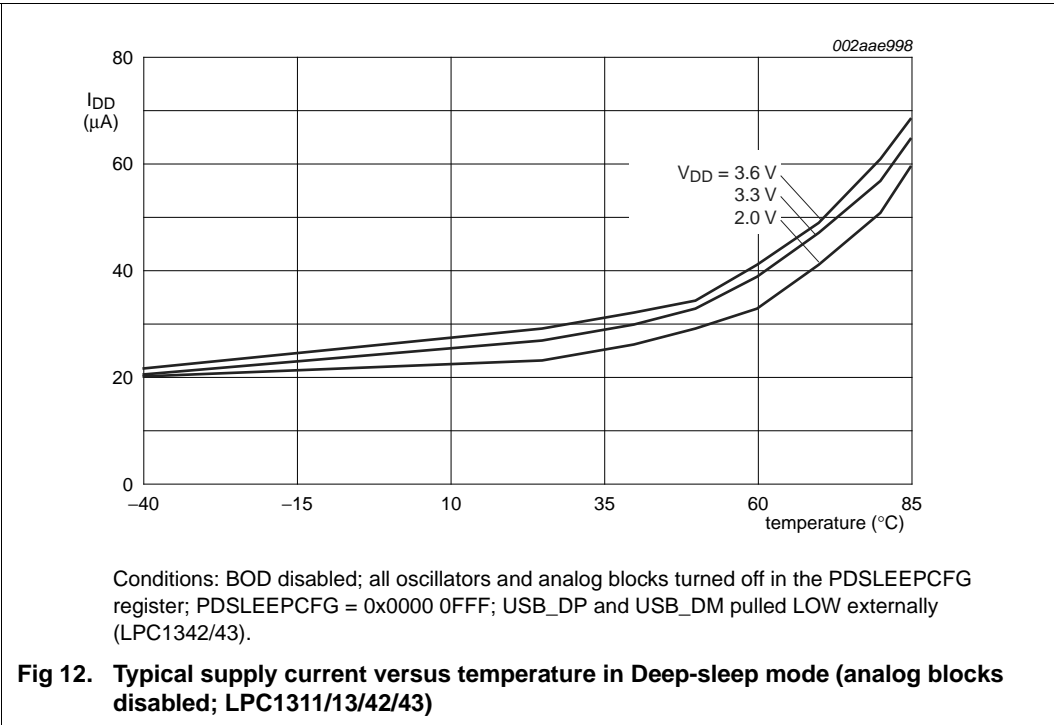
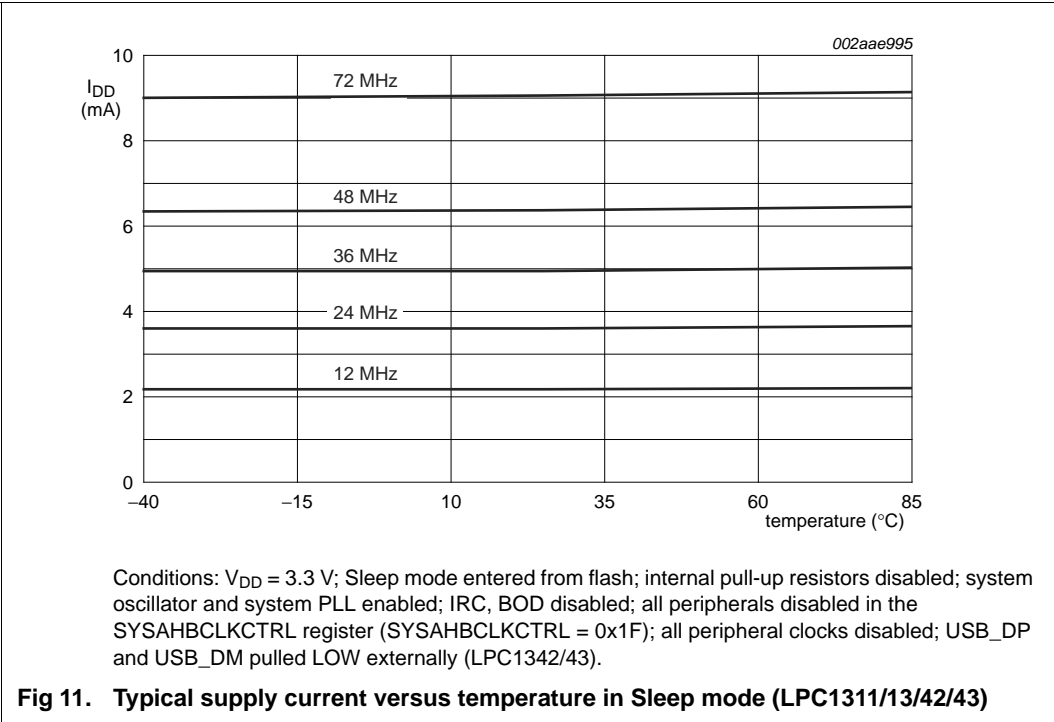
Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
V_{OH}	HIGH-level output voltage	driven; for low-/full-speed; R_L of 15 k Ω to GND	^[17] 2.8	-	3.5	V
C_{trans}	transceiver capacitance	pin to GND	^[17] -	-	20	pF
Z_{DRV}	driver output impedance for driver which is not high-speed capable	with 33 Ω series resistor; steady state drive	^{[18][17]} 36	-	44.1	Ω

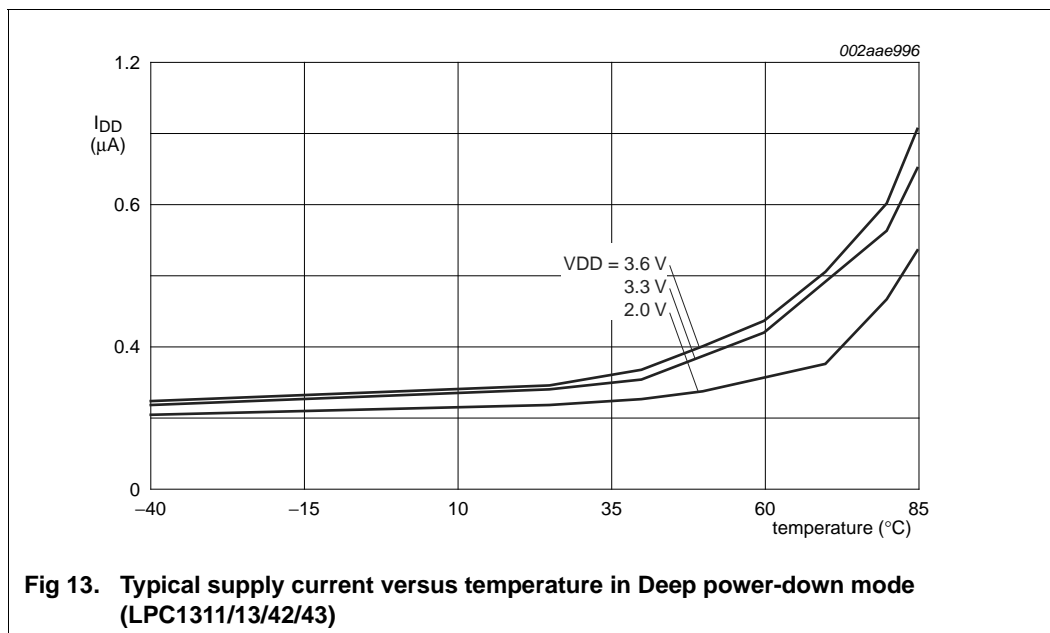
- [1] Typical ratings are not guaranteed. The values listed are at room temperature (25 $^{\circ}\text{C}$), nominal supply voltages.
- [2] For LPC1342 and LPC1343 only: For USB operation $3.0\text{ V} \leq V_{DD} \leq 3.6\text{ V}$. Guaranteed by design.
- [3] IRC enabled; system oscillator disabled; system PLL disabled.
- [4] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.
- [5] BOD disabled.
- [6] All peripherals disabled in the SYSAHBCLKCTRL register. Peripheral clocks to UART, SSP, trace clock, and SysTick timer disabled in the syscon block.
- [7] For LPC1342/43: USB_DP and USB_DM pulled LOW externally.
- [8] IRC disabled; system oscillator enabled; system PLL enabled.
- [9] All oscillators and analog blocks turned off in the PDSLEEPCFG register; PDSLEEPCFG = 0x0000 0FFF.
- [10] WAKEUP pin pulled HIGH externally. An external pull-up resistor is required on the $\overline{\text{RESET}}$ pin for the Deep power-down mode.
- [11] Low-current mode PWR_LOW_CURRENT selected when running the set_power routine in the power profiles.
- [12] Including voltage on outputs in 3-state mode.
- [13] V_{DD} supply voltage must be present.
- [14] 3-state outputs go into 3-state mode in Deep power-down mode.
- [15] Allowed as long as the current limit does not exceed the maximum current allowed by the device.
- [16] To V_{SS} .
- [17] $3.0\text{ V} \leq V_{DD} \leq 3.6\text{ V}$.
- [18] Includes external resistors of 33 $\Omega \pm 1\%$ on USB_DP and USB_DM.

Table 8. ADC static characteristics
 $T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ unless otherwise specified; ADC frequency 4.5 MHz, $V_{DD} = 2.5\text{ V}$ to 3.6 V .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IA}	analog input voltage		0	-	V_{DD}	V
C_{ia}	analog input capacitance		-	-	1	pF
E_D	differential linearity error	^{[1][2]}	-	-	± 1	LSB
$E_{L(adj)}$	integral non-linearity	^[3]	-	-	± 1.5	LSB
E_O	offset error	^[4]	-	-	± 3.5	LSB
E_G	gain error	^[5]	-	-	0.6	%
E_T	absolute error	^[6]	-	-	± 4	LSB
R_{vsi}	voltage source interface resistance		-	-	40	k Ω
R_i	input resistance	^{[7][8]}	-	-	2.5	M Ω

- [1] The ADC is monotonic, there are no missing codes.
- [2] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 8.



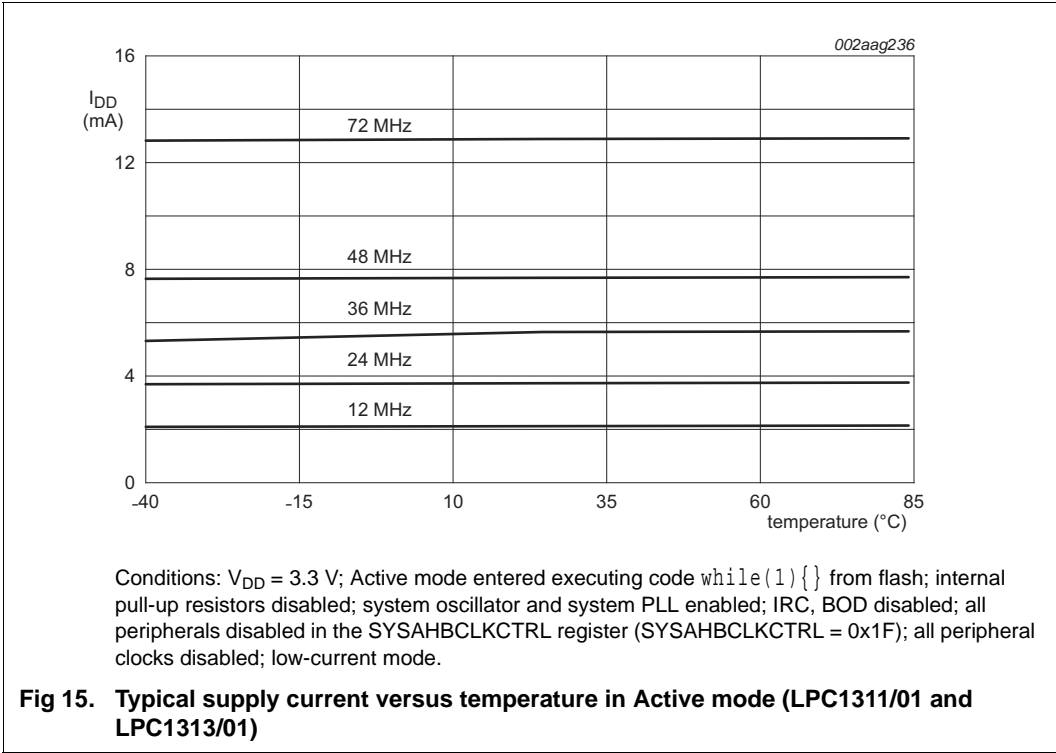
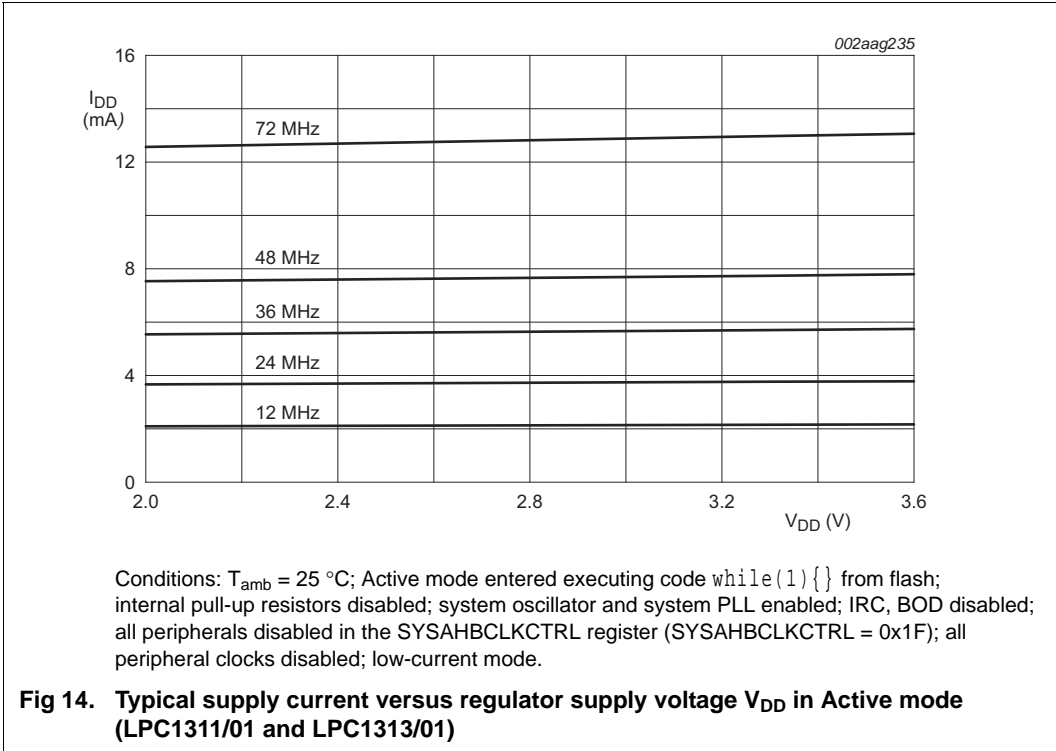


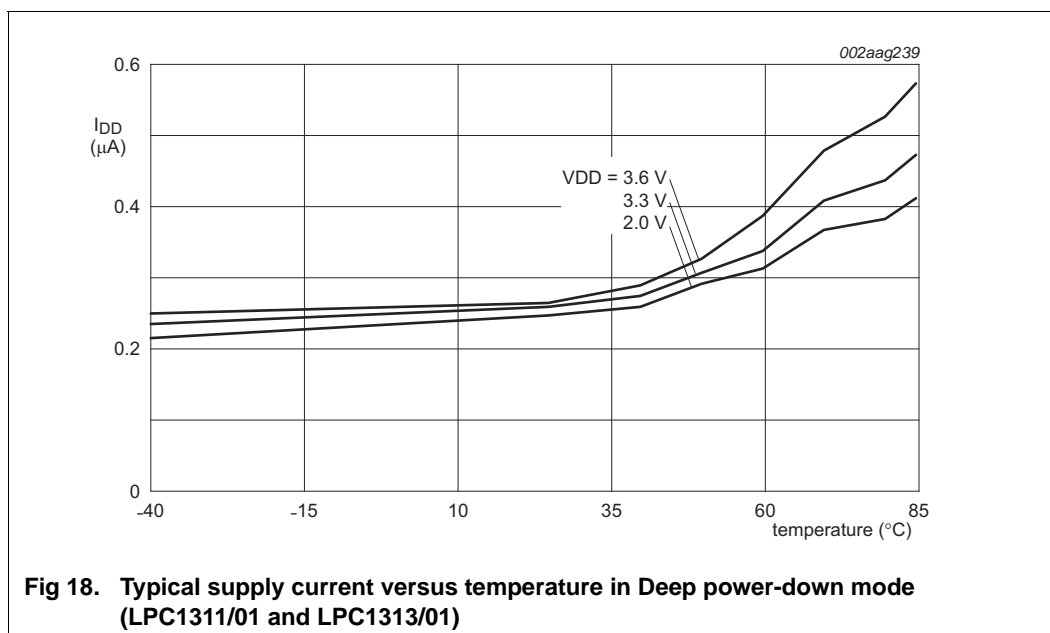
9.4 Power consumption for LPC1300L series (LPC1311/01 and LPC1313/01)

Remark: Applies to parts LPC1311/01 and LPC1313/01 and all their packages.

Power measurements in Active, Sleep, and Deep-sleep modes were performed under the following conditions (see *LPC13xx user manual*):

- Configure all pins as GPIO with pull-up resistor disabled in the IOCONFIG block.
- Configure GPIO pins as outputs using the GPIODIR registers.
- Write 0 to all GPIODATA registers to drive the outputs LOW.





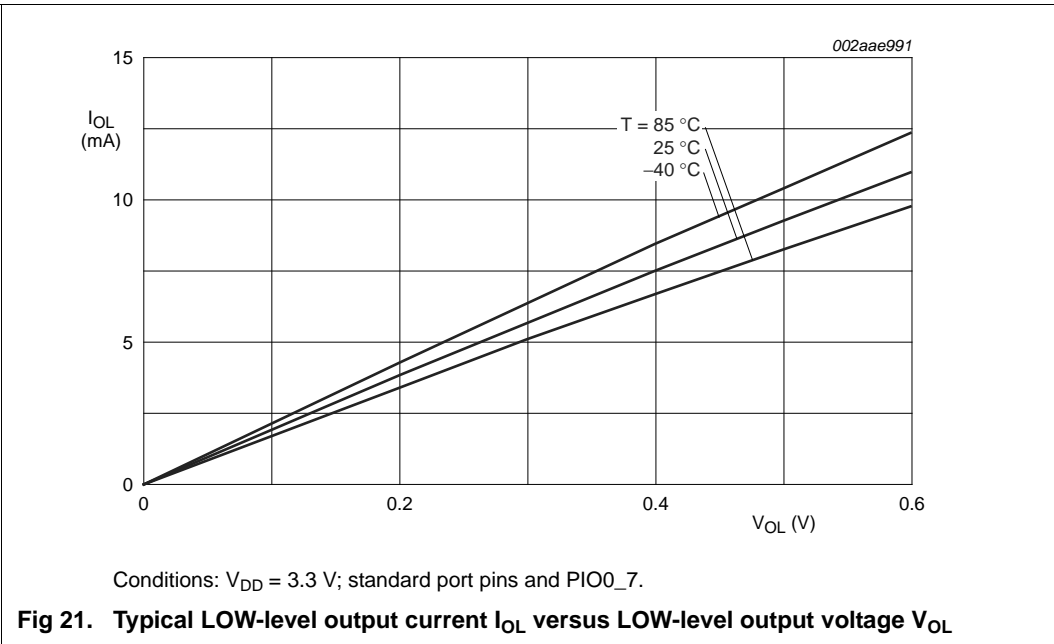
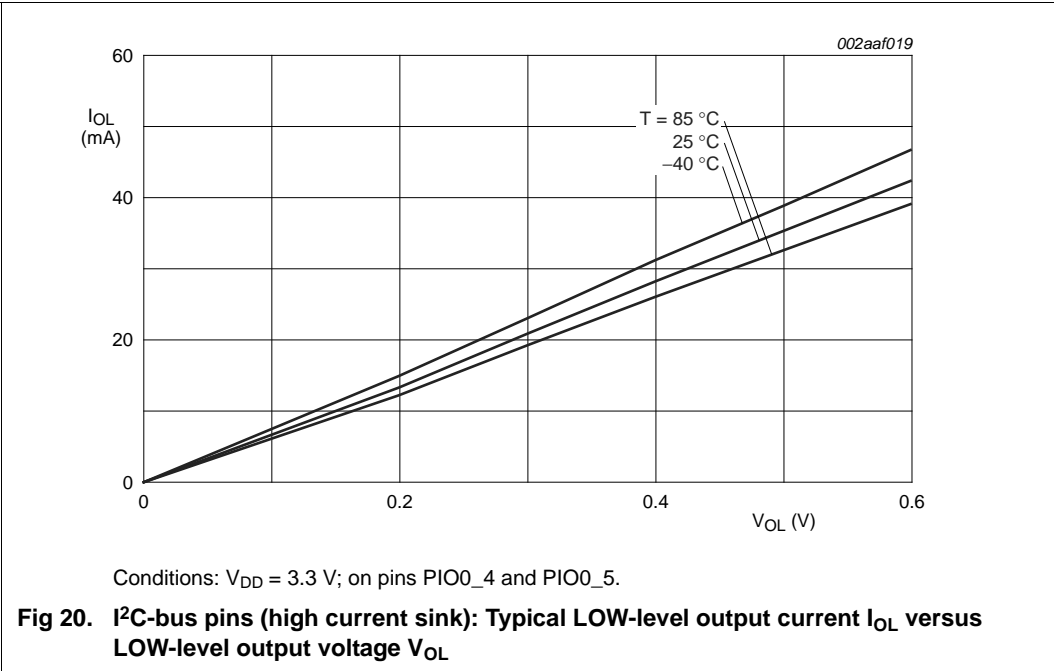
9.5 Peripheral power consumption

The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG or PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code is executed. Measured on a typical sample at $T_{amb} = 25^{\circ}\text{C}$. Unless noted otherwise, the system oscillator and PLL are running in both measurements.

The supply currents are shown for system clock frequencies of 12 MHz, 48 MHz, and 72 MHz.

Table 11. Power consumption for individual analog and digital blocks

Peripheral	Typical supply current in mA				Notes
	n/a	12 MHz	48 MHz	72 MHz	
IRC	0.23	-	-	-	System oscillator running; PLL off; independent of main clock frequency.
System oscillator at 12 MHz	0.23	-	-	-	IRC running; PLL off; independent of main clock frequency.
Watchdog oscillator at 500 kHz/2	0.002	-	-	-	System oscillator running; PLL off; independent of main clock frequency.
BOD	0.045	-	-	-	Independent of main clock frequency.
Main or USB PLL	-	0.26	0.34	0.48	-
ADC	-	0.07	0.25	0.37	-
CLKOUT	-	0.14	0.56	0.82	Main clock divided by 4 in the CLKOUTDIV register.
CT16B0	-	0.01	0.05	0.08	-
CT16B1	-	0.01	0.04	0.06	-
CT32B0	-	0.01	0.05	0.07	-
CT32B1	-	0.01	0.04	0.06	-



10.4 Internal oscillators

Table 15. Dynamic characteristics: IRC

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$; $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ [1].

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	-	11.88	12	12.12	MHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature ($25\text{ }^{\circ}\text{C}$), nominal supply voltages.

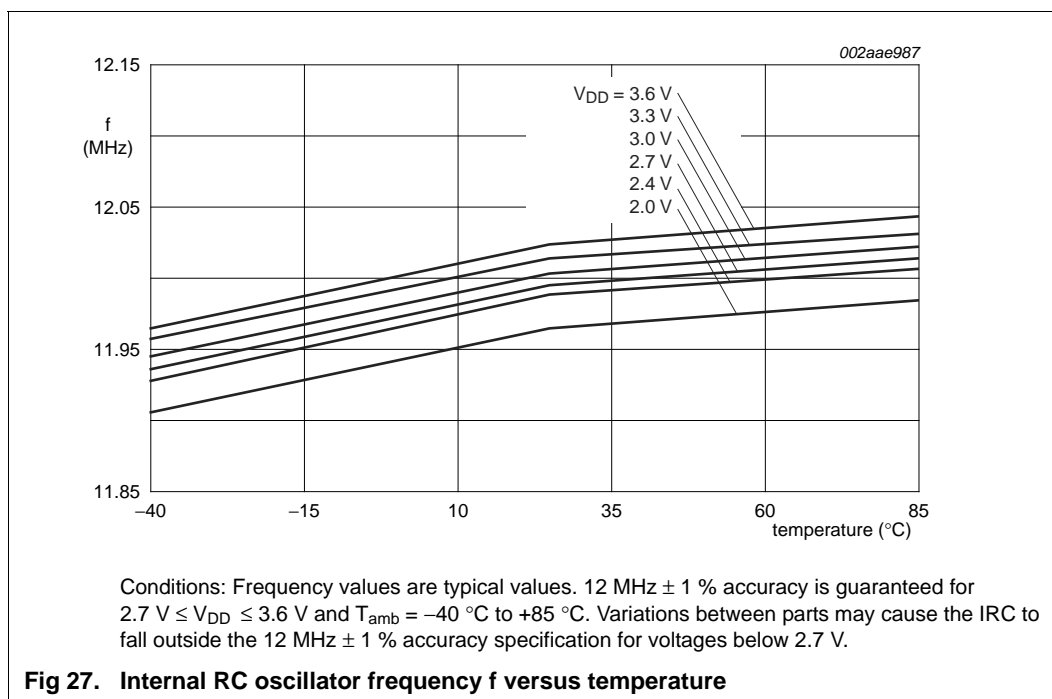


Table 16. Dynamic characteristics: Watchdog oscillator

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$f_{osc(int)}$	internal oscillator frequency	DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register;	[2][3] -	7.8	-	kHz
		DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register	[2][3] -	1700	-	kHz

[1] Typical ratings are not guaranteed. The values listed are at nominal supply voltages.

[2] The typical frequency spread over processing and temperature ($T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$) is $\pm 40\%$.

[3] See the *LPC13xx user manual*.

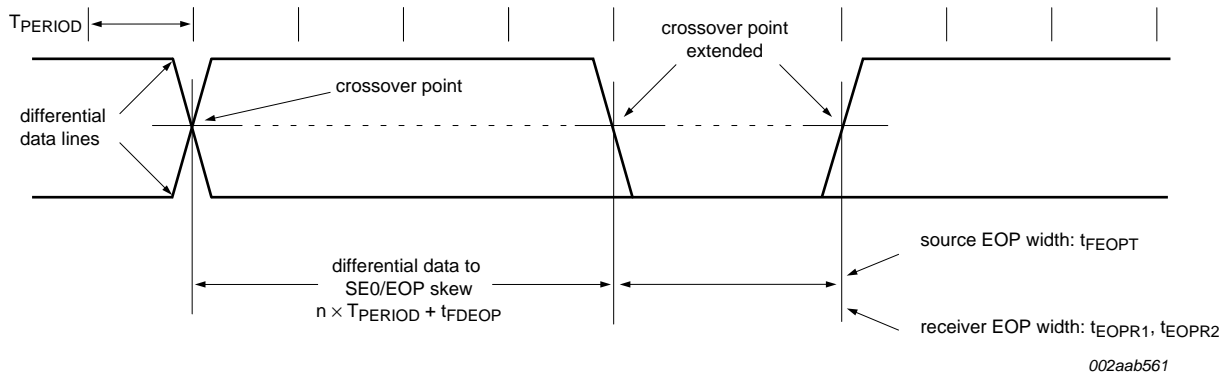
10.8 USB interface (LPC1342/43 only)

Table 20. Dynamic characteristics: USB pins (full-speed)

$C_L = 50\text{ pF}$; $R_{pu} = 1.5\text{ k}\Omega$ on D+ to V_{DD} , unless otherwise specified. $3.0\text{ V} \leq V_{DD} \leq 3.6\text{ V}$

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	10 % to 90 %	8.5	-	13.8	ns
t_f	fall time	10 % to 90 %	7.7	-	13.7	ns
t_{FRFM}	differential rise and fall time matching	t_r / t_f	-	-	109	%
V_{CRS}	output signal crossover voltage		1.3	-	2.0	V
t_{FEOP}	source SE0 interval of EOP	see Figure 31	160	-	175	ns
t_{FDEOP}	source jitter for differential transition to SE0 transition	see Figure 31	-2	-	+5	ns
t_{JR1}	receiver jitter to next transition		-18.5	-	+18.5	ns
t_{JR2}	receiver jitter for paired transitions	10 % to 90 %	-9	-	+9	ns
t_{EOPR1}	EOP width at receiver	must reject as EOP; see Figure 31	[1] 40	-	-	ns
t_{EOPR2}	EOP width at receiver	must accept as EOP; see Figure 31	[1] 82	-	-	ns

[1] Characterized but not implemented as production test. Guaranteed by design.



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Fig 31. Differential data-to-EOP transition skew and EOP width

11. Application information

11.1 Suggested USB interface solutions (LPC1342/43 only)

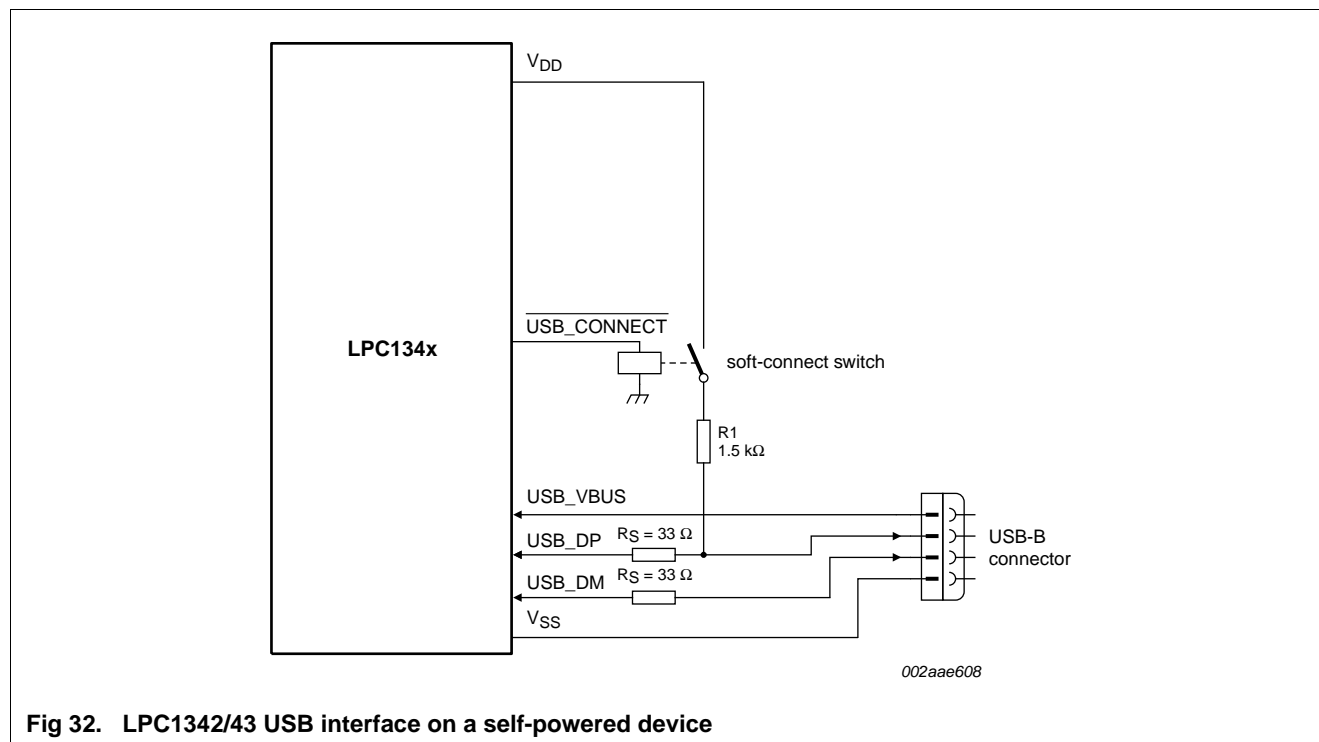


Fig 32. LPC1342/43 USB interface on a self-powered device

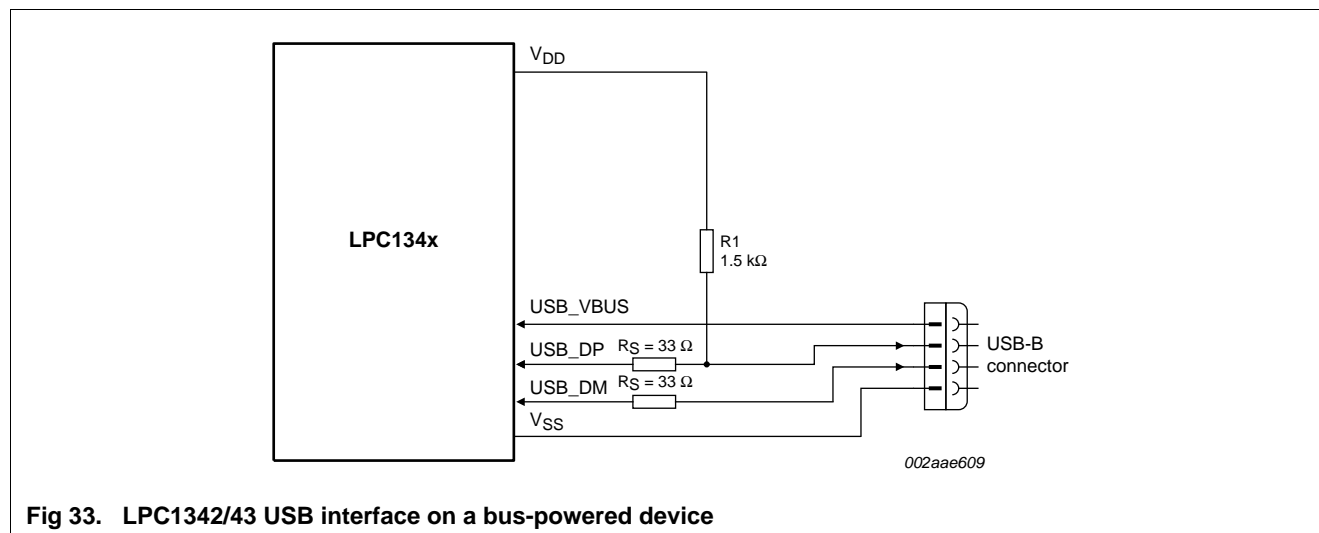


Fig 33. LPC1342/43 USB interface on a bus-powered device

11.2 XTAL input

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with $C_i = 100$ pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV(RMS) is needed.

11.4 Standard I/O pad configuration

Figure 36 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver
- Digital input: Pull-up enabled/disabled
- Digital input: Pull-down enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Analog input

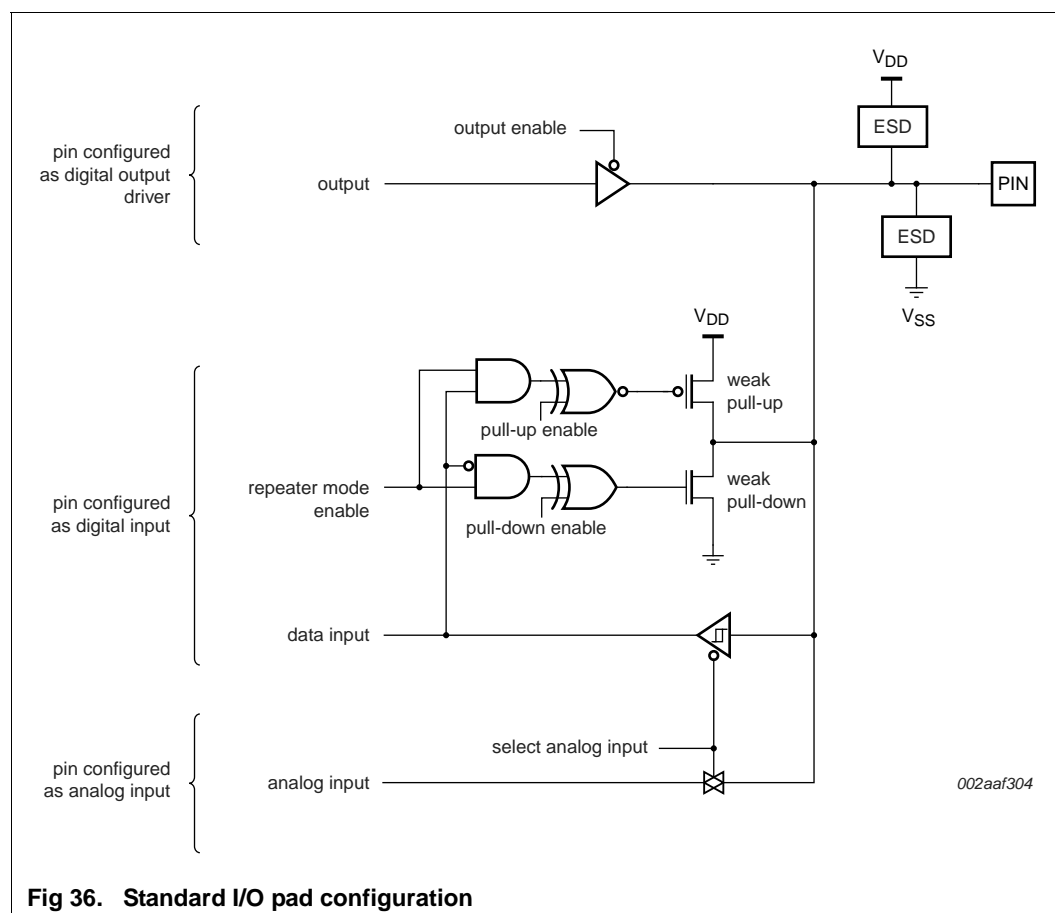


Fig 36. Standard I/O pad configuration

14. Abbreviations

Table 24. Abbreviations

Acronym	Description
A/D	Analog-to-Digital
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
EOP	End Of Packet
ETM	Embedded Trace Macrocell
FIFO	First-In, First-Out
GPIO	General Purpose Input/Output
HID	Human Interface Device
I/O	Input/Output
LSB	Least Significant Bit
MSC	Mass Storage Class
PHY	Physical Layer
PLL	Phase-Locked Loop
SE0	Single Ended Zero
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
SSP	Synchronous Serial Port
SoF	Start-of-Frame
TCM	Tightly-Coupled Memory
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

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