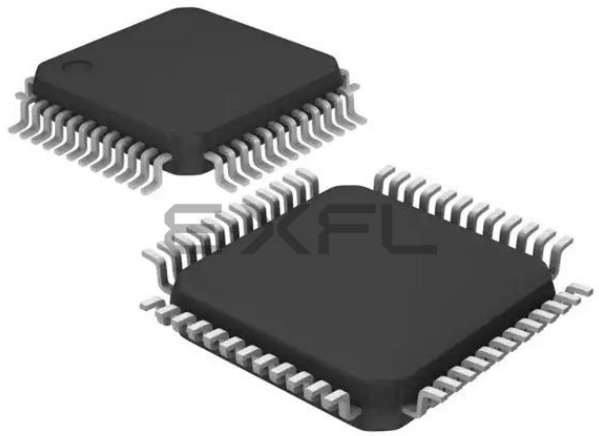

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	I²C, Microwire, SPI, SSI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	42
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1313fbd48-01-15

- Serial interfaces:
  - USB 2.0 full-speed device controller with on-chip PHY for device (LPC1342/43 only).
  - UART with fractional baud rate generation, modem, internal FIFO, and RS-485/EIA-485 support.
  - SSP controller with FIFO and multi-protocol capabilities.
  - Additional SSP controller on LPC1313FBD48/01.
  - I^2C-bus interface supporting full I^2C-bus specification and Fast-mode Plus with a data rate of 1 Mbit/s with multiple address recognition and monitor mode.
- Other peripherals:
  - Up to 42 General Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors.
  - Four general purpose counter/timers with a total of four capture inputs and 13 match outputs.
  - Programmable WatchDog Timer (WDT).
  - Programmable Windowed Watchdog Timer (WWDT) on LPC1311/01 and LPC1313/01.
  - System tick timer.
- Serial Wire Debug and Serial Wire Trace port.
- High-current output driver (20 mA) on one pin.
- High-current sink drivers (20 mA) on two I^2C-bus pins in Fast-mode Plus.
- Integrated PMU (Power Management Unit) to minimize power consumption during Sleep, Deep-sleep, and Deep power-down modes.
- Power profiles residing in boot ROM allowing to optimize performance and minimize power consumption for any given application through one simple function call. (LPC1300L series, on LPC1311/01 and LPC1313/01 only.)
- Three reduced power modes: Sleep, Deep-sleep, and Deep power-down.
- Single power supply (2.0 V to 3.6 V).
- 10-bit ADC with input multiplexing among 8 pins.
- GPIO pins can be used as edge and level sensitive interrupt sources.
- Clock output function with divider that can reflect the system oscillator clock, IRC clock, CPU clock, or the watchdog clock.
- Processor wake-up from Deep-sleep mode via a dedicated start logic using up to 40 of the functional pins.
- Brownout detect with four separate thresholds for interrupt and one threshold for forced reset (four thresholds for forced reset on the LPC1311/01 and LPC1313/01 parts).
- Power-On Reset (POR).
- Integrated oscillator with an operating range of 1 MHz to 25 MHz.
- 12 MHz internal RC oscillator trimmed to 1 % accuracy over the entire temperature and voltage range that can optionally be used as a system clock.
- Programmable watchdog oscillator with a frequency range of 7.8 kHz to 1.8 MHz.
- System PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the system oscillator or the internal RC oscillator.
- For USB (LPC1342/43), a second, dedicated PLL is provided.
- Code Read Protection (CRP) with different security levels.

Table 2. Ordering options for LPC1311/13/42/43 *…continued*

Type number	Flash	Total SRAM	USB	Power profiles	UART RS-485	I^2C/ Fast+	SSP	ADC channels	Pins	Package
LPC1342FHN33	16 kB	4 kB	Device	no	1	1	1	8	33	HVQFN33
LPC1342FBD48	16 kB	4 kB	Device	no	1	1	1	8	48	LQFP48
LPC1343FHN33	32 kB	8 kB	Device	no	1	1	1	8	33	HVQFN33
LPC1343FBD48	32 kB	8 kB	Device	no	1	1	1	8	48	LQFP48

6. Pinning information

6.1 Pinning

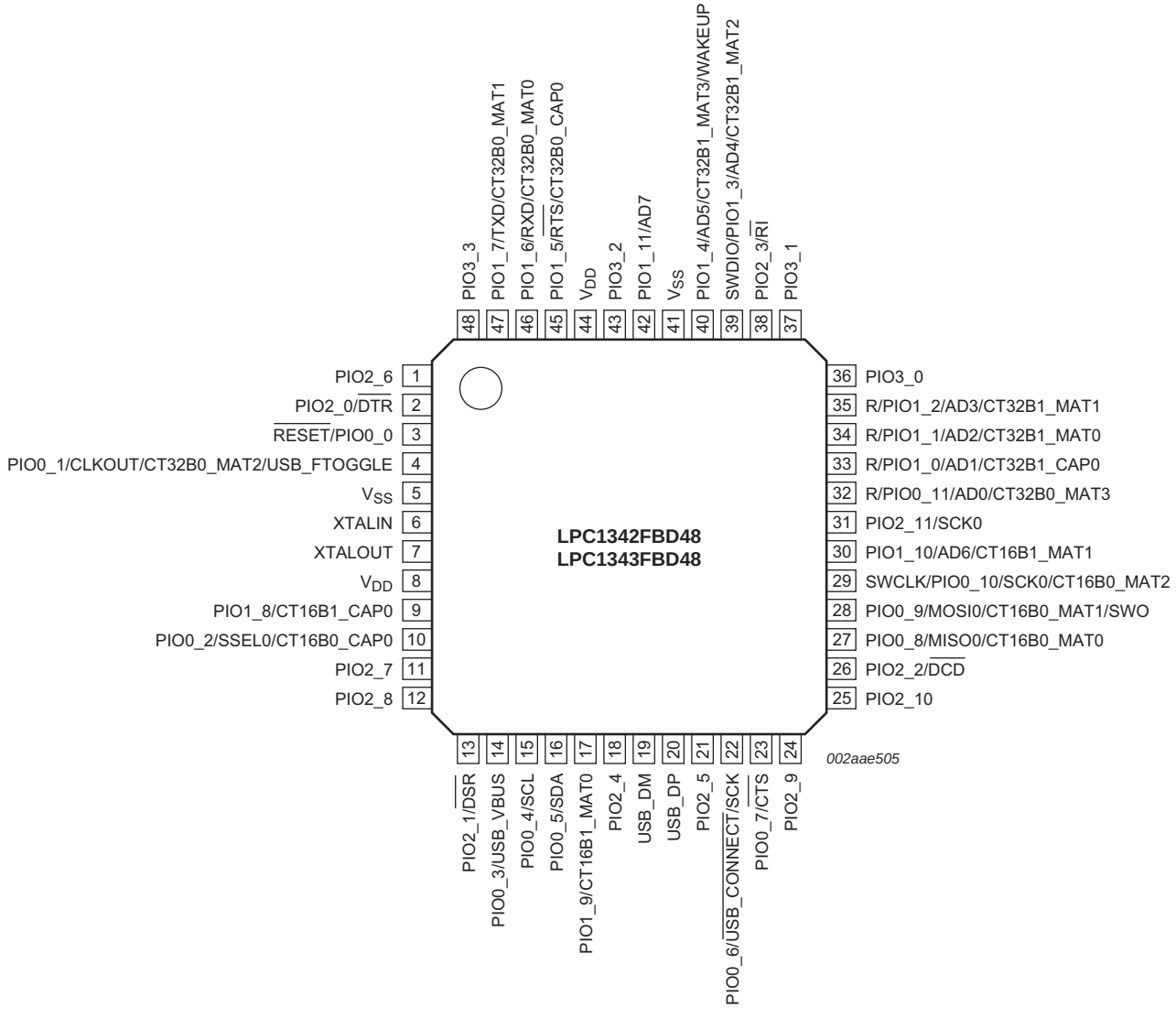


Fig 2. LPC1342/43 LQFP48 package

7. Functional description

7.1 Architectural overview

The ARM Cortex-M3 includes three AHB-Lite buses: the system bus, the I-code bus, and the D-code bus (see Figure 1). The I-code and D-code core buses are faster than the system bus and are used similarly to TCM interfaces: one bus dedicated for instruction fetch (I-code) and one bus for data access (D-code). The use of two core buses allows for simultaneous operations if concurrent operations target different devices.

7.2 ARM Cortex-M3 processor

The ARM Cortex-M3 is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption. The ARM Cortex-M3 offers many new features, including a Thumb-2 instruction set, low interrupt latency, hardware multiply and divide, interruptible/continuable multiple load and store instructions, automatic state save and restore for interrupts, tightly integrated interrupt controller, and multiple core buses capable of simultaneous accesses.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM Cortex-M3 processor is described in detail in the *Cortex-M3 Technical Reference Manual* which is available on the official ARM website.

7.3 On-chip flash program memory

The LPC1311/13/42/43 contain 32 kB (LPC1313 and LPC1343), 16 kB (LPC1342), or 8 kB (LPC1311) of on-chip flash memory.

7.4 On-chip SRAM

The LPC1311/13/42/43 contain a total of 8 kB (LPC1343 and LPC1313) or 4 kB (LPC1342 and LPC1311) on-chip static RAM memory.

7.5 Memory map

The LPC1311/13/42/43 incorporate several distinct memory regions. Figure 6 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB peripheral area is 2 MB in size and is divided to allow for up to 128 peripherals. The APB peripheral area is 512 kB in size and is divided to allow for up to 32 peripherals. Each peripheral of either type is allocated 16 kB of space. This allows simplifying the address decoding for each peripheral.

7.6.1 Features

- Controls system exceptions and peripheral interrupts.
- On the LPC1311/13/42/43, the NVIC supports up to 17 vectored interrupts. In addition, up to 40 of the individual GPIO inputs are NVIC-vector capable.
- 8 programmable interrupt priority levels, with hardware priority level masking
- Relocatable vector table.
- Software interrupt generation.

7.6.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Any GPIO pin (total of up to 42 pins) regardless of the selected function, can be programmed to generate an interrupt on a level, or rising edge or falling edge, or both.

7.7 IOCONFIG block

The IOCONFIG block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Peripherals should be connected to the appropriate pins prior to being activated and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

7.8 Fast general purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC1311/13/42/43 use accelerated GPIO functions:

- GPIO block is a dedicated AHB peripheral so that the fastest possible I/O timing can be achieved.
- Entire port value can be written in one instruction.

Additionally, any GPIO pin (total of up to 42 pins) providing a digital function can be programmed to generate an interrupt on a level, a rising or falling edge, or both.

7.8.1 Features

- Bit level port registers allow a single instruction to set or clear any number of bits in one write operation.
- Direction control of individual bits.
- All I/O default to inputs with pull-up resistors enabled after reset with the exception of the I^2C-bus pins PIO0_4 and PIO0_5.
- Pull-up/pull-down resistor configuration can be programmed through the IOCONFIG block for each GPIO pin.

7.18.5 Power control

The LPC1311/13/42/43 support a variety of power control features. There are three special modes of processor power reduction: Sleep mode, Deep-sleep mode, and Deep power-down mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals, allowing fine tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

7.18.5.1 Power profiles (LPC1300L series, LPC1311/01 and LPC1313/01 only)

The power consumption in Active and Sleep modes can be optimized for the application through simple calls to the power profile. The power configuration routine configures the LPC1311/01 and the LPC1313/01 for one of the following power modes:

- Default mode corresponding to power configuration after reset.
- CPU performance mode corresponding to optimized processing capability.
- Efficiency mode corresponding to optimized balance of current consumption and CPU performance.
- Low-current mode corresponding to lowest power consumption.

In addition, the power profile includes routines to select the optimal PLL settings for a given system clock and PLL input clock.

7.18.5.2 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

7.18.5.3 Deep-sleep mode

In Deep-sleep mode, the chip is in Sleep mode, and in addition all analog blocks are shut down. As an exception, the user has the option to keep the watchdog oscillator and the BOD circuit running for self-timed wake-up and BOD protection. Deep-sleep mode allows for additional power savings.

Up to 40 pins total can serve as external wake-up pins to the start logic to wake up the chip from Deep-sleep mode (see Section 7.19.1).

Unless the watchdog oscillator is selected to run in Deep-sleep mode, the clock source should be switched to IRC before entering Deep-sleep mode, because the IRC can be switched on and off glitch-free.

8. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage (core and external rail)			2.0	3.6	V
V_I	input voltage	5 V tolerant I/O pins; only valid when the V_{DD} supply voltage is present	[2]	−0.5	+5.5	V
I_{DD}	supply current	per supply pin		-	100	mA
I_{SS}	ground current	per ground pin		-	100	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD}) < V_I < (1.5V_{DD})$; $T_j < 125$ °C		-	100	mA
T_{stg}	storage temperature	non-operating	[3]	−65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins	[4]	−6500	+6500	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Including voltage on outputs in 3-state mode.

[3] The maximum non-operating storage temperature is different than the temperature for required shelf life which should be determined based on required shelf lifetime. Please refer to the JEDEC specification J-STD-033B.1 for further details.

[4] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

Table 7. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	$2.5\ V \le V_{DD} \le 3.6\ V$; $I_{OH} = -4\ mA$		$V_{DD} - 0.4$	-	-	V
		$2.0\ V \le V_{DD} < 2.5\ V$; $I_{OH} = -3\ mA$		$V_{DD} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	$2.5\ V \le V_{DD} \le 3.6\ V$; $I_{OL} = 4\ mA$		-	-	0.4	V
		$2.0\ V \le V_{DD} < 2.5\ V$; $I_{OL} = 3\ mA$		-	-	0.4	V
I_{OH}	HIGH-level output current	$2.5\ V \le V_{DD} \le 3.6\ V$; $V_{OH} = V_{DD} - 0.4\ V$		−4	-	-	mA
		$2.0\ V \le V_{DD} < 2.5\ V$; $V_{OH} = V_{DD} - 0.4\ V$		−3	-	-	mA
I_{OL}	LOW-level output current	$2.5\ V \le V_{DD} \le 3.6\ V$; $V_{OL} = 0.4\ V$		4	-	-	mA
		$2.0\ V \le V_{DD} < 2.5\ V$; $V_{OL} = 0.4\ V$		3	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	$V_{OH} = 0\ V$	[15]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD}$	[15]	-	-	50	mA
I_{pd}	pull-down current	$V_I = 5\ V$		10	50	150	µA
I_{pu}	pull-up current	$V_I = 0\ V$		−15	−50	−85	µA
		$V_{DD} < V_I < 5\ V$		0	0	0	µA
High-drive output pin (PIO0_7); see Figure 19 and Figure 21							
I_{IL}	LOW-level input current	$V_I = 0\ V$; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled		-	0.5	10	nA
I_{OZ}	OFF-state output current	$V_O = 0\ V$; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled		-	0.5	10	nA
V_I	input voltage	pin configured to provide a digital function	[12][13] [14]	0	-	5.0	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	$2.5\ V \le V_{DD} \le 3.6\ V$; $I_{OH} = -20\ mA$		$V_{DD} - 0.4$	-	-	V
		$2.0\ V \le V_{DD} < 2.5\ V$; $I_{OH} = -12\ mA$		$V_{DD} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	$2.5\ V \le V_{DD} \le 3.6\ V$; $I_{OL} = 4\ mA$		-	-	0.4	V
		$2.0\ V \le V_{DD} < 2.5\ V$; $I_{OL} = 3\ mA$		-	-	0.4	V

[3] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 8.

[4] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 8.

[5] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 8.

[6] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 8.

[7] T_{amb} = 25 °C; maximum sampling frequency f_s = 400 kSamples/s and analog input capacitance C_{ia} = 1 pF.

[8] Input resistance R_i depends on the sampling frequency f_s: $R_i = 1 / (f_s \times C_{ia})$.

9.2 BOD static characteristics for LPC1300L series (LPC1311/01 and LPC1313/01)

Remark: Applies to parts LPC1311/01 and LPC1313/01 and all packages.

Table 10. BOD static characteristics[1]
T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 0				
		assertion	-	1.65	-	V
		de-assertion	-	1.80	-	V
		interrupt level 1				
		assertion	-	2.22	-	V
		de-assertion	-	2.35	-	V
		interrupt level 2				
		assertion	-	2.52	-	V
		de-assertion	-	2.66	-	V
		interrupt level 3				
		assertion	-	2.80	-	V
		de-assertion	-	2.90	-	V
		reset level 0				
		assertion	-	1.46	-	V
		de-assertion	-	1.63	-	V
		reset level 1				
		assertion	-	2.06	-	V
		de-assertion	-	2.15	-	V
		reset level 2				
		assertion	-	2.35	-	V
		de-assertion	-	2.43	-	V
		reset level 3				
		assertion	-	2.63	-	V
		de-assertion	-	2.71	-	V

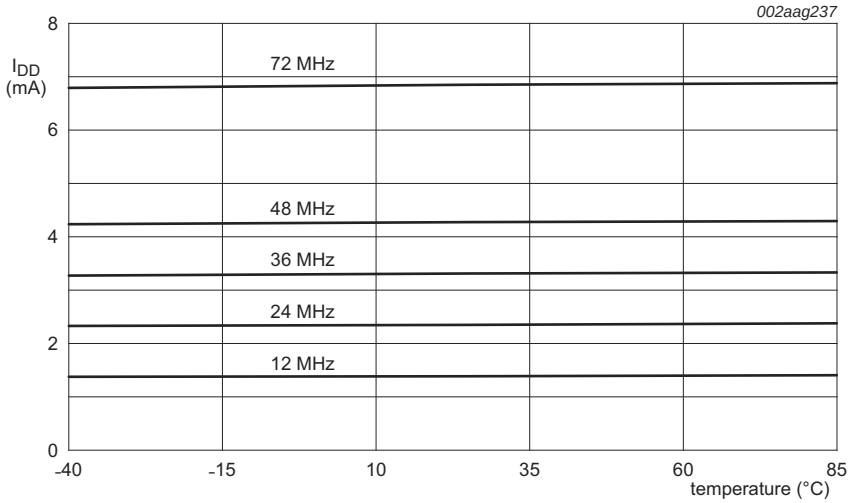
[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see *LPC13xx user manual*.

9.3 Power consumption for LPC1300 series

Remark: Applies to parts LPC1311/13/42/43 and all their packages.

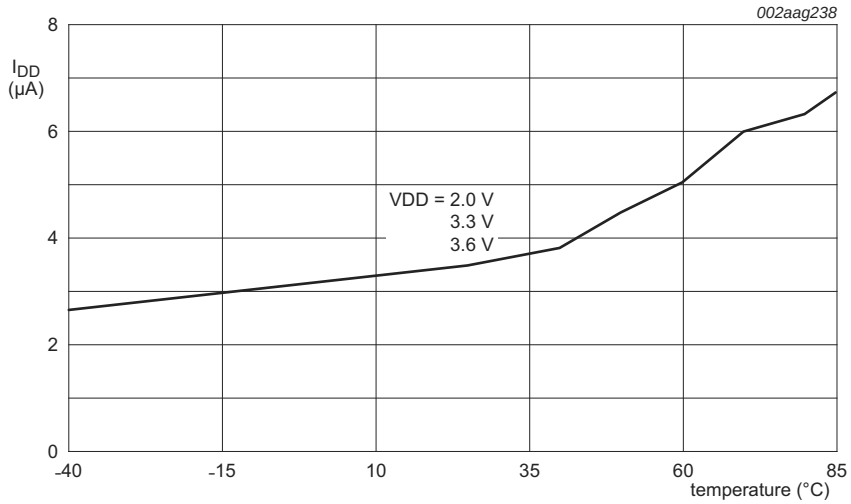
Power measurements in Active, Sleep, and Deep-sleep modes were performed under the following conditions (see *LPC13xx user manual*):

- Configure all pins as GPIO with pull-up resistor disabled in the IOCONFIG block.
- Configure GPIO pins as outputs using the GPIOnDIR registers.
- Write 0 to all GPIOnDATA registers to drive the outputs LOW.



Conditions: V_{DD} = 3.3 V; Sleep mode entered from flash; internal pull-up resistors disabled; system oscillator and system PLL enabled; IRC, BOD disabled; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; low-current mode.

Fig 16. Typical supply current versus temperature in Sleep mode (LPC1311/01 and LPC1313/01)



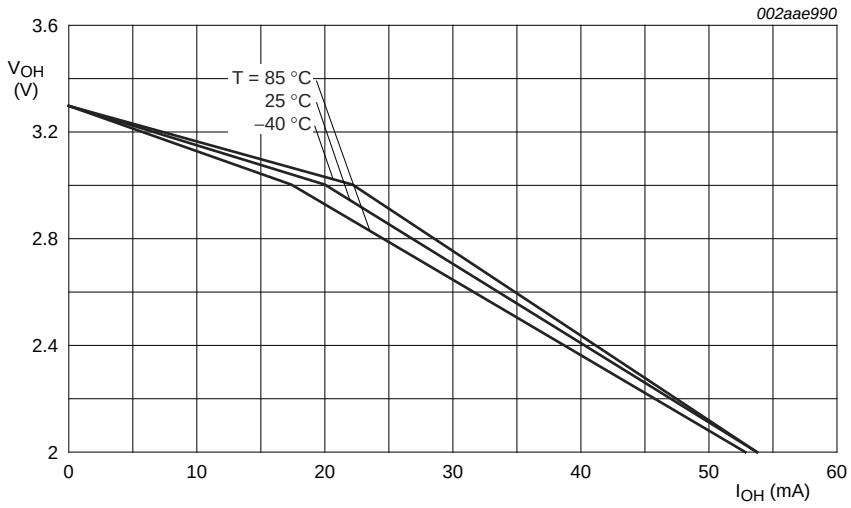
Conditions: BOD disabled; all oscillators and analog blocks turned off in the PDSLEEPCFG register; PDSLEEPCFG = 0x0000 0FFF.

Fig 17. Typical supply current versus temperature in Deep-sleep mode (analog blocks disabled, LPC1311/01 and LPC1313/01)

Table 11. Power consumption for individual analog and digital blocks *…continued*

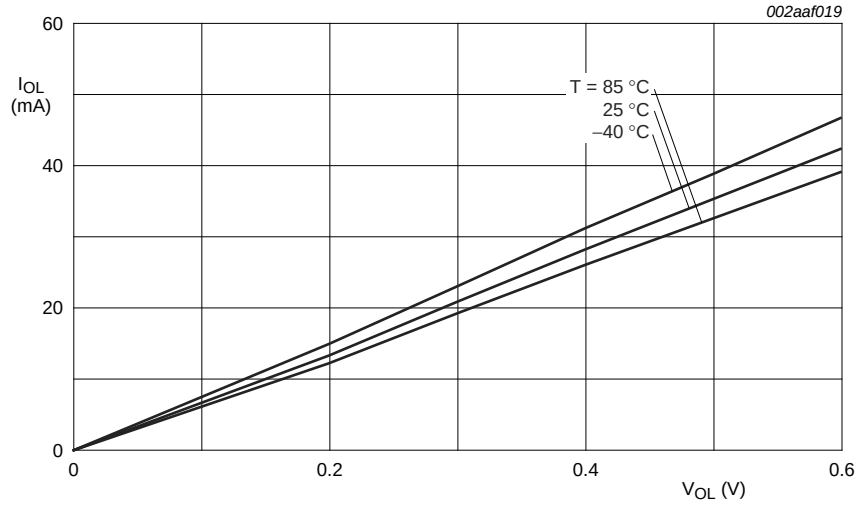
Peripheral	Typical supply current in mA				Notes
	n/a	12 MHz	48 MHz	72 MHz	
GPIO	-	0.21	0.80	1.17	GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register.
IOCONFIG	-	0.00	0.02	0.02	-
I2C	-	0.03	0.12	0.17	-
ROM	-	0.04	0.15	0.22	-
SSP0	-	0.11	0.41	0.60	-
SSP1	-	0.11	0.41	0.60	On LPC1313FBD48/01 only.
UART	-	0.20	0.76	1.11	-
WDT	-	0.01	0.05	0.08	Main clock selected as clock source for the WDT.
USB	-	-	3.91	-	Main clock selected as clock source for the USB. USB_DP and USB_DM pulled LOW externally.
USB	-	1.84	4.19	5.71	Dedicated USB PLL selected as clock source for the USB. USB_DP and USB_DM pulled LOW externally.

9.6 Electrical pin characteristics



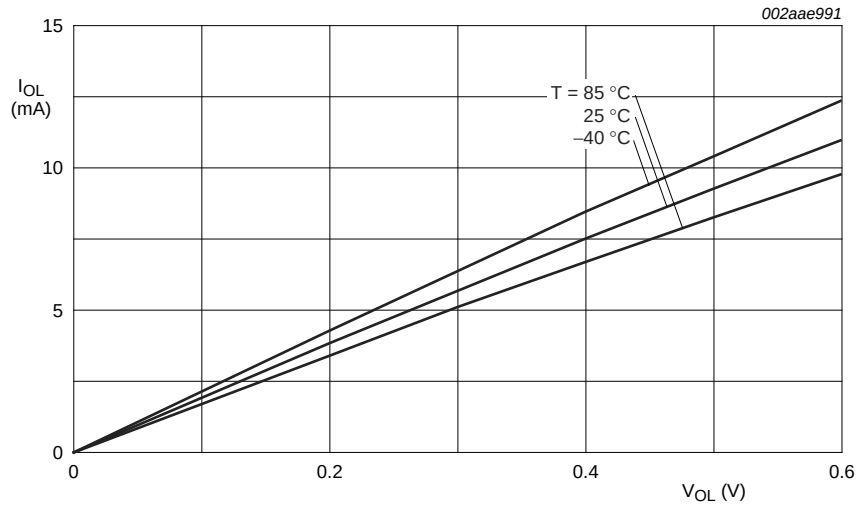
Conditions: V_{DD} = 3.3 V; on pin PIO0_7.

Fig 19. High-drive output: Typical HIGH-level output voltage V_{OH} versus HIGH-level output current I_{OH}.



Conditions: V_{DD} = 3.3 V; on pins PIO0_4 and PIO0_5.

Fig 20. I^2C-bus pins (high current sink): Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}



Conditions: V_{DD} = 3.3 V; standard port pins and PIO0_7.

Fig 21. Typical LOW-level output current I_{OL} versus LOW-level output voltage V_{OL}

10.4 Internal oscillators

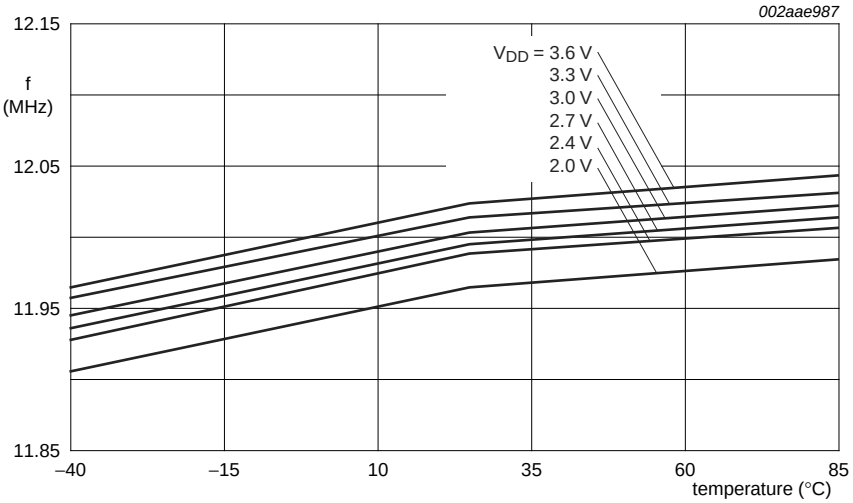
Table 15. Dynamic characteristics: IRC

T_{amb} = –40 °C to +85 °C; 2.7 V ≤ V_{DD} ≤ 3.6 V[1].

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	-	11.88	12	12.12	MHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.



Conditions: Frequency values are typical values. 12 MHz ± 1 % accuracy is guaranteed for 2.7 V ≤ V_{DD} ≤ 3.6 V and T_{amb} = –40 °C to +85 °C. Variations between parts may cause the IRC to fall outside the 12 MHz ± 1 % accuracy specification for voltages below 2.7 V.

Fig 27. Internal RC oscillator frequency f versus temperature

Table 16. Dynamic characteristics: Watchdog oscillator

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$f_{osc(int)}$	internal oscillator frequency	DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register;	[2][3]	-	7.8	-	kHz
		DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register	[2][3]	-	1700	-	kHz

[1] Typical ratings are not guaranteed. The values listed are at nominal supply voltages.

[2] The typical frequency spread over processing and temperature (T_{amb} = –40 °C to +85 °C) is ±40 %.

[3] See the *LPC13xx user manual.*

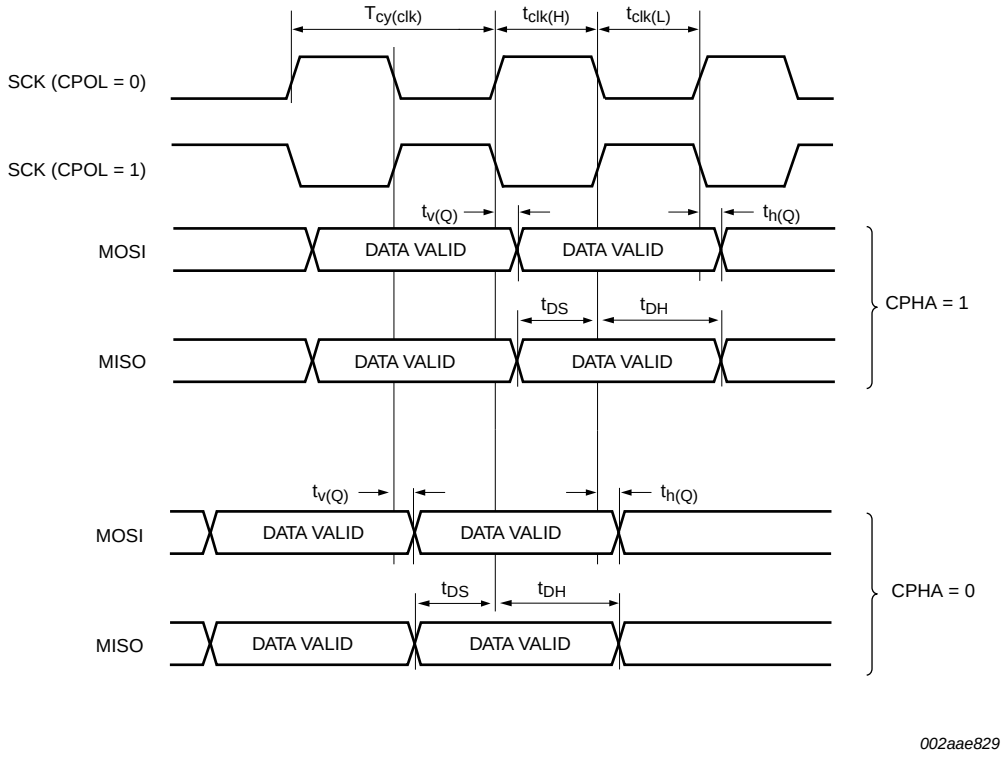


Fig 29. SSP master timing in SPI mode

10.8 USB interface (LPC1342/43 only)

Table 20. Dynamic characteristics: USB pins (full-speed)

C_L = 50 pF; R_{pu} = 1.5 kΩ on D+ to V_{DD}, unless otherwise specified. 3.0 V ≤ V_{DD} ≤ 3.6 V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_r	rise time	10 % to 90 %		8.5	-	13.8	ns
t_f	fall time	10 % to 90 %		7.7	-	13.7	ns
t_{FRFM}	differential rise and fall time matching	t_r / t_f		-	-	109	%
V_{CRS}	output signal crossover voltage			1.3	-	2.0	V
t_{FEOPT}	source SE0 interval of EOP	see Figure 31		160	-	175	ns
t_{FDEOP}	source jitter for differential transition to SE0 transition	see Figure 31		–2	-	+5	ns
t_{JR1}	receiver jitter to next transition			–18.5	-	+18.5	ns
t_{JR2}	receiver jitter for paired transitions	10 % to 90 %		–9	-	+9	ns
t_{EOPR1}	EOP width at receiver	must reject as EOP; see Figure 31	[1]	40	-	-	ns
t_{EOPR2}	EOP width at receiver	must accept as EOP; see Figure 31	[1]	82	-	-	ns

[1] Characterized but not implemented as production test. Guaranteed by design.

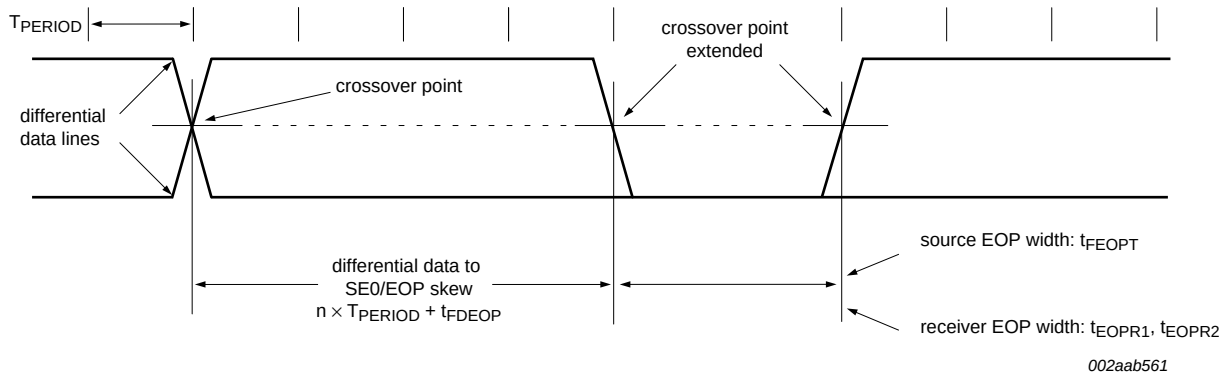


Fig 31. Differential data-to-EOP transition skew and EOP width

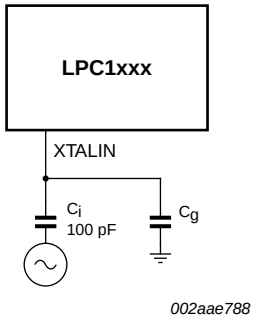


Fig 34. Slave mode operation of the on-chip oscillator

In slave mode the input clock signal should be coupled by means of a capacitor of 100 pF (Figure 34), with an amplitude between 200 mV(RMS) and 1000 mV(RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTALOUT pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in Figure 35 and in Table 21 and Table 22. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} need to be connected externally in case of fundamental mode oscillation (the fundamental frequency is represented by L, C_L and R_S). Capacitance C_P in Figure 35 represents the parallel package capacitance and should not be larger than 7 pF. Parameters F_{OSC}, C_L, R_S and C_P are supplied by the crystal manufacturer.

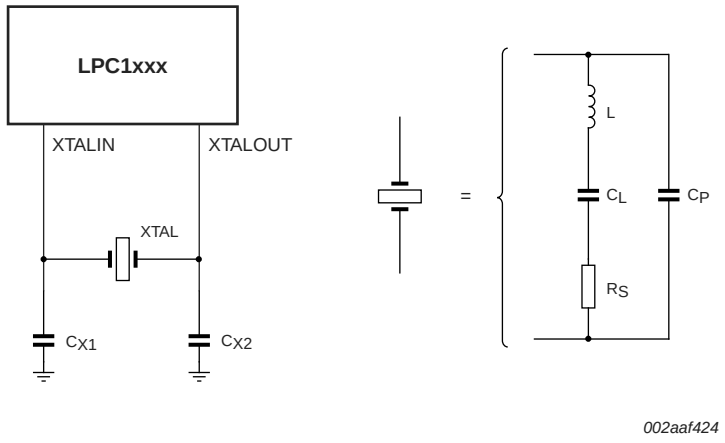


Fig 35. Oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

11.4 Standard I/O pad configuration

Figure 36 shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver
- Digital input: Pull-up enabled/disabled
- Digital input: Pull-down enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Analog input

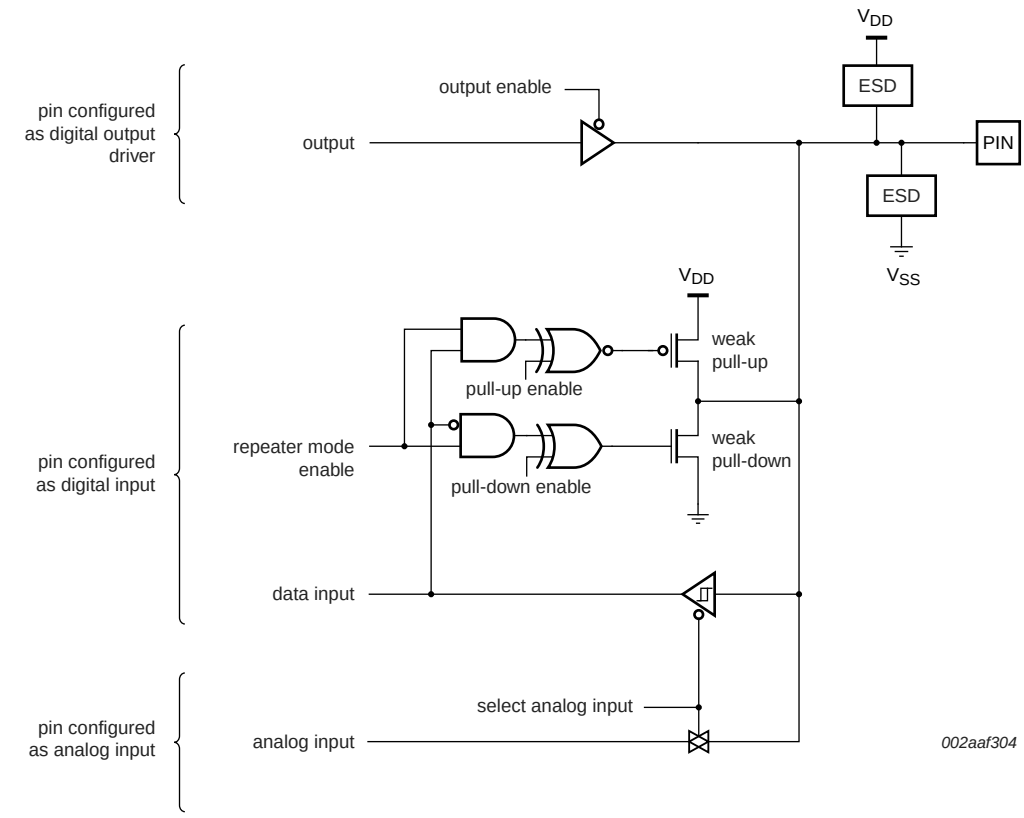


Fig 36. Standard I/O pad configuration

11.7 ElectroMagnetic Compatibility (EMC)

Radiated emission measurements according to the IEC61967-2 standard using the TEM-cell method are shown for the LPC1343FBD48 in Table 23.

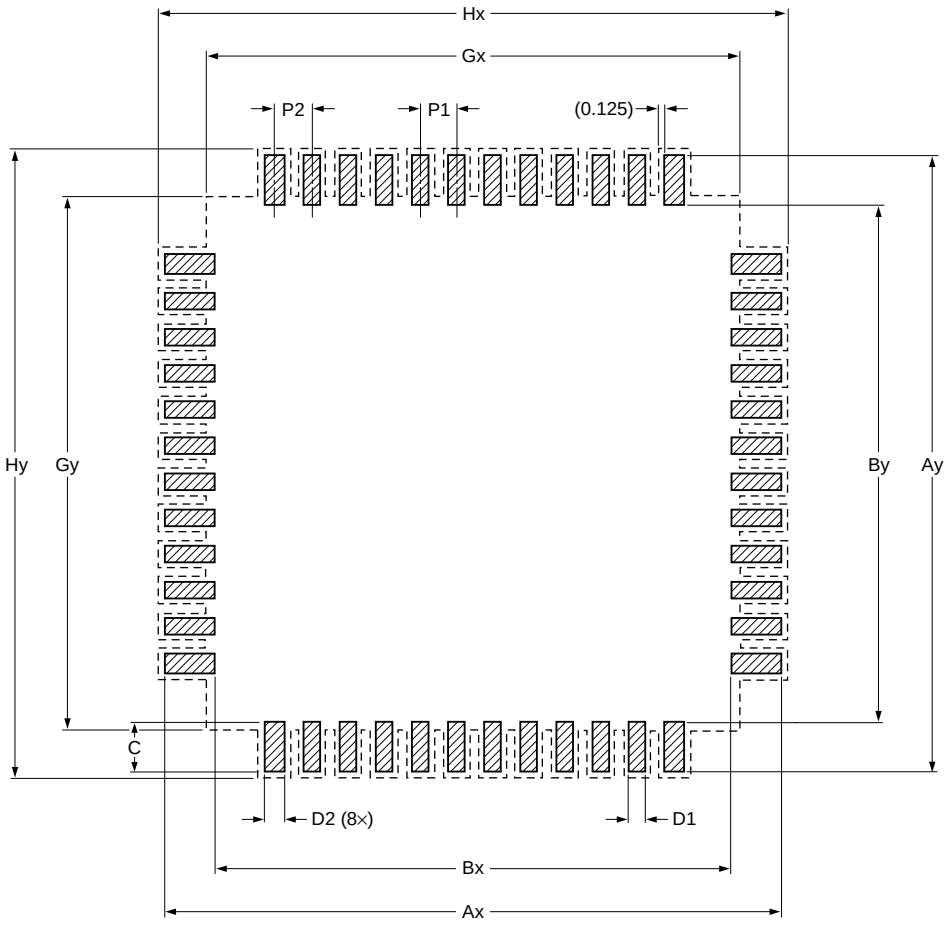
Table 23. ElectroMagnetic Compatibility (EMC) for part LPC1343FBD48 (TEM-cell method)
V_{DD} = 3.3 V; T_{amb} = 25 °C.

Parameter	Frequency band	System clock =				Unit
		12 MHz	24 MHz	48 MHz	72 MHz	
Input clock: IRC (12 MHz)						
maximum peak level	150 kHz - 30 MHz	–6	–5	–7	–7	dBµV
	30 MHz - 150 MHz	–1	+3	+9	+13	dBµV
	150 MHz - 1 GHz	+3	+7	+15	+19	dBµV
IEC level[1]	-	O	N	M	L	-
Input clock: crystal oscillator (12 MHz)						
maximum peak level	150 kHz - 30 MHz	-5	–5	–7	–7	dBµV
	30 MHz - 150 MHz	0	+4	+9	+13	dBµV
	150 MHz - 1 GHz	3	+8	+15	+20	dBµV
IEC level[1]	-	O	N	M	L	-

[1] IEC levels refer to Appendix D in the IEC61967-2 Specification.

13. Soldering

Footprint information for reflow soldering of LQFP48 package **SOT313-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	10.350	10.350	7.350	7.350	1.500	0.280	0.500	7.500	7.500	10.650	10.650

sot313-2_fr

Fig 40. Reflow soldering of the LQFP48 package