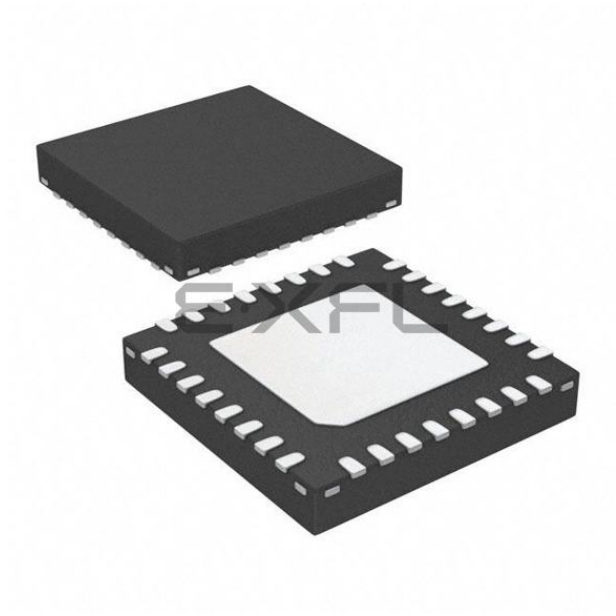

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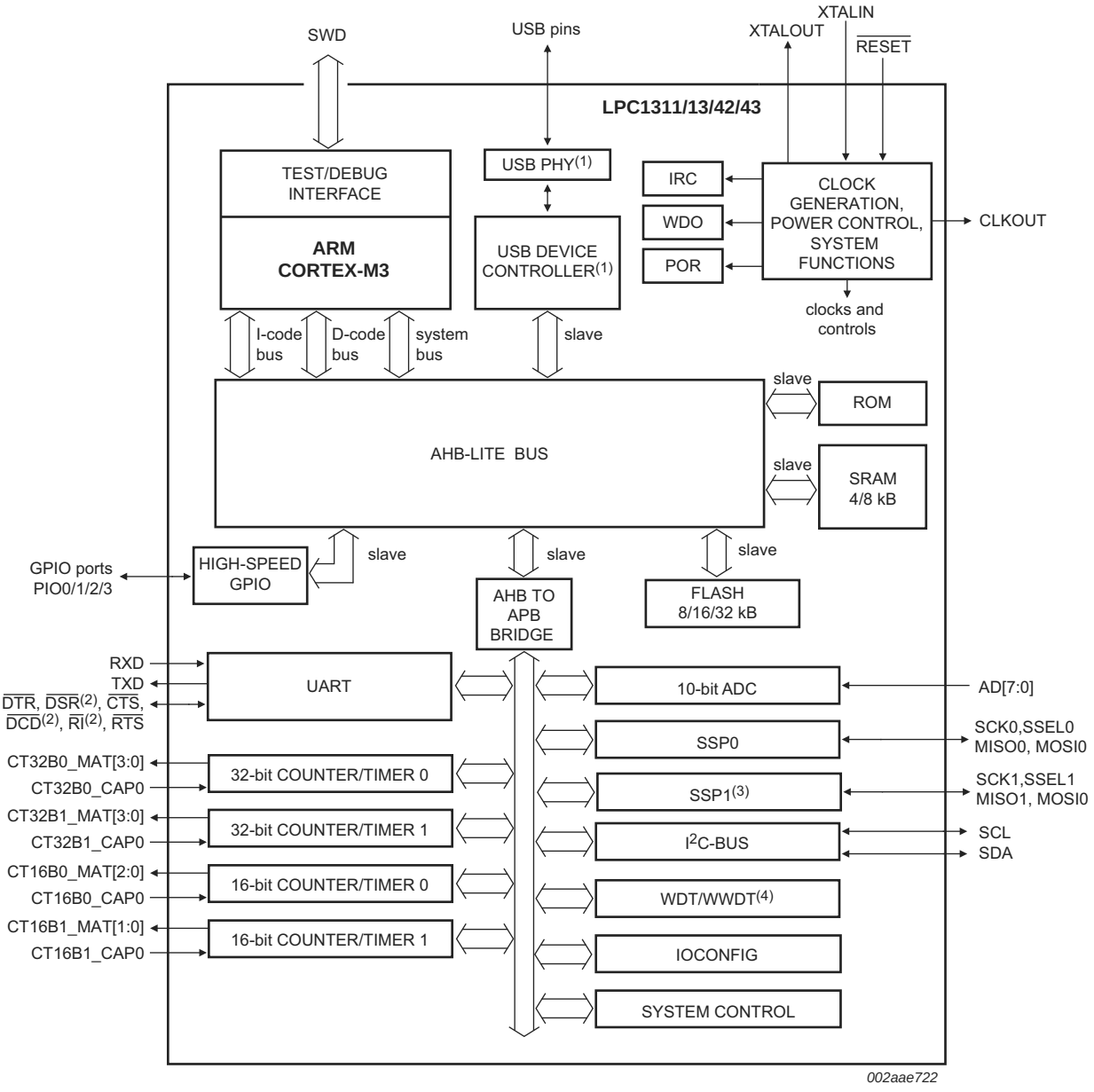
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	I²C, Microwire, SPI, SSI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	28
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VQFN Exposed Pad
Supplier Device Package	32-HVQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1313fhn33-01-51

5. Block diagram



(1) LPC1342/43 only.

(2) LQFP48 package only.

(3) On LPC1313FBD48/01 only.

(4) Windowed WatchDog Timer (WWDT) on LPC1311/01 and LPC1313/01 only.

Fig 1. Block diagram

6. Pinning information

6.1 Pinning

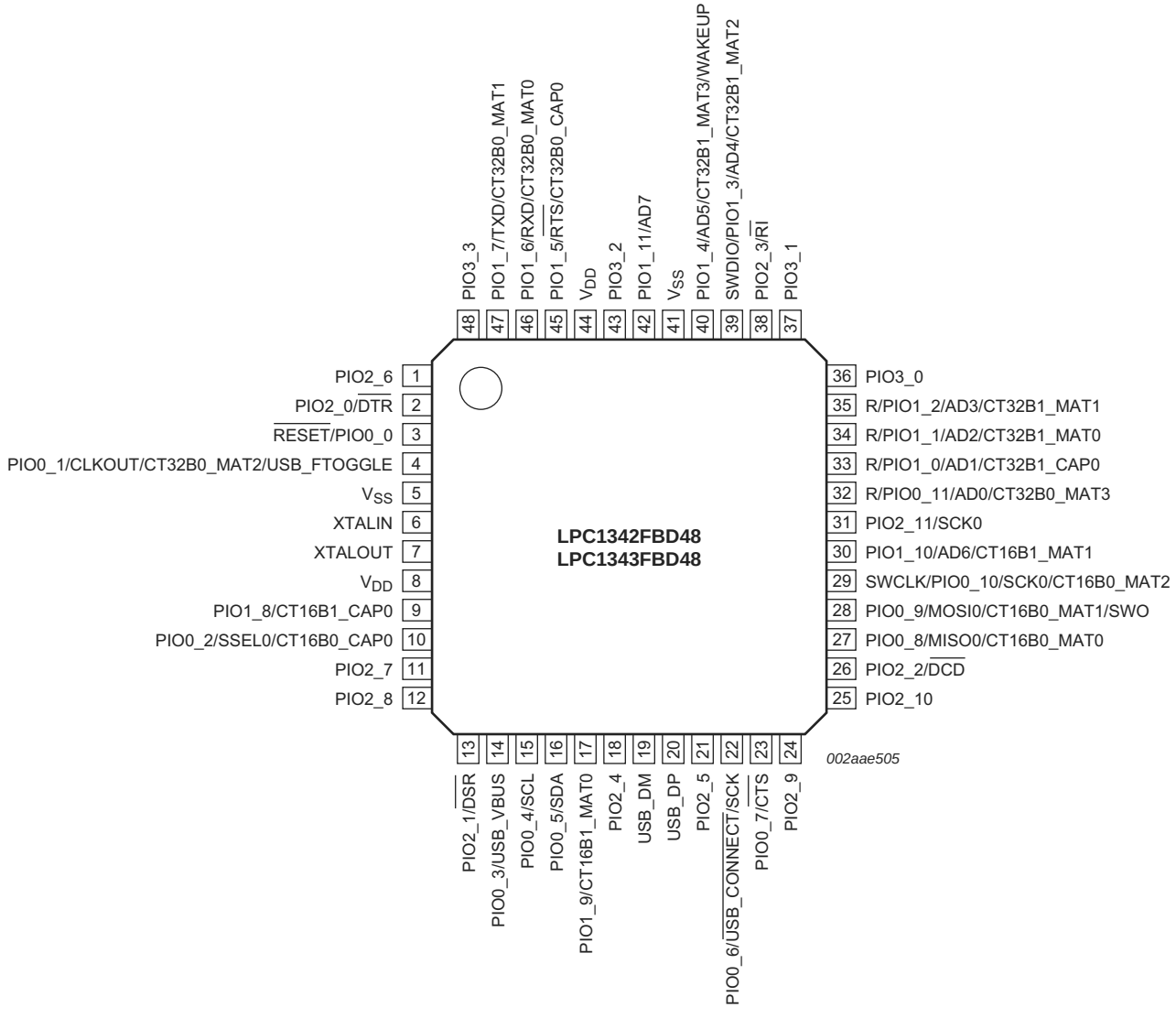


Fig 2. LPC1342/43 LQFP48 package

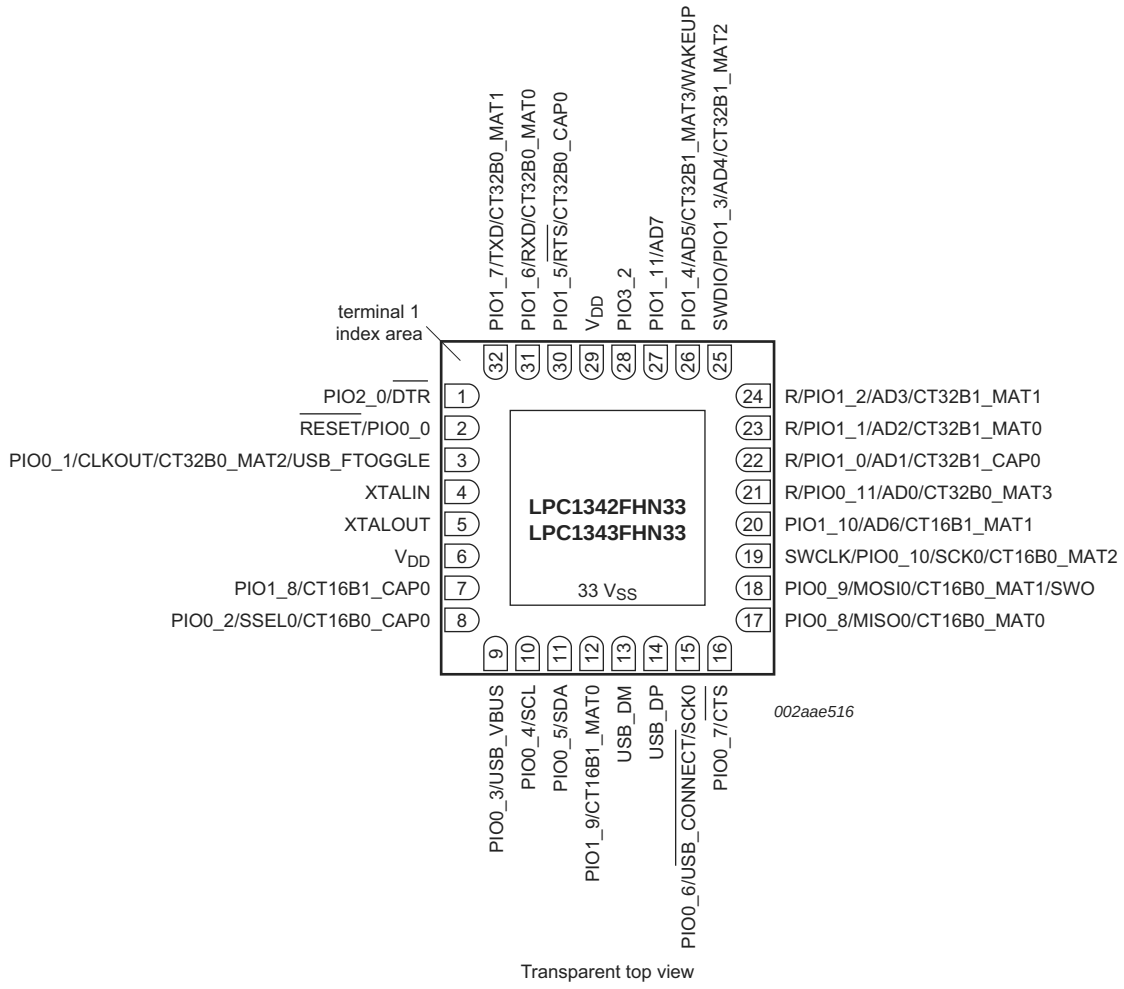


Fig 3. LPC1342/43 HVQFN33 package

Table 3. LPC1313/42/43 LQFP48 pin description table *…continued*

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
PIO0_9/MOSI0/ CT16B0_MAT1/ SWO	28[3]	yes	I/O	I; PU	**PIO0_9 —** General purpose digital input/output pin.
			I/O	-	**MOSI0 —** Master Out Slave In for SSP0.
			O	-	**CT16B0_MAT1 —** Match output 1 for 16-bit timer 0.
			O	-	**SWO —** Serial wire trace output.
SWCLK/PIO0_10/ SCK0/CT16B0_MAT2	29[3]	yes	I	I; PU	**SWCLK —** Serial wire clock.
			I/O	-	**PIO0_10 —** General purpose digital input/output pin.
			I/O	-	**SCK0 —** Serial clock for SSP0.
			O	-	**CT16B0_MAT2 —** Match output 2 for 16-bit timer 0.
R/PIO0_11/ AD0/CT32B0_MAT3	32[5]	yes	-	I; PU	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	**PIO0_11 —** General purpose digital input/output pin.
			I	-	**AD0 —** A/D converter, input 0.
			O	-	**CT32B0_MAT3 —** Match output 3 for 32-bit timer 0.
R/PIO1_0/ AD1/CT32B1_CAP0	33[5]	yes	-	I; PU	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	**PIO1_0 —** General purpose digital input/output pin.
			I	-	**AD1 —** A/D converter, input 1.
			I	-	**CT32B1_CAP0 —** Capture input 0 for 32-bit timer 1.
R/PIO1_1/ AD2/CT32B1_MAT0	34[5]	yes	-	I; PU	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	**PIO1_1 —** General purpose digital input/output pin.
			I	-	**AD2 —** A/D converter, input 2.
			O	-	**CT32B1_MAT0 —** Match output 0 for 32-bit timer 1.
R/PIO1_2/ AD3/CT32B1_MAT1	35[5]	yes	-	I; PU	**R —** Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	**PIO1_2 —** General purpose digital input/output pin.
			I	-	**AD3 —** A/D converter, input 3.
			O	-	**CT32B1_MAT1 —** Match output 1 for 32-bit timer 1.
SWDIO/PIO1_3/ AD4/ CT32B1_MAT2	39[5]	yes	I/O	I; PU	**SWDIO —** Serial wire debug input/output.
			I/O	-	**PIO1_3 —** General purpose digital input/output pin.
			I	-	**AD4 —** A/D converter, input 4.
			O	-	**CT32B1_MAT2 —** Match output 2 for 32-bit timer 1.
PIO1_4/AD5/ CT32B1_MAT3/ WAKEUP	40[5]	yes	I/O	I; PU	**PIO1_4 —** General purpose digital input/output pin.
			I	-	**AD5 —** A/D converter, input 5.
			O	-	**CT32B1_MAT3 —** Match output 3 for 32-bit timer 1.
			I	-	**WAKEUP —** Deep power-down mode wake-up pin with 20 ns glitch filter. This pin must be pulled HIGH externally to enter Deep power-down mode and pulled LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.

Table 4. LPC1311/13/42/43 HVQFN33 pin description table *…continued*

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
PIO1_7/TXD/ CT32B0_MAT1	32[3]	yes	I/O	I; PU	**PIO1_7 —** General purpose digital input/output pin.
			O	-	**TXD —** Transmitter output for UART.
			O	-	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
PIO1_8/ CT16B1_CAP0	7[3]	yes	I/O	I; PU	**PIO1_8 —** General purpose digital input/output pin.
			I	-	**CT16B1_CAP0 —** Capture input 0 for 16-bit timer 1.
PIO1_9/ CT16B1_MAT0	12[3]	yes	I/O	I; PU	**PIO1_9 —** General purpose digital input/output pin.
			O	-	**CT16B1_MAT0 —** Match output 0 for 16-bit timer 1.
PIO1_10/AD6/ CT16B1_MAT1	20[5]	yes	I/O	I; PU	**PIO1_10 —** General purpose digital input/output pin.
			I	-	**AD6 —** A/D converter, input 6.
			O	-	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
PIO1_11/AD7	27[5]	yes	I/O	I; PU	**PIO1_11 —** General purpose digital input/output pin.
			I	-	**AD7 —** A/D converter, input 7.
PIO2_0/$\overline{\text{DTR}}$	1[3]	yes	I/O	I; PU	**PIO2_0 —** General purpose digital input/output pin.
			O	-	**$\overline{\text{DTR}}$ —** Data Terminal Ready output for UART.
PIO3_2	28[3]	yes	I/O	I; PU	**PIO3_2 —** General purpose digital input/output pin.
PIO3_4	13[3]	no	I/O	I; PU	**PIO3_4 —** General purpose digital input/output pin (LPC1311/13 only).
PIO3_5	14[3]	no	I/O	I; PU	**PIO3_5 —** General purpose digital input/output pin (LPC1311/13 only).
USB_DM	13[6]	no	I/O	F	**USB_DM —** USB bidirectional D− line (LPC1342/43 only).
USB_DP	14[6]	no	I/O	F	**USB_DP —** USB bidirectional D+ line (LPC1342/43 only).
V_{DD}	6; 29	-	I	-	3.3 V supply voltage to the internal regulator, the external rail, and the ADC. Also used as the ADC reference voltage.
XTALIN	4[7]	-	I	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	5[7]	-	O	-	Output from the oscillator amplifier.
V_{SS}	33	-	-	-	Thermal pad. Connect to ground.

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled (for V_{DD} = 3.3 V, pin is pulled up to 2.6 V for parts LPC1311/13/42/43 and pulled up to 3.3 V for parts LPC1311/01 and LPC1313/01); IA = inactive, no pull-up/down enabled. F = floating; floating pins, if not used, should be tied to ground or power to minimize power consumption.

[2] 5 V tolerant pad. See Figure 37 for pad characteristics. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 36).

[4] I^2C-bus pads compliant with the I^2C-bus specification for I^2C standard mode and I^2C Fast-mode Plus.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled, and the pin is not 5 V tolerant (see Figure 36).

[6] Pad provides USB functions. It is designed in accordance with the USB specification, revision 2.0 (Full-speed and Low-speed mode only). This pad is not 5 V tolerant.

[7] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

7.10 UART

The LPC1311/13/42/43 contains one UART.

Support for RS-485/9-bit mode allows both software address detection and automatic address detection using 9-bit mode.

The UART includes a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.10.1 Features

- Maximum UART data bit rate of 4.5 MBit/s.
- 16-byte receive and transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Fractional divider for baud rate control, auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit mode.
- Support for modem control.

7.11 SSP serial I/O controller

The LPC1311/13/42/43 contain one SSP controller. An additional SSP controller is available on the LPC1313FBD48/01 package.

The SSP controller is capable of operation on a SSP, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

7.11.1 Features

- Maximum SSP speed of 36 Mbit/s (master) or 6 Mbit/s (slave)
- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame

7.12 I^2C-bus serial I/O controller

The LPC1311/13/42/43 contain one I^2C-bus controller.

- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the Internal RC oscillator (IRC), the watchdog oscillator, or the main clock. This gives a wide range of potential timing choices of watchdog operation under different power reduction conditions. It also provides the ability to run the WDT from an entirely internal source that is not dependent on an external crystal and its associated components and wiring for increased reliability.

7.17 Windowed WatchDog Timer (WWDT)

Remark: The windowed watchdog timer is available on parts LPC1311/01 and LPC1313/01.

The purpose of the watchdog is to reset the controller if software fails to periodically service it within a programmable time window.

7.17.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the IRC or the dedicated watchdog oscillator (WDO). This gives a wide range of potential timing choices of watchdog operation under different power conditions.

7.18 Clocking and power control

7.18.1 Integrated oscillators

The LPC1311/13/42/43 include three independent oscillators. These are the system oscillator, the Internal RC oscillator (IRC), and the watchdog oscillator. Each oscillator can be used for more than one purpose as required in a particular application.

Following reset, the LPC1311/13/42/43 will operate from the internal RC oscillator until switched by software. This allows systems to operate without any external crystal and the bootloader code to operate at a known frequency.

See Figure 7 for an overview of the LPC1311/13/42/43 clock generation.

There are three levels of Code Read Protection:

1. CRP1 disables access to chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors can not be erased.
2. CRP2 disables access to chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected fully disables any access to chip via the SWD pins and the ISP. This mode effectively disables ISP override using PIO0_1 pin, too. It is up to the user's application to provide (if needed) flash update mechanism using IAP calls or call reinvoke ISP command to enable flash update via UART.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

7.19.5 Boot loader

The boot loader controls initial operation after reset and also provides the means to program the flash memory. This could be initial programming of a blank device, erasure and re-programming of a previously programmed device, or programming of the flash memory by the application program in a running system.

The boot loader code is executed every time the part is reset or powered up. The loader can either execute the ISP command handler or the user application code, or, on the LPC1342/43, it can program the flash image via an attached MSC device through USB (Windows operating system only). A LOW level during reset applied to the PIO0_1 pin is considered as an external hardware request to start the ISP command handler or the USB device enumeration. The state of PIO0_3 determines whether the UART or USB interface will be used (LPC1342/43 only).

7.19.6 APB interface

The APB peripherals are located on one APB bus.

7.19.7 AHB-Lite

The AHB-Lite connects the instruction (I-code) and data (D-code) CPU buses of the ARM Cortex-M3 to the flash memory, the main static RAM, and the boot ROM.

7.19.8 External interrupt inputs

All GPIO pins can be level or edge sensitive interrupt inputs. In addition, start logic inputs serve as external interrupts (see Section 7.19.1).

7.19.9 Memory mapping control

The Cortex-M3 incorporates a mechanism that allows remapping the interrupt vector table to alternate locations in the memory map. This is controlled via the Vector Table Offset Register contained in the NVIC.

The vector table may be located anywhere within the bottom 1 GB of Cortex-M3 address space. The vector table must be located on a 256 word boundary.

7.20 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M3. Serial wire debug is supported.

8. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage (core and external rail)			2.0	3.6	V
V_I	input voltage	5 V tolerant I/O pins; only valid when the V_{DD} supply voltage is present	[2]	−0.5	+5.5	V
I_{DD}	supply current	per supply pin		-	100	mA
I_{SS}	ground current	per ground pin		-	100	mA
I_{latch}	I/O latch-up current	$-(0.5V_{DD}) < V_I < (1.5V_{DD})$; $T_j < 125$ °C		-	100	mA
T_{stg}	storage temperature	non-operating	[3]	−65	+150	°C
$T_{j(max)}$	maximum junction temperature			-	150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{ESD}	electrostatic discharge voltage	human body model; all pins	[4]	−6500	+6500	V

[1] The following applies to the limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Including voltage on outputs in 3-state mode.

[3] The maximum non-operating storage temperature is different than the temperature for required shelf life which should be determined based on required shelf lifetime. Please refer to the JEDEC specification J-STD-033B.1 for further details.

[4] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

Table 7. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{OH}	HIGH-level output current	2.5 V ≤ V_{DD} ≤ 3.6 V; V_{OH} = V_{DD} − 0.4 V		20	-	-	mA
		2.0 V ≤ V_{DD} < 2.5 V; V_{OH} = V_{DD} − 0.4 V;		12	-	-	mA
I_{OL}	LOW-level output current	2.5 V ≤ V_{DD} ≤ 3.6 V; V_{OL} = 0.4 V		4	-	-	mA
		2.0 V ≤ V_{DD} < 2.5 V; V_{OL} = 0.4 V		3	-	-	mA
I_{pd}	pull-down current	V_I = 5 V		10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V		−15	−50	−85	µA
		V_{DD} < V_I < 5 V		0	0	0	µA
I^2C-bus pins (PIO0_4 and PIO0_5); see Figure 20							
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3V_{DD}	V
V_{hys}	hysteresis voltage			-	0.05V_{DD}	-	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as standard mode pins					
		2.5 V ≤ V_{DD} ≤ 3.6 V		3.5	-	-	mA
		2.0 V ≤ V_{DD} < 2.5 V		3.0	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as Fast-mode Plus pins					
		2.5 V ≤ V_{DD} ≤ 3.6 V		20	-	-	mA
		2.0 V ≤ V_{DD} < 2.5 V		16	-	-	
I_{LI}	input leakage current	V_I = V_{DD}	[16]	-	2	4	µA
		V_I = 5 V		-	10	22	µA
Oscillator pins							
$V_{i(xtal)}$	crystal input voltage			−0.5	+1.8	+1.95	V
$V_{o(xtal)}$	crystal output voltage			−0.5	+1.8	+1.95	V
USB pins (LPC1342/43 only)							
I_{OZ}	OFF-state output current	0 V < V_I < 3.3 V	[17]	-	-	±10	µA
V_{BUS}	bus supply voltage		[17]	-	-	5.25	V
V_{DI}	differential input sensitivity voltage	|(D+) − (D−)|	[17]	0.2	-	-	V
V_{CM}	differential common mode voltage range	includes V_{DI} range	[17]	0.8	-	2.5	V
$V_{th(rs)se}$	single-ended receiver switching threshold voltage		[17]	0.8	-	2.0	V
V_{OL}	LOW-level output voltage	for low-/full-speed; R_L of 1.5 kΩ to 3.6 V	[17]	-	-	0.18	V

9.2 BOD static characteristics for LPC1300L series (LPC1311/01 and LPC1313/01)

Remark: Applies to parts LPC1311/01 and LPC1313/01 and all packages.

Table 10. BOD static characteristics[1]
T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 0				
		assertion	-	1.65	-	V
		de-assertion	-	1.80	-	V
		interrupt level 1				
		assertion	-	2.22	-	V
		de-assertion	-	2.35	-	V
		interrupt level 2				
		assertion	-	2.52	-	V
		de-assertion	-	2.66	-	V
		interrupt level 3				
		assertion	-	2.80	-	V
		de-assertion	-	2.90	-	V
		reset level 0				
		assertion	-	1.46	-	V
		de-assertion	-	1.63	-	V
		reset level 1				
		assertion	-	2.06	-	V
		de-assertion	-	2.15	-	V
		reset level 2				
		assertion	-	2.35	-	V
		de-assertion	-	2.43	-	V
		reset level 3				
		assertion	-	2.63	-	V
		de-assertion	-	2.71	-	V

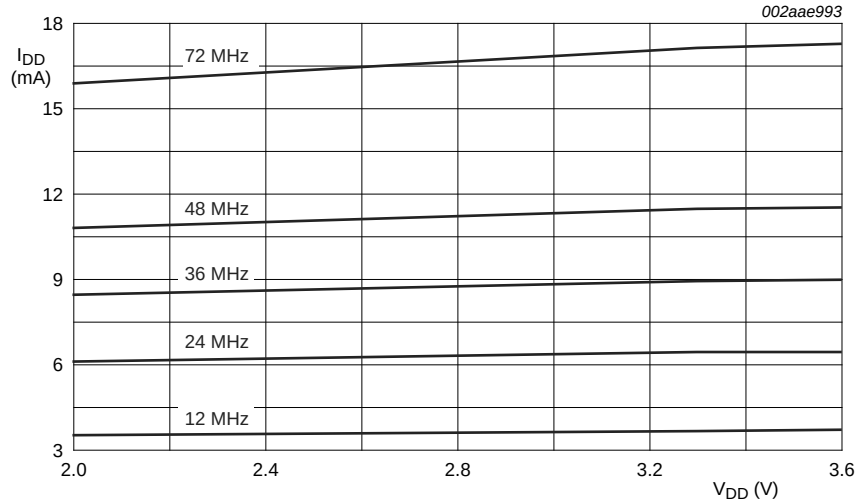
[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see *LPC13xx user manual*.

9.3 Power consumption for LPC1300 series

Remark: Applies to parts LPC1311/13/42/43 and all their packages.

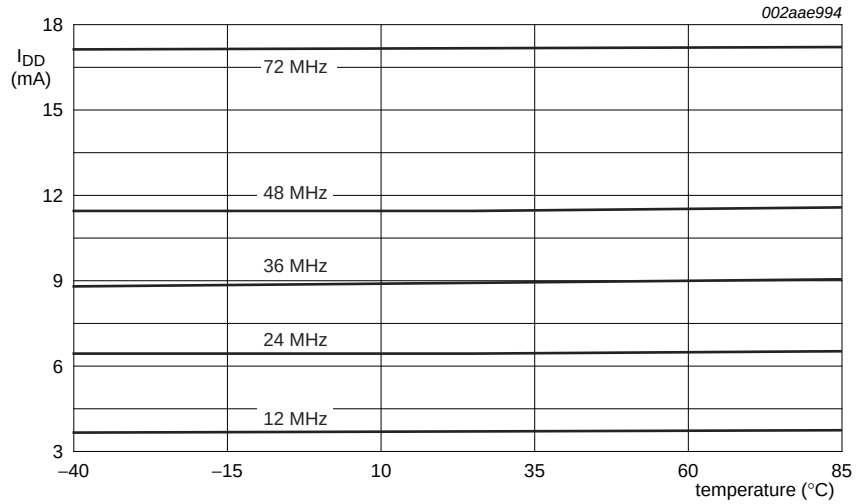
Power measurements in Active, Sleep, and Deep-sleep modes were performed under the following conditions (see *LPC13xx user manual*):

- Configure all pins as GPIO with pull-up resistor disabled in the IOCONFIG block.
- Configure GPIO pins as outputs using the GPIOnDIR registers.
- Write 0 to all GPIOnDATA registers to drive the outputs LOW.



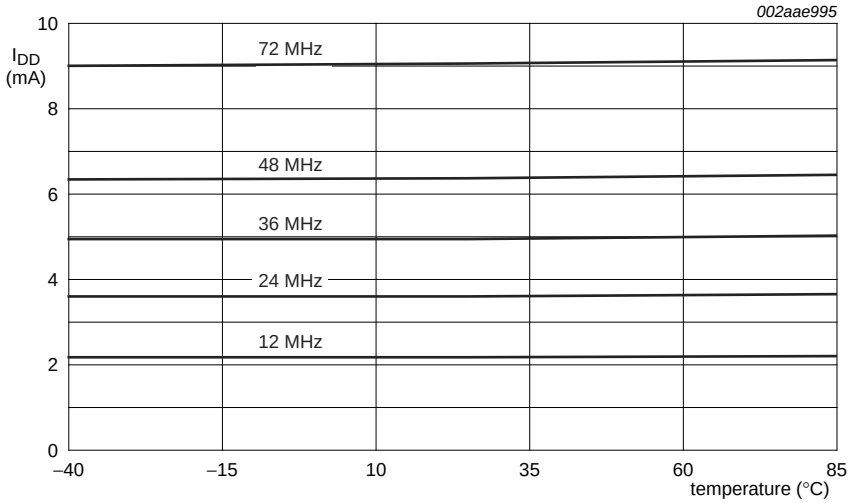
Conditions: T_{amb} = 25 °C; Active mode entered executing code `while(1){}` from flash; internal pull-up resistors disabled; system oscillator and system PLL enabled; IRC, BOD disabled; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; USB_DP and USB_DM pulled LOW externally (LPC1342/43).

Fig 9. Typical supply current versus regulator supply voltage V_{DD} in Active mode (LPC1311/13/42/43)



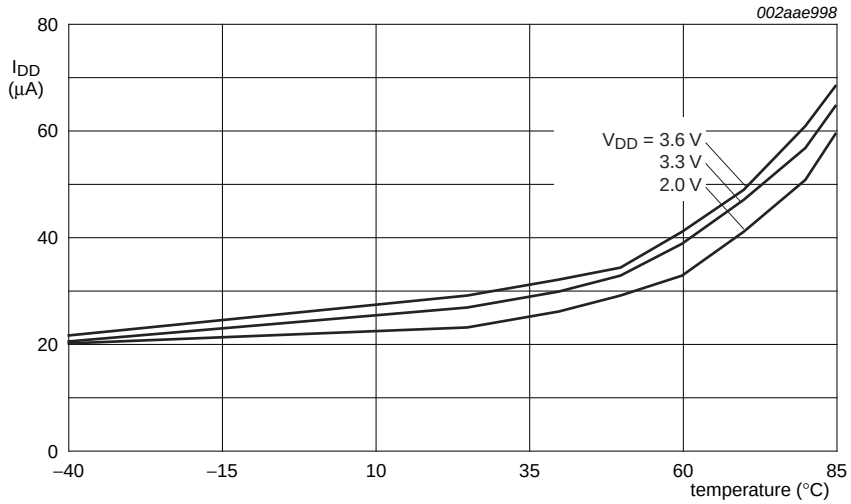
Conditions: V_{DD} = 3.3 V; Active mode entered executing code `while(1){}` from flash; internal pull-up resistors disabled; system oscillator and system PLL enabled; IRC, BOD disabled; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; USB_DP and USB_DM pulled LOW externally (LPC1342/43).

Fig 10. Typical supply current versus temperature in Active mode (LPC1311/13/42/43)



Conditions: V_{DD} = 3.3 V; Sleep mode entered from flash; internal pull-up resistors disabled; system oscillator and system PLL enabled; IRC, BOD disabled; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; USB_DP and USB_DM pulled LOW externally (LPC1342/43).

Fig 11. Typical supply current versus temperature in Sleep mode (LPC1311/13/42/43)



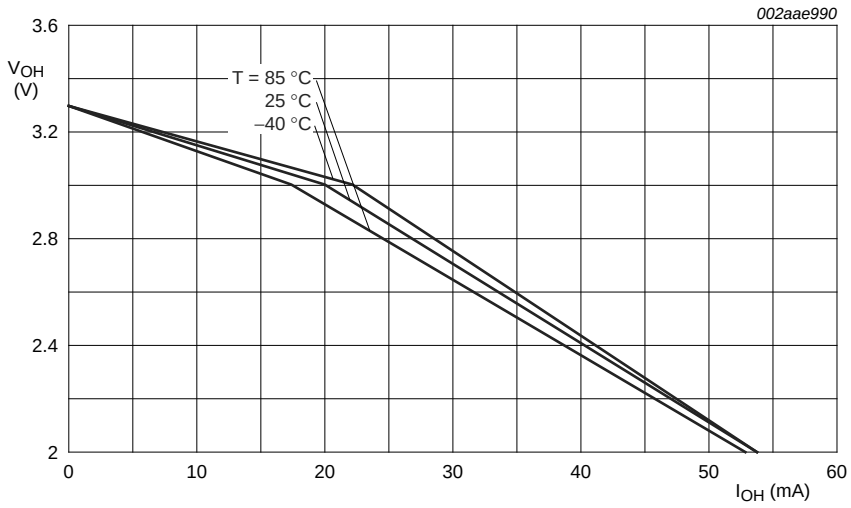
Conditions: BOD disabled; all oscillators and analog blocks turned off in the PDSLEEPCFG register; PDSLEEPCFG = 0x0000 0FFF; USB_DP and USB_DM pulled LOW externally (LPC1342/43).

Fig 12. Typical supply current versus temperature in Deep-sleep mode (analog blocks disabled; LPC1311/13/42/43)

Table 11. Power consumption for individual analog and digital blocks *…continued*

Peripheral	Typical supply current in mA				Notes
	n/a	12 MHz	48 MHz	72 MHz	
GPIO	-	0.21	0.80	1.17	GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register.
IOCONFIG	-	0.00	0.02	0.02	-
I2C	-	0.03	0.12	0.17	-
ROM	-	0.04	0.15	0.22	-
SSP0	-	0.11	0.41	0.60	-
SSP1	-	0.11	0.41	0.60	On LPC1313FBD48/01 only.
UART	-	0.20	0.76	1.11	-
WDT	-	0.01	0.05	0.08	Main clock selected as clock source for the WDT.
USB	-	-	3.91	-	Main clock selected as clock source for the USB. USB_DP and USB_DM pulled LOW externally.
USB	-	1.84	4.19	5.71	Dedicated USB PLL selected as clock source for the USB. USB_DP and USB_DM pulled LOW externally.

9.6 Electrical pin characteristics



Conditions: V_{DD} = 3.3 V; on pin PIO0_7.

Fig 19. High-drive output: Typical HIGH-level output voltage V_{OH} versus HIGH-level output current I_{OH}.

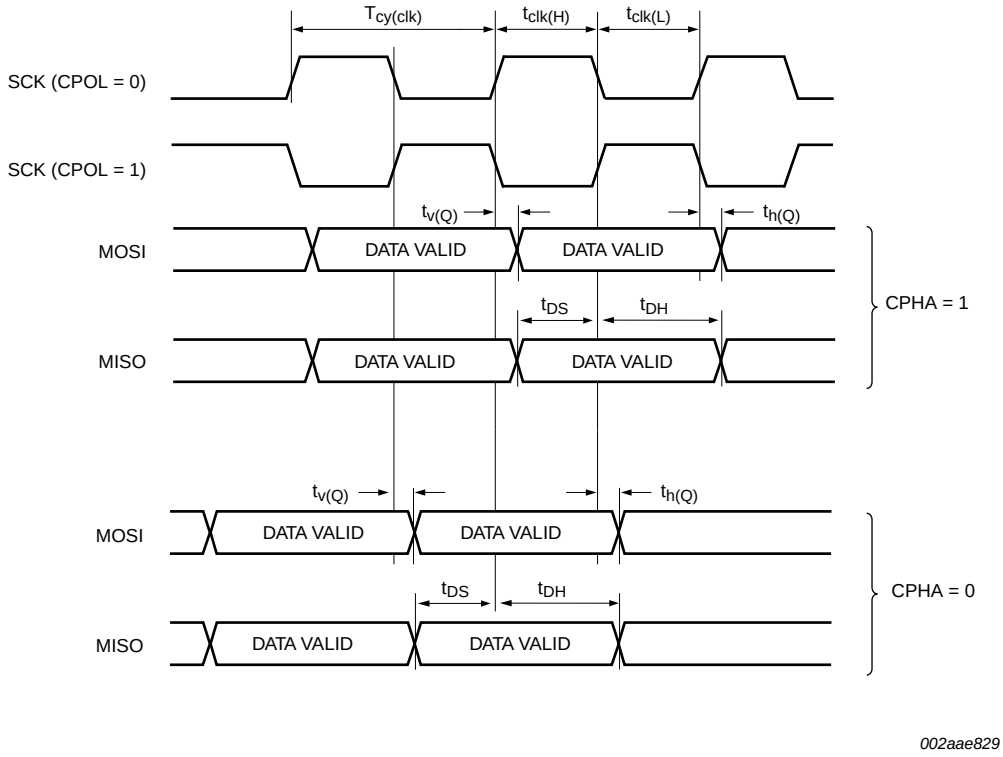


Fig 29. SSP master timing in SPI mode

11.5 Reset pad configuration

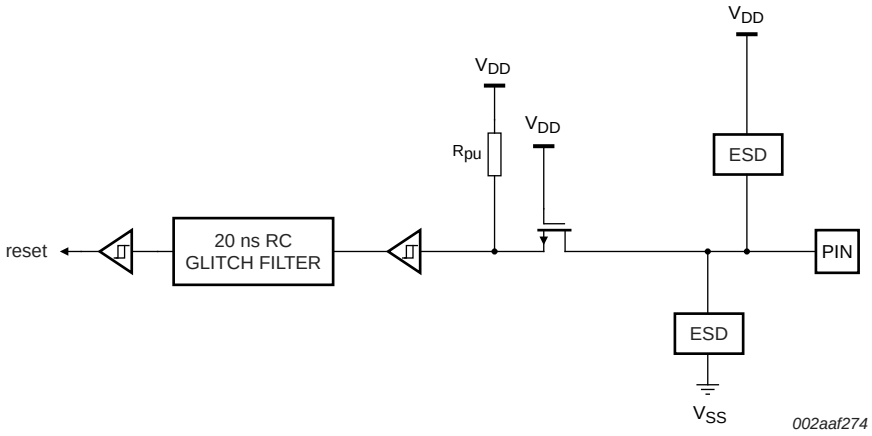


Fig 37. Reset pad configuration

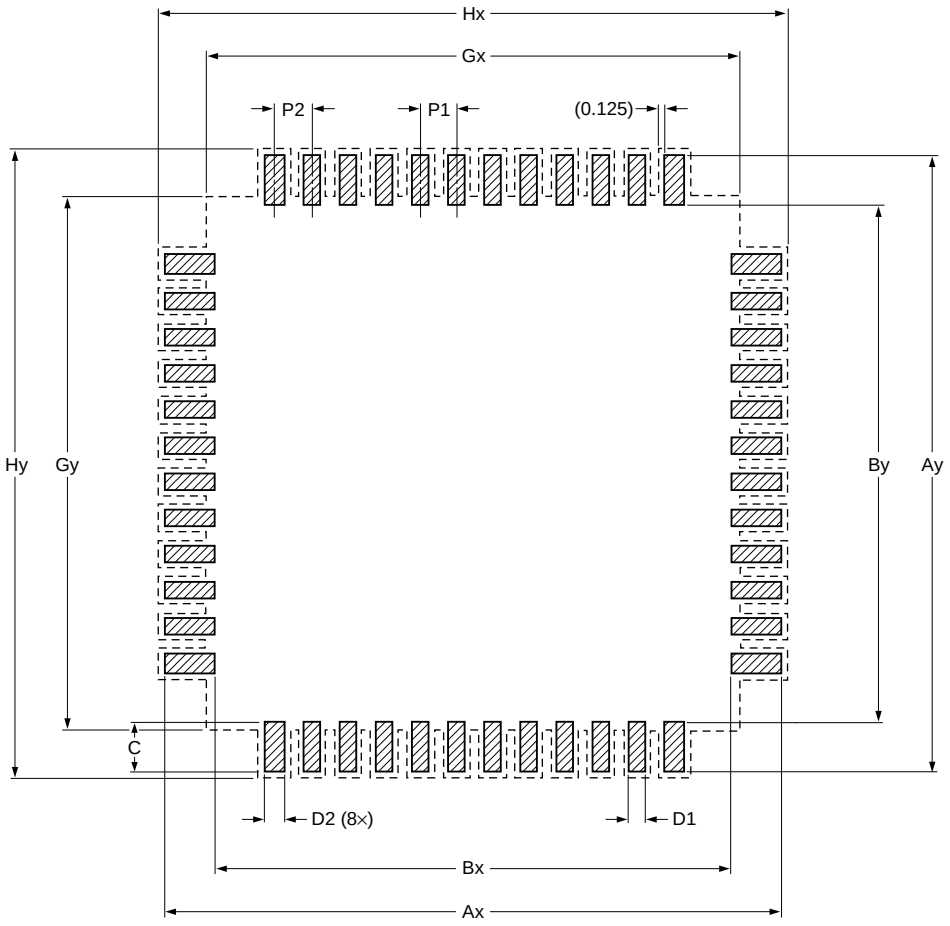
11.6 ADC usage notes

The following guidelines show how to increase the performance of the ADC in a noisy environment beyond the ADC specifications listed in Table 8:

- The ADC input trace must be short and as close as possible to the LPC1311/13/42/43 chip.
- The ADC input traces must be shielded from fast switching digital signals and noisy power supply lines.
- Because the ADC and the digital core share the same power supply, the power supply line must be adequately filtered.
- To improve the ADC performance in a very noisy environment, put the device in Sleep mode during the ADC conversion.

13. Soldering

Footprint information for reflow soldering of LQFP48 package **SOT313-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	10.350	10.350	7.350	7.350	1.500	0.280	0.500	7.500	7.500	10.650	10.650

sot313-2_fr

Fig 40. Reflow soldering of the LQFP48 package

14. Abbreviations

Table 24. Abbreviations

Acronym	Description
A/D	Analog-to-Digital
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
EOP	End Of Packet
ETM	Embedded Trace Macrocell
FIFO	First-In, First-Out
GPIO	General Purpose Input/Output
HID	Human Interface Device
I/O	Input/Output
LSB	Least Significant Bit
MSC	Mass Storage Class
PHY	Physical Layer
PLL	Phase-Locked Loop
SE0	Single Ended Zero
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
SSP	Synchronous Serial Port
SoF	Start-of-Frame
TCM	Tightly-Coupled Memory
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

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