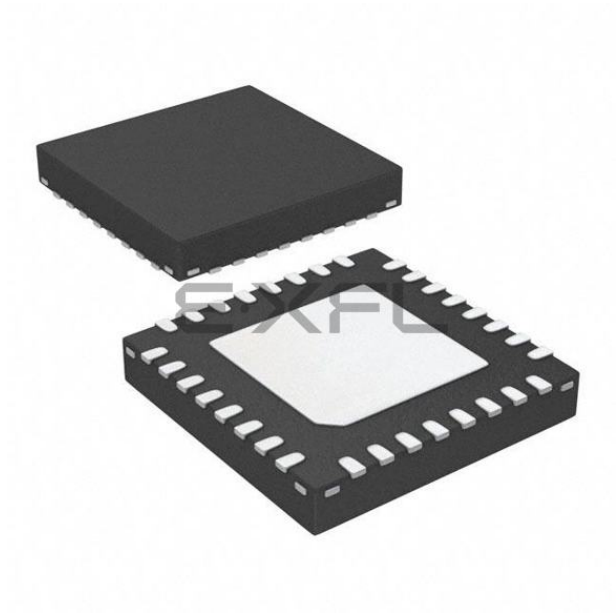

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

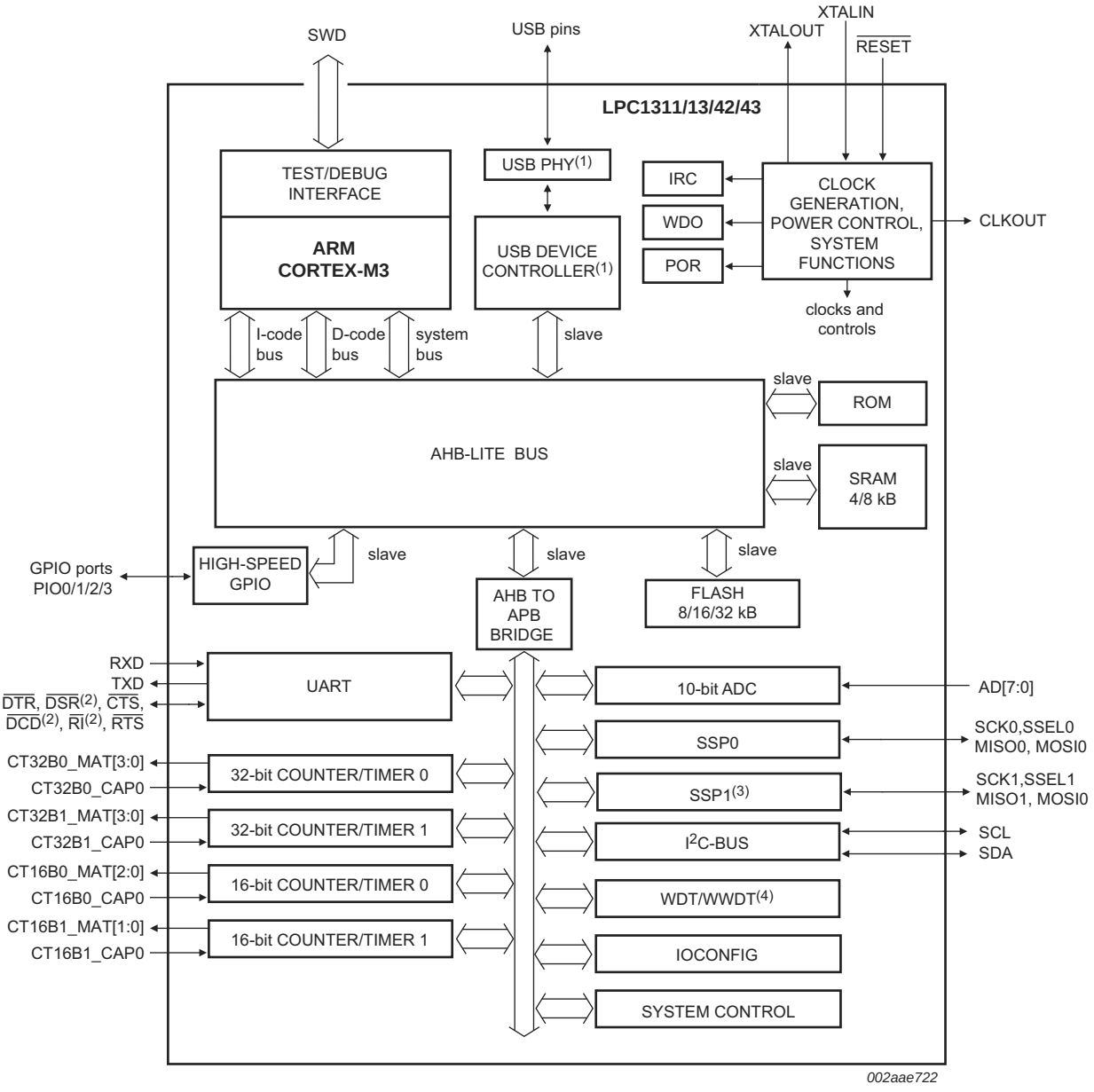
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	I²C, Microwire, SPI, SSI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	28
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VQFN Exposed Pad
Supplier Device Package	32-HVQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1313fhn33-551

Table 2. Ordering options for LPC1311/13/42/43 *…continued*

Type number	Flash	Total SRAM	USB	Power profiles	UART RS-485	I^2C/ Fast+	SSP	ADC channels	Pins	Package
LPC1342FHN33	16 kB	4 kB	Device	no	1	1	1	8	33	HVQFN33
LPC1342FBD48	16 kB	4 kB	Device	no	1	1	1	8	48	LQFP48
LPC1343FHN33	32 kB	8 kB	Device	no	1	1	1	8	33	HVQFN33
LPC1343FBD48	32 kB	8 kB	Device	no	1	1	1	8	48	LQFP48

5. Block diagram



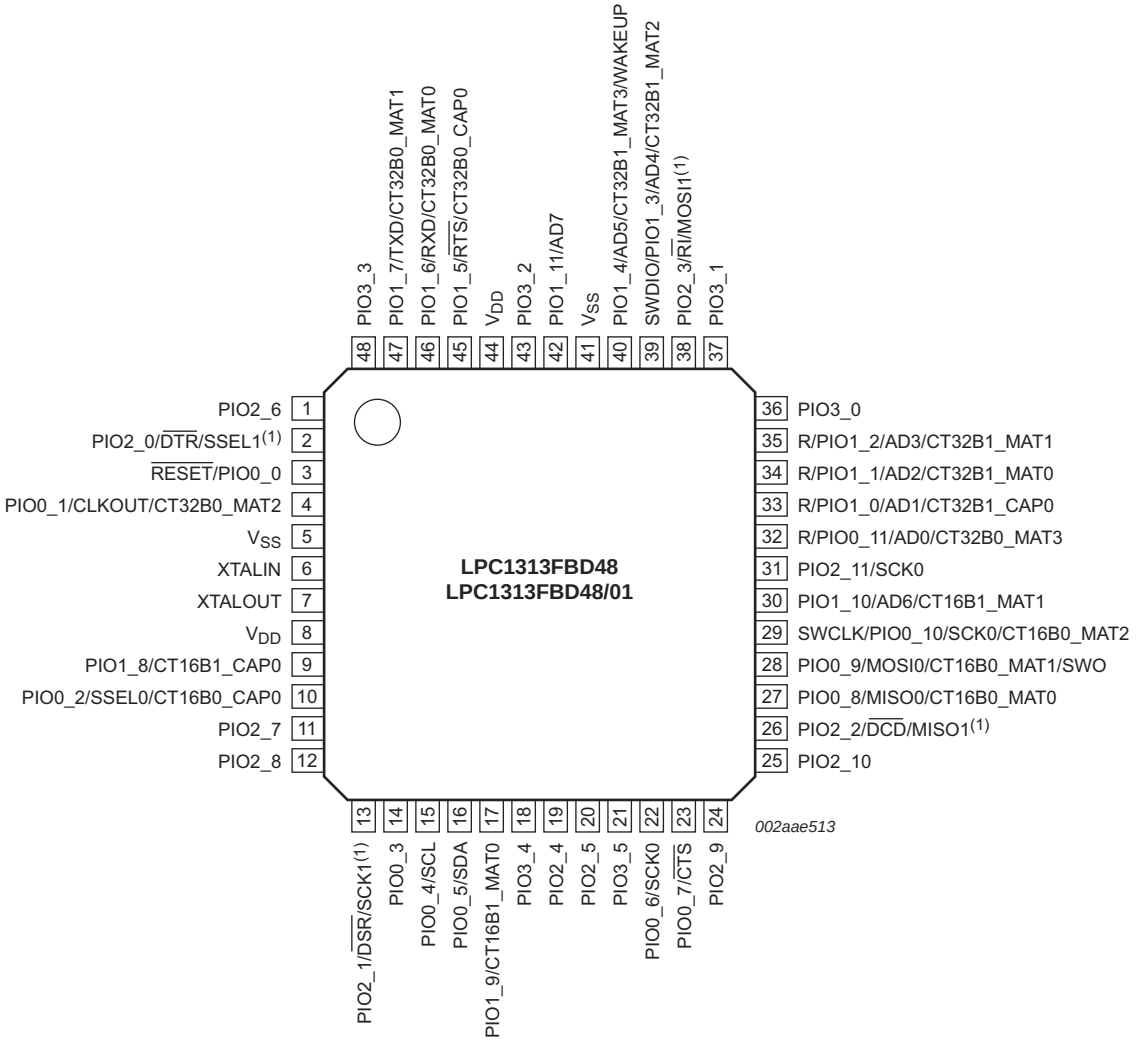
(1) LPC1342/43 only.

(2) LQFP48 package only.

(3) On LPC1313FBD48/01 only.

(4) Windowed WatchDog Timer (WWDT) on LPC1311/01 and LPC1313/01 only.

Fig 1. Block diagram



(1) SSP1 or UART function on LPC1313FBD48/01 only.

Fig 4. LPC1313 LQFP48 package

Table 3. LPC1313/42/43 LQFP48 pin description table *…continued*

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
PIO2_10	25[3]	yes	I/O	I; PU	**PIO2_10 —** General purpose digital input/output pin.
PIO2_11/SCK0	31[3]	yes	I/O	I; PU	**PIO2_11 —** General purpose digital input/output pin.
			I/O	-	**SCK0 —** Serial clock for SSP0.
PIO3_0/$\overline{\text{DTR}}$	36[3]	yes	I/O	I; PU	**PIO3_0 —** General purpose digital input/output pin.
			O	-	**$\overline{\text{DTR}}$ —** Data Terminal Ready output for UART (LPC1311/01 and LPC1313/01 only).
PIO3_1/$\overline{\text{DSR}}$	37[3]	yes	I/O	I; PU	**PIO3_1 —** General purpose digital input/output pin.
			I	-	**$\overline{\text{DSR}}$ —** Data Set Ready input for UART (LPC1311/01 and LPC1313/01 only).
PIO3_2/$\overline{\text{DCD}}$	43[3]	yes	I/O	I; PU	**PIO3_2 —** General purpose digital input/output pin.
			I	-	**$\overline{\text{DCD}}$ —** Data Carrier Detect input for UART (LPC1311/01 and LPC1313/01 only).
PIO3_3/$\overline{\text{RI}}$	48[3]	yes	I/O	I; PU	**PIO3_3 —** General purpose digital input/output pin.
			I	-	**$\overline{\text{RI}}$ —** Ring Indicator input for UART (LPC1311/01 and LPC1313/01 only).
PIO3_4	18[3]	no	I/O	I; PU	**PIO3_4 —** General purpose digital input/output pin (LPC1313 only).
PIO3_5	21[3]	no	I/O	I; PU	**PIO3_5 —** General purpose digital input/output pin (LPC1313 only).
USB_DM	19[6]	no	I/O	F	**USB_DM —** USB bidirectional D− line (LPC1342/43 only).
USB_DP	20[6]	no	I/O	F	**USB_DP —** USB bidirectional D+ line (LPC1342/43 only).
V_{DD}	8; 44	-	I	-	3.3 V supply voltage to the internal regulator, the external rail, and the ADC. Also used as the ADC reference voltage.
XTALIN	6[7]	-	I	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	7[7]	-	O	-	Output from the oscillator amplifier.
V_{SS}	5; 41	-	I	-	Ground.

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled (for V_{DD} = 3.3 V, pin is pulled up to 2.6 V for parts LPC1311/13/42/43 and pulled up to 3.3 V for parts LPC1311/01 and LPC1313/01); IA = inactive, no pull-up/down enabled; F = floating; floating pins, if not used, should be tied to ground or power to minimize power consumption.

[2] 5 V tolerant pad. See Figure 37 for pad characteristics. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 36).

[4] I^2C-bus pads compliant with the I^2C-bus specification for I^2C standard mode and I^2C Fast-mode Plus.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see Figure 36).

[6] Pad provides USB functions. It is designed in accordance with the USB specification, revision 2.0 (Full-speed and Low-speed mode only). This pad is not 5 V tolerant.

[7] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

7.14 General purpose external event counter/timers

The LPC1311/13/42/43 includes two 32-bit counter/timers and two 16-bit counter/timers. The counter/timer is designed to count cycles of the system derived clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. Each counter/timer also includes one capture input to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.14.1 Features

- A 32-bit/16-bit counter/timer with a programmable 32-bit/16-bit prescaler.
- Counter or timer operation.
- One capture channel per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt.
- Four match registers per timer that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

7.15 System tick timer

The ARM Cortex-M3 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a fixed time interval, normally set to 10 ms.

7.16 Watchdog timer

Remark: The standard Watchdog timer is available on parts LPC1311/13/42/43.

The purpose of the watchdog is to reset the microcontroller within a selectable time period. When enabled, the watchdog will generate a system reset if the user program fails to ‘feed’ (or reload) the watchdog within a predetermined amount of time.

7.16.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect/incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.

- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the Internal RC oscillator (IRC), the watchdog oscillator, or the main clock. This gives a wide range of potential timing choices of watchdog operation under different power reduction conditions. It also provides the ability to run the WDT from an entirely internal source that is not dependent on an external crystal and its associated components and wiring for increased reliability.

7.17 Windowed WatchDog Timer (WWDT)

Remark: The windowed watchdog timer is available on parts LPC1311/01 and LPC1313/01.

The purpose of the watchdog is to reset the controller if software fails to periodically service it within a programmable time window.

7.17.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the IRC or the dedicated watchdog oscillator (WDO). This gives a wide range of potential timing choices of watchdog operation under different power conditions.

7.18 Clocking and power control

7.18.1 Integrated oscillators

The LPC1311/13/42/43 include three independent oscillators. These are the system oscillator, the Internal RC oscillator (IRC), and the watchdog oscillator. Each oscillator can be used for more than one purpose as required in a particular application.

Following reset, the LPC1311/13/42/43 will operate from the internal RC oscillator until switched by software. This allows systems to operate without any external crystal and the bootloader code to operate at a known frequency.

See Figure 7 for an overview of the LPC1311/13/42/43 clock generation.

Upon power-up, any chip reset, or wake-up from Deep power-down mode, the LPC1311/13/42/43 use the IRC as the clock source. Software may later switch to one of the other available clock sources.

7.18.1.2 System oscillator

The system oscillator can be used as the clock source for the CPU, with or without using the PLL. On the LPC1342/43, the system oscillator must be used to provide the clock source to USB.

The system oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

7.18.1.3 Watchdog oscillator

The watchdog oscillator can be used as a clock source that directly drives the CPU, the watchdog timer, or the CLKOUT pin. The watchdog oscillator nominal frequency is programmable between 7.8 kHz and 1.7 MHz. The frequency spread over processing and temperature is ±40 % (see also Table 16).

7.18.2 System PLL and USB PLL

The LPC1342/43 contain a system PLL and a dedicated PLL for generating the 48 MHz USB clock. The LPC131x contain the system PLL only. The system and USB PLLs are identical.

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. The PLL output frequency must be lower than 100 MHz. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 µs.

7.18.3 Clock output

The LPC1311/13/42/43 features a clock output function that routes the IRC oscillator, the system oscillator, the watchdog oscillator, or the main clock to an output pin.

7.18.4 Wake-up process

The LPC1311/13/42/43 begin operation at power-up and when awakened from Deep power-down mode by using the 12 MHz IRC oscillator as the clock source. This allows chip operation to resume quickly. If the main oscillator or the PLL is needed by the application, software will need to enable these features and wait for them to stabilize before they are used as a clock source.

7.18.5.4 Deep power-down mode

In Deep power-down mode, power is shut off to the entire chip with the exception of the WAKEUP pin. The LPC1311/13/42/43 can wake up from Deep power-down mode via the WAKEUP pin.

A LOW-going pulse as short as 50 ns wakes up the part from Deep power-down mode.

When entering Deep power-down mode, an external pull-up resistor is required on the WAKEUP pin to hold it HIGH. The RESET pin must also be held HIGH to prevent it from floating while in Deep power-down mode.

7.19 System control

7.19.1 Start logic

The start logic connects external pins to corresponding interrupts in the NVIC. Each pin shown in Table 3 and Table 4 as input to the start logic has an individual interrupt in the NVIC interrupt vector table. The start logic pins can serve as external interrupt pins when the chip is running. In addition, an input signal on the start logic pins can wake up the chip from Deep-sleep mode when all clocks are shut down.

The start logic must be configured in the system configuration block and in the NVIC before being used.

7.19.2 Reset

Reset has four sources on the LPC1311/13/42/43: the RESET pin, the Watchdog reset, power-on reset (POR), and the Brown-Out Detection (BOD) circuit. The RESET pin is a Schmitt trigger input pin. Assertion of chip reset by any source, once the operating voltage attains a usable level, starts the IRC and initializes the flash controller.

When the internal reset is removed, the processor begins executing at address 0, which is initially the reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

7.19.3 Brownout detection

The LPC1311/13/42/43 includes four levels for monitoring the voltage on the V_{DD} pin. If this voltage falls below one of the four selected levels, the BOD asserts an interrupt signal to the NVIC. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC in order to cause a CPU interrupt; if not, software can monitor the signal by reading a dedicated status register. An additional threshold level can be selected to cause a forced reset of the chip.

7.19.4 Code security (Code Read Protection - CRP)

This feature of the LPC1311/13/42/43 allows user to enable different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. In-Application Programming (IAP) commands are not affected by the CRP.

In addition, ISP entry via the PIO0_1 pin can be disabled without enabling CRP (NO_ISP mode). For details see the *LPC13xx user manual*.

Table 7. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{OH}	HIGH-level output voltage	driven; for low-/full-speed; R_L of 15 kΩ to GND	[17]	2.8	-	3.5	V
C_{trans}	transceiver capacitance	pin to GND	[17]	-	-	20	pF
Z_{DRV}	driver output impedance for driver which is not high-speed capable	with 33 Ω series resistor; steady state drive	[18][17]	36	-	44.1	Ω

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] For LPC1342 and LPC1343 only: For USB operation 3.0 V ≤ V_{DD} ≤ 3.6 V. Guaranteed by design.

[3] IRC enabled; system oscillator disabled; system PLL disabled.

[4] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.

[5] BOD disabled.

[6] All peripherals disabled in the SYSAHBCLKCTRL register. Peripheral clocks to UART, SSP, trace clock, and SysTick timer disabled in the syscon block.

[7] For LPC1342/43: USB_DP and USB_DM pulled LOW externally.

[8] IRC disabled; system oscillator enabled; system PLL enabled.

[9] All oscillators and analog blocks turned off in the PDSLEEPCFG register; PDSLEEPCFG = 0x0000 0FFF.

[10] WAKEUP pin pulled HIGH externally. An external pull-up resistor is required on the $\overline{\text{RESET}}$ pin for the Deep power-down mode.

[11] Low-current mode PWR_LOW_CURRENT selected when running the set_power routine in the power profiles.

[12] Including voltage on outputs in 3-state mode.

[13] V_{DD} supply voltage must be present.

[14] 3-state outputs go into 3-state mode in Deep power-down mode.

[15] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[16] To V_{SS}.

[17] 3.0 V ≤ V_{DD} ≤ 3.6 V.

[18] Includes external resistors of 33 Ω ± 1 % on USB_DP and USB_DM.

Table 8. ADC static characteristics
T_{amb} = −40 °C to +85 °C unless otherwise specified; ADC frequency 4.5 MHz, V_{DD} = 2.5 V to 3.6 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IA}	analog input voltage			0	-	V_{DD}	V
C_{ia}	analog input capacitance			-	-	1	pF
E_D	differential linearity error		[1][2]	-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity		[3]	-	-	±1.5	LSB
E_O	offset error		[4]	-	-	±3.5	LSB
E_G	gain error		[5]	-	-	0.6	%
E_T	absolute error		[6]	-	-	±4	LSB
R_{vsi}	voltage source interface resistance			-	-	40	kΩ
R_i	input resistance		[7][8]	-	-	2.5	MΩ

[1] The ADC is monotonic, there are no missing codes.

[2] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 8.

9.2 BOD static characteristics for LPC1300L series (LPC1311/01 and LPC1313/01)

Remark: Applies to parts LPC1311/01 and LPC1313/01 and all packages.

Table 10. BOD static characteristics[1]
T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 0				
		assertion	-	1.65	-	V
		de-assertion	-	1.80	-	V
		interrupt level 1				
		assertion	-	2.22	-	V
		de-assertion	-	2.35	-	V
		interrupt level 2				
		assertion	-	2.52	-	V
		de-assertion	-	2.66	-	V
		interrupt level 3				
		assertion	-	2.80	-	V
		de-assertion	-	2.90	-	V
		reset level 0				
		assertion	-	1.46	-	V
		de-assertion	-	1.63	-	V
		reset level 1				
		assertion	-	2.06	-	V
		de-assertion	-	2.15	-	V
		reset level 2				
		assertion	-	2.35	-	V
		de-assertion	-	2.43	-	V
		reset level 3				
		assertion	-	2.63	-	V
		de-assertion	-	2.71	-	V

[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see *LPC13xx user manual*.

9.3 Power consumption for LPC1300 series

Remark: Applies to parts LPC1311/13/42/43 and all their packages.

Power measurements in Active, Sleep, and Deep-sleep modes were performed under the following conditions (see *LPC13xx user manual*):

- Configure all pins as GPIO with pull-up resistor disabled in the IOCONFIG block.
- Configure GPIO pins as outputs using the GPIOnDIR registers.
- Write 0 to all GPIOnDATA registers to drive the outputs LOW.

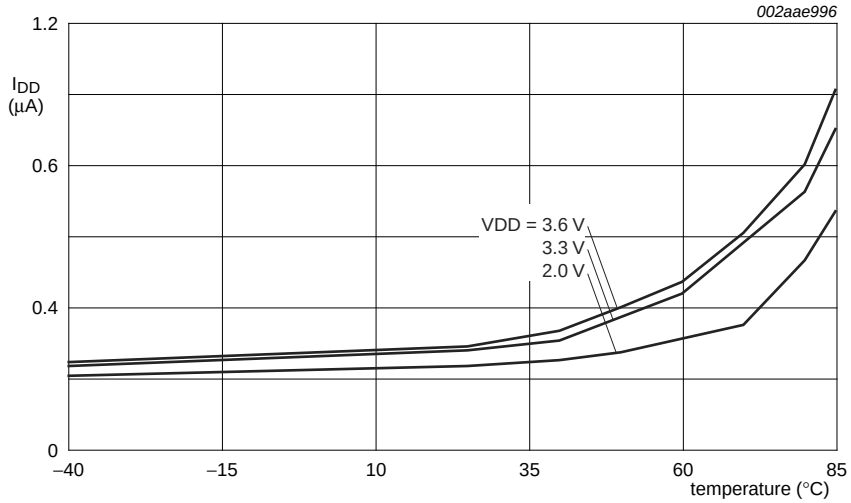


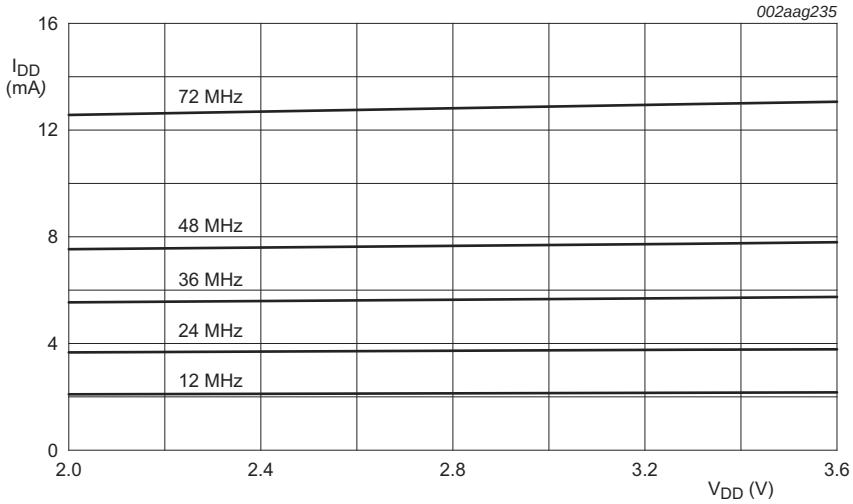
Fig 13. Typical supply current versus temperature in Deep power-down mode (LPC1311/13/42/43)

9.4 Power consumption for LPC1300L series (LPC1311/01 and LPC1313/01)

Remark: Applies to parts LPC1311/01 and LPC1313/01 and all their packages.

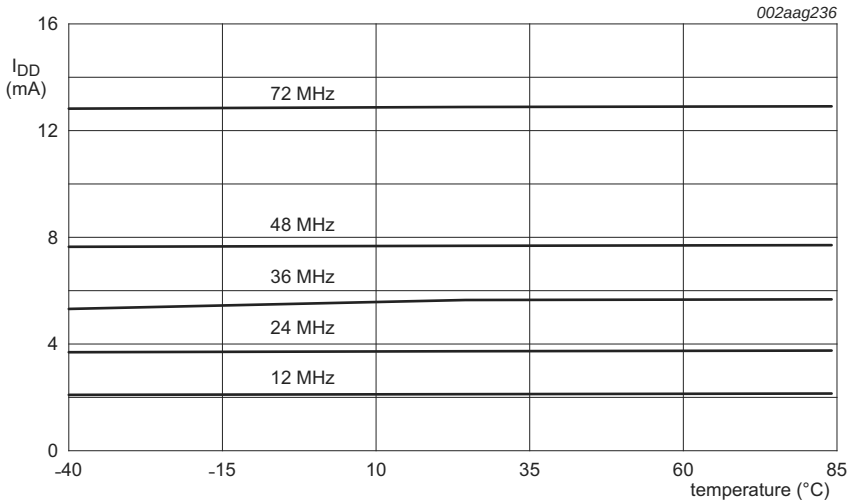
Power measurements in Active, Sleep, and Deep-sleep modes were performed under the following conditions (see *LPC13xx user manual*):

- Configure all pins as GPIO with pull-up resistor disabled in the IOCONFIG block.
- Configure GPIO pins as outputs using the GPIOnDIR registers.
- Write 0 to all GPIOnDATA registers to drive the outputs LOW.



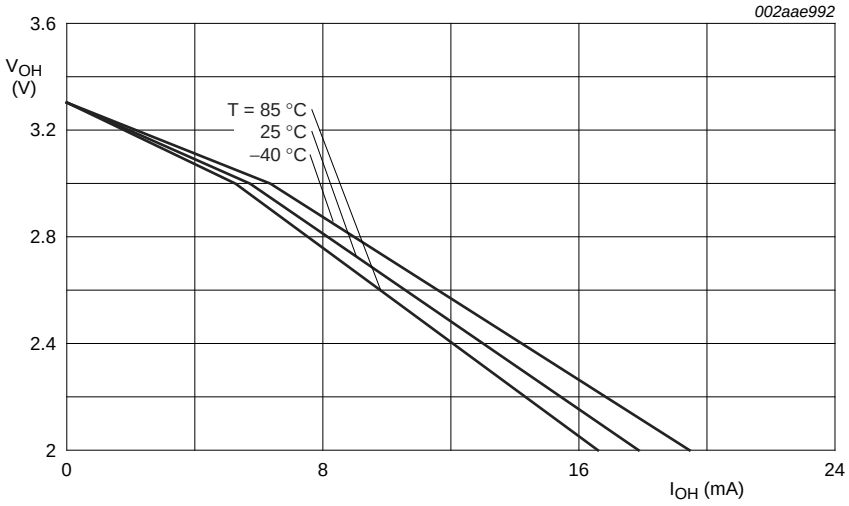
Conditions: T_{amb} = 25 °C; Active mode entered executing code `while(1){}` from flash; internal pull-up resistors disabled; system oscillator and system PLL enabled; IRC, BOD disabled; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; low-current mode.

Fig 14. Typical supply current versus regulator supply voltage V_{DD} in Active mode (LPC1311/01 and LPC1313/01)



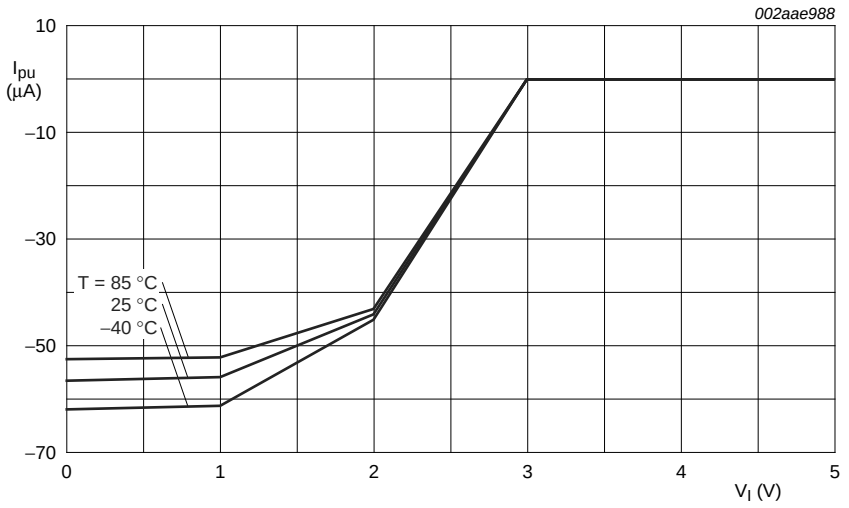
Conditions: V_{DD} = 3.3 V; Active mode entered executing code `while(1){}` from flash; internal pull-up resistors disabled; system oscillator and system PLL enabled; IRC, BOD disabled; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; low-current mode.

Fig 15. Typical supply current versus temperature in Active mode (LPC1311/01 and LPC1313/01)



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 22. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 23. Typical pull-up current I_{pu} versus input voltage V_i

10.3 External clock

Table 14. Dynamic characteristic: external clock
T_{amb} = –40 °C to +85 °C; V_{DD} over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
f_{osc}	oscillator frequency		1	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

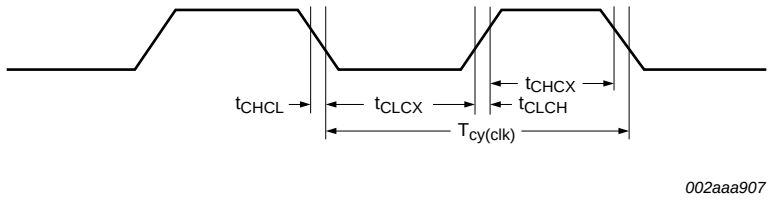
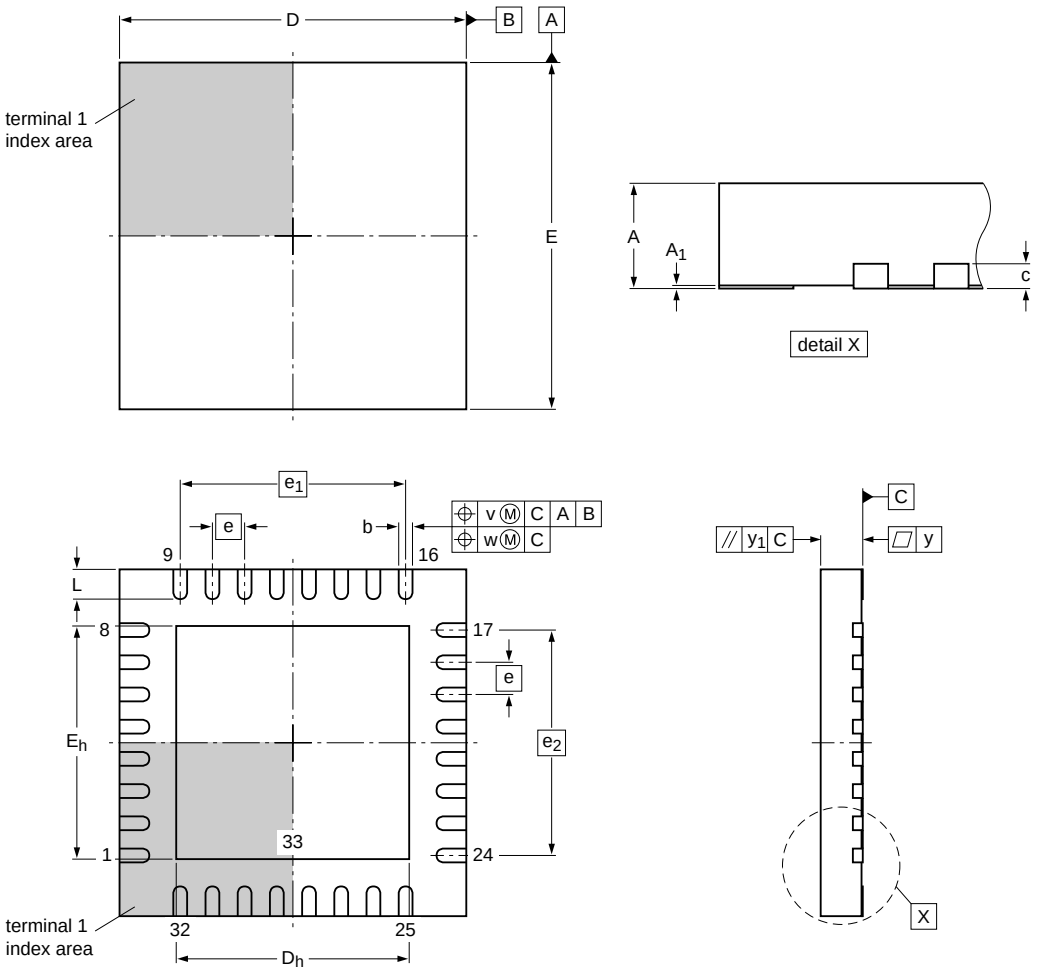


Fig 26. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

HVQFN33: plastic thermal enhanced very thin quad flat package; no leads; 33 terminals; body 7 x 7 x 0.85 mm



Dimensions

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
	max	1.00	0.05	0.35		7.1	4.85	7.1	4.85				0.75				
mm	nom	0.85	0.02	0.28	0.2	7.0	4.70	7.0	4.70	0.65	4.55	4.55	0.60	0.1	0.05	0.08	0.1
	min	0.80	0.00	0.23		6.9	4.55	6.9	4.55				0.45				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

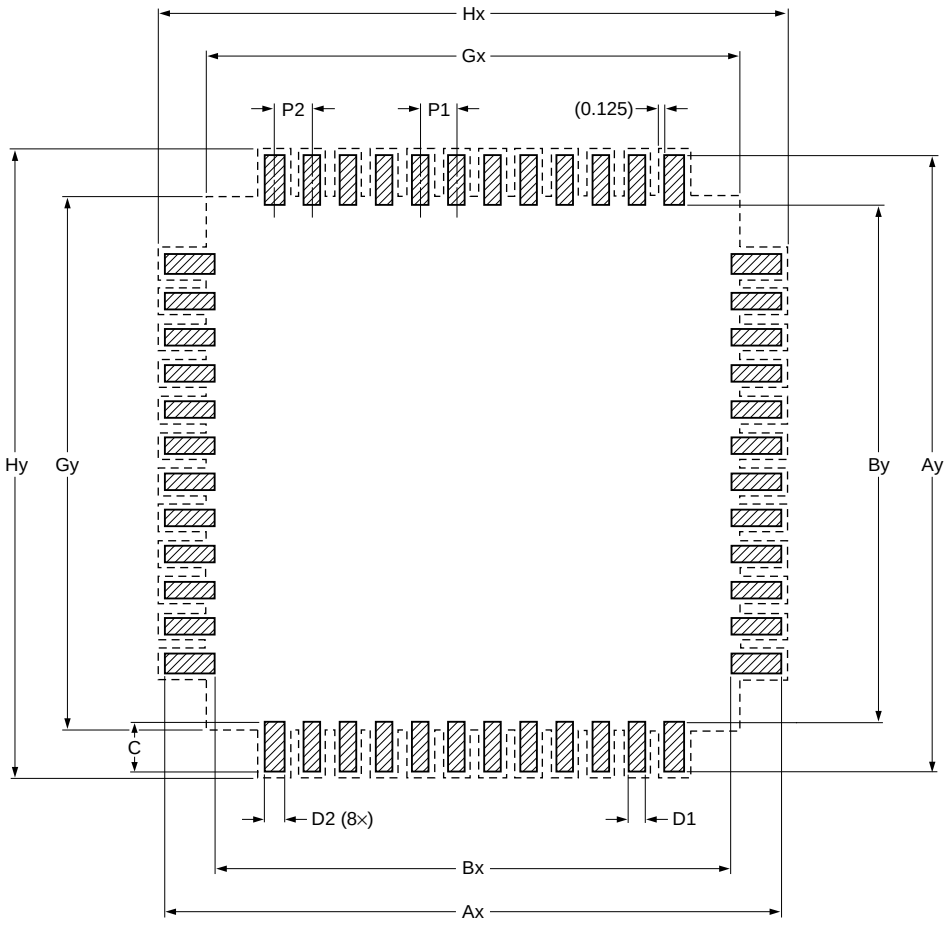
hvqfn33_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
		- - -				~~09-03-17~~ 09-03-23

Fig 39. Package outline (HVQFN33)

13. Soldering

Footprint information for reflow soldering of LQFP48 package **SOT313-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	10.350	10.350	7.350	7.350	1.500	0.280	0.500	7.500	7.500	10.650	10.650

sot313-2_fr

Fig 40. Reflow soldering of the LQFP48 package

Footprint information for reflow soldering of HVQFN33 package

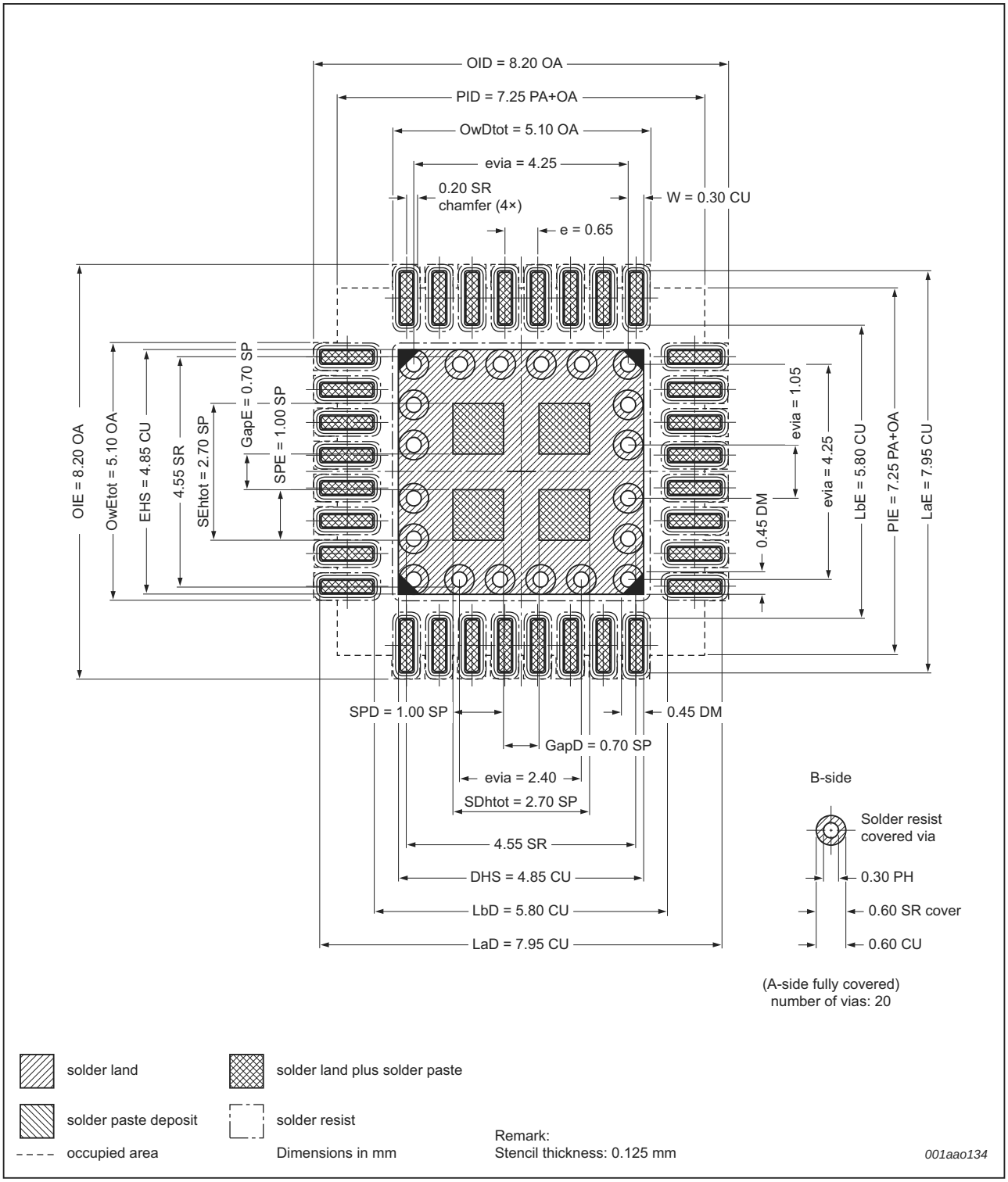


Fig 41. Reflow soldering of the HVQFN33 package

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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For sales office addresses, please send an email to: **salesaddresses@nxp.com**

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