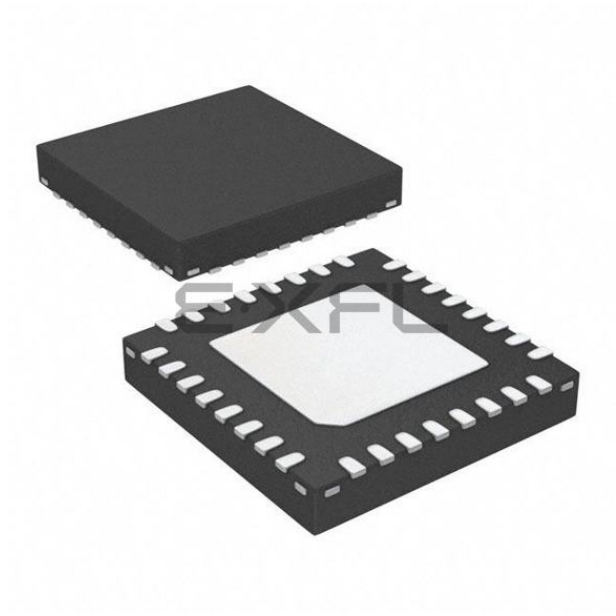

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What is "Embedded - Microcontrollers"?

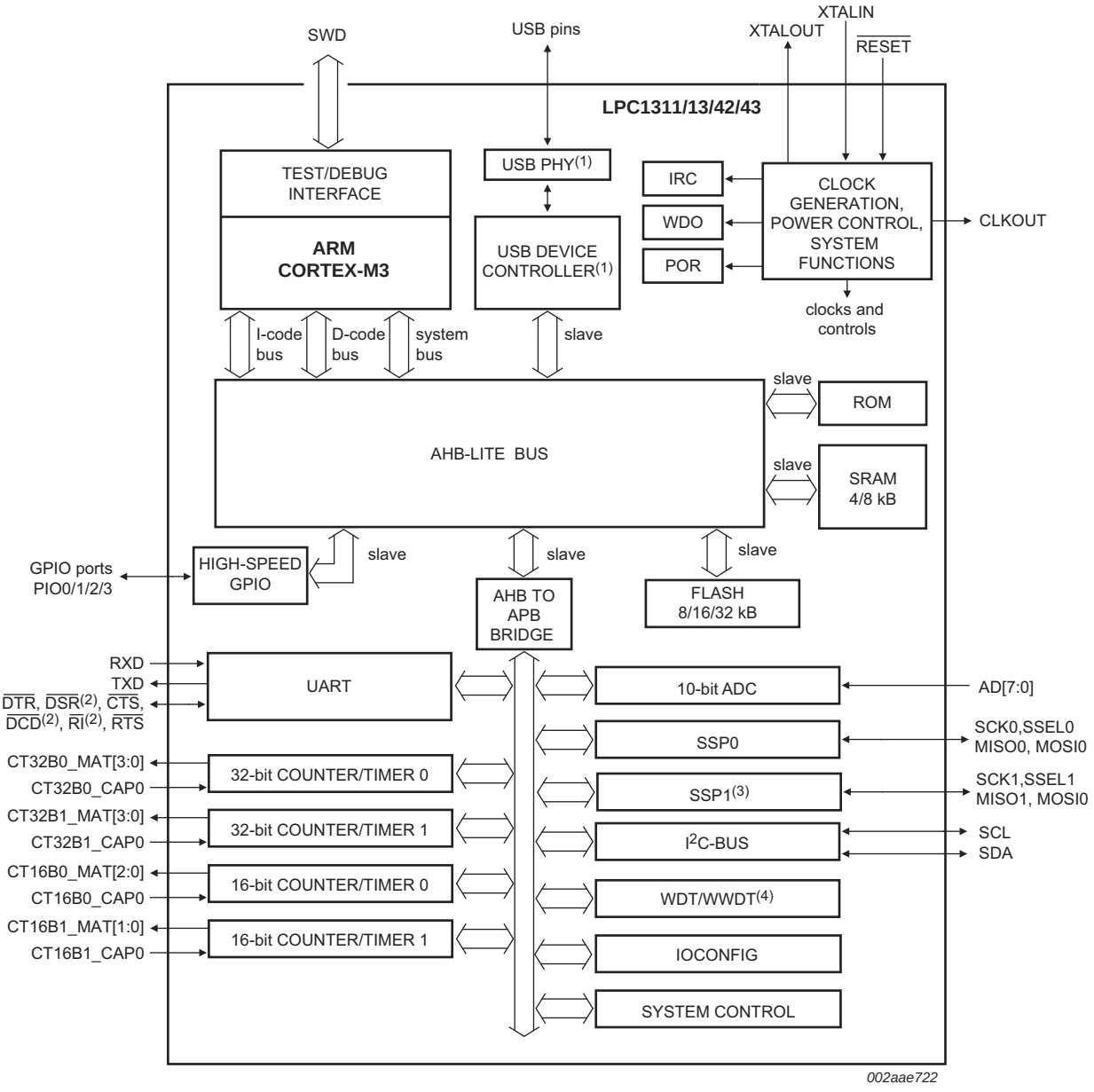
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	28
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VQFN Exposed Pad
Supplier Device Package	32-HVQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1342fhn33-518

- Serial interfaces:
  - USB 2.0 full-speed device controller with on-chip PHY for device (LPC1342/43 only).
  - UART with fractional baud rate generation, modem, internal FIFO, and RS-485/EIA-485 support.
  - SSP controller with FIFO and multi-protocol capabilities.
  - Additional SSP controller on LPC1313FBD48/01.
  - I^2C-bus interface supporting full I^2C-bus specification and Fast-mode Plus with a data rate of 1 Mbit/s with multiple address recognition and monitor mode.
- Other peripherals:
  - Up to 42 General Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors.
  - Four general purpose counter/timers with a total of four capture inputs and 13 match outputs.
  - Programmable WatchDog Timer (WDT).
  - Programmable Windowed Watchdog Timer (WWDT) on LPC1311/01 and LPC1313/01.
  - System tick timer.
- Serial Wire Debug and Serial Wire Trace port.
- High-current output driver (20 mA) on one pin.
- High-current sink drivers (20 mA) on two I^2C-bus pins in Fast-mode Plus.
- Integrated PMU (Power Management Unit) to minimize power consumption during Sleep, Deep-sleep, and Deep power-down modes.
- Power profiles residing in boot ROM allowing to optimize performance and minimize power consumption for any given application through one simple function call. (LPC1300L series, on LPC1311/01 and LPC1313/01 only.)
- Three reduced power modes: Sleep, Deep-sleep, and Deep power-down.
- Single power supply (2.0 V to 3.6 V).
- 10-bit ADC with input multiplexing among 8 pins.
- GPIO pins can be used as edge and level sensitive interrupt sources.
- Clock output function with divider that can reflect the system oscillator clock, IRC clock, CPU clock, or the watchdog clock.
- Processor wake-up from Deep-sleep mode via a dedicated start logic using up to 40 of the functional pins.
- Brownout detect with four separate thresholds for interrupt and one threshold for forced reset (four thresholds for forced reset on the LPC1311/01 and LPC1313/01 parts).
- Power-On Reset (POR).
- Integrated oscillator with an operating range of 1 MHz to 25 MHz.
- 12 MHz internal RC oscillator trimmed to 1 % accuracy over the entire temperature and voltage range that can optionally be used as a system clock.
- Programmable watchdog oscillator with a frequency range of 7.8 kHz to 1.8 MHz.
- System PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the system oscillator or the internal RC oscillator.
- For USB (LPC1342/43), a second, dedicated PLL is provided.
- Code Read Protection (CRP) with different security levels.

5. Block diagram



(1) LPC1342/43 only.

(2) LQFP48 package only.

(3) On LPC1313FBD48/01 only.

(4) Windowed WatchDog Timer (WWDT) on LPC1311/01 and LPC1313/01 only.

Fig 1. Block diagram

6. Pinning information

6.1 Pinning

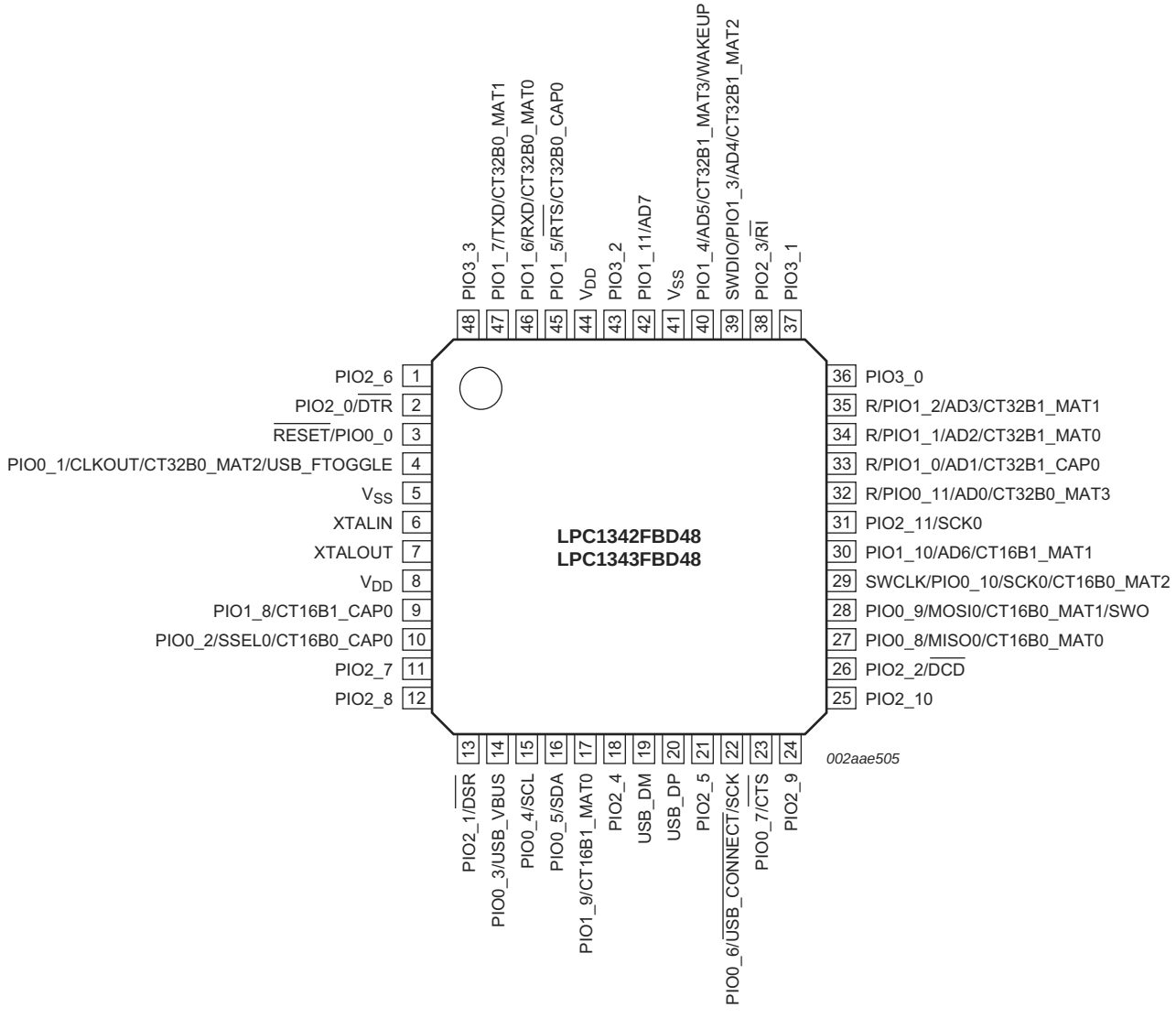


Fig 2. LPC1342/43 LQFP48 package

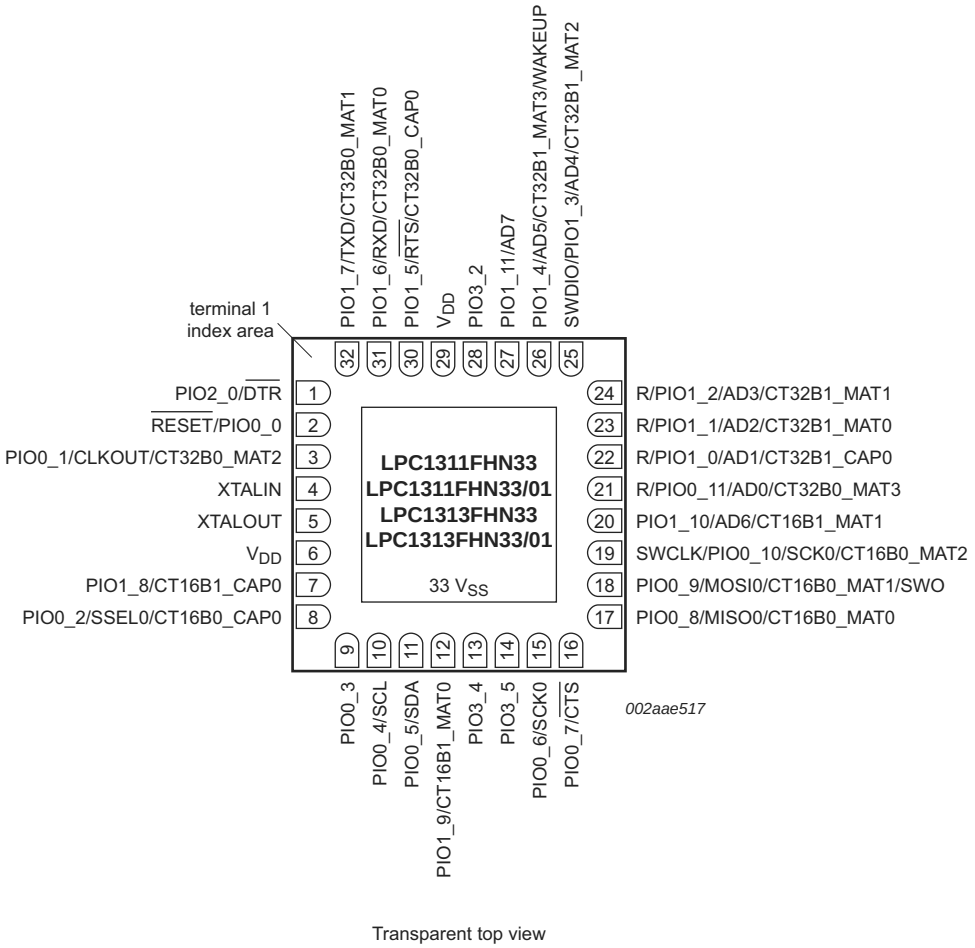


Fig 5. LPC1311/13 HVQFN33 package

7. Functional description

7.1 Architectural overview

The ARM Cortex-M3 includes three AHB-Lite buses: the system bus, the I-code bus, and the D-code bus (see Figure 1). The I-code and D-code core buses are faster than the system bus and are used similarly to TCM interfaces: one bus dedicated for instruction fetch (I-code) and one bus for data access (D-code). The use of two core buses allows for simultaneous operations if concurrent operations target different devices.

7.2 ARM Cortex-M3 processor

The ARM Cortex-M3 is a general purpose, 32-bit microprocessor, which offers high performance and very low power consumption. The ARM Cortex-M3 offers many new features, including a Thumb-2 instruction set, low interrupt latency, hardware multiply and divide, interruptible/continuable multiple load and store instructions, automatic state save and restore for interrupts, tightly integrated interrupt controller, and multiple core buses capable of simultaneous accesses.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM Cortex-M3 processor is described in detail in the *Cortex-M3 Technical Reference Manual* which is available on the official ARM website.

7.3 On-chip flash program memory

The LPC1311/13/42/43 contain 32 kB (LPC1313 and LPC1343), 16 kB (LPC1342), or 8 kB (LPC1311) of on-chip flash memory.

7.4 On-chip SRAM

The LPC1311/13/42/43 contain a total of 8 kB (LPC1343 and LPC1313) or 4 kB (LPC1342 and LPC1311) on-chip static RAM memory.

7.5 Memory map

The LPC1311/13/42/43 incorporate several distinct memory regions. Figure 6 shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The AHB peripheral area is 2 MB in size and is divided to allow for up to 128 peripherals. The APB peripheral area is 512 kB in size and is divided to allow for up to 32 peripherals. Each peripheral of either type is allocated 16 kB of space. This allows simplifying the address decoding for each peripheral.

7.6.1 Features

- Controls system exceptions and peripheral interrupts.
- On the LPC1311/13/42/43, the NVIC supports up to 17 vectored interrupts. In addition, up to 40 of the individual GPIO inputs are NVIC-vector capable.
- 8 programmable interrupt priority levels, with hardware priority level masking
- Relocatable vector table.
- Software interrupt generation.

7.6.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Any GPIO pin (total of up to 42 pins) regardless of the selected function, can be programmed to generate an interrupt on a level, or rising edge or falling edge, or both.

7.7 IOCONFIG block

The IOCONFIG block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Peripherals should be connected to the appropriate pins prior to being activated and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

7.8 Fast general purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC1311/13/42/43 use accelerated GPIO functions:

- GPIO block is a dedicated AHB peripheral so that the fastest possible I/O timing can be achieved.
- Entire port value can be written in one instruction.

Additionally, any GPIO pin (total of up to 42 pins) providing a digital function can be programmed to generate an interrupt on a level, a rising or falling edge, or both.

7.8.1 Features

- Bit level port registers allow a single instruction to set or clear any number of bits in one write operation.
- Direction control of individual bits.
- All I/O default to inputs with pull-up resistors enabled after reset with the exception of the I^2C-bus pins PIO0_4 and PIO0_5.
- Pull-up/pull-down resistor configuration can be programmed through the IOCONFIG block for each GPIO pin.

- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the Internal RC oscillator (IRC), the watchdog oscillator, or the main clock. This gives a wide range of potential timing choices of watchdog operation under different power reduction conditions. It also provides the ability to run the WDT from an entirely internal source that is not dependent on an external crystal and its associated components and wiring for increased reliability.

7.17 Windowed WatchDog Timer (WWDT)

Remark: The windowed watchdog timer is available on parts LPC1311/01 and LPC1313/01.

The purpose of the watchdog is to reset the controller if software fails to periodically service it within a programmable time window.

7.17.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from ($T_{cy(WDCLK)} \times 256 \times 4$) to ($T_{cy(WDCLK)} \times 2^{24} \times 4$) in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the IRC or the dedicated watchdog oscillator (WDO). This gives a wide range of potential timing choices of watchdog operation under different power conditions.

7.18 Clocking and power control

7.18.1 Integrated oscillators

The LPC1311/13/42/43 include three independent oscillators. These are the system oscillator, the Internal RC oscillator (IRC), and the watchdog oscillator. Each oscillator can be used for more than one purpose as required in a particular application.

Following reset, the LPC1311/13/42/43 will operate from the internal RC oscillator until switched by software. This allows systems to operate without any external crystal and the bootloader code to operate at a known frequency.

See Figure 7 for an overview of the LPC1311/13/42/43 clock generation.

The vector table may be located anywhere within the bottom 1 GB of Cortex-M3 address space. The vector table must be located on a 256 word boundary.

7.20 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M3. Serial wire debug is supported.

Table 7. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	$2.5\ V \le V_{DD} \le 3.6\ V$; $I_{OH} = -4\ mA$		$V_{DD} - 0.4$	-	-	V
		$2.0\ V \le V_{DD} < 2.5\ V$; $I_{OH} = -3\ mA$		$V_{DD} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	$2.5\ V \le V_{DD} \le 3.6\ V$; $I_{OL} = 4\ mA$		-	-	0.4	V
		$2.0\ V \le V_{DD} < 2.5\ V$; $I_{OL} = 3\ mA$		-	-	0.4	V
I_{OH}	HIGH-level output current	$2.5\ V \le V_{DD} \le 3.6\ V$; $V_{OH} = V_{DD} - 0.4\ V$		−4	-	-	mA
		$2.0\ V \le V_{DD} < 2.5\ V$; $V_{OH} = V_{DD} - 0.4\ V$		−3	-	-	mA
I_{OL}	LOW-level output current	$2.5\ V \le V_{DD} \le 3.6\ V$; $V_{OL} = 0.4\ V$		4	-	-	mA
		$2.0\ V \le V_{DD} < 2.5\ V$; $V_{OL} = 0.4\ V$		3	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	$V_{OH} = 0\ V$	[15]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DD}$	[15]	-	-	50	mA
I_{pd}	pull-down current	$V_I = 5\ V$		10	50	150	µA
I_{pu}	pull-up current	$V_I = 0\ V$		−15	−50	−85	µA
		$V_{DD} < V_I < 5\ V$		0	0	0	µA
High-drive output pin (PIO0_7); see Figure 19 and Figure 21							
I_{IL}	LOW-level input current	$V_I = 0\ V$; on-chip pull-up resistor disabled		-	0.5	10	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled		-	0.5	10	nA
I_{OZ}	OFF-state output current	$V_O = 0\ V$; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled		-	0.5	10	nA
V_I	input voltage	pin configured to provide a digital function	[12][13] [14]	0	-	5.0	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	$2.5\ V \le V_{DD} \le 3.6\ V$; $I_{OH} = -20\ mA$		$V_{DD} - 0.4$	-	-	V
		$2.0\ V \le V_{DD} < 2.5\ V$; $I_{OH} = -12\ mA$		$V_{DD} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	$2.5\ V \le V_{DD} \le 3.6\ V$; $I_{OL} = 4\ mA$		-	-	0.4	V
		$2.0\ V \le V_{DD} < 2.5\ V$; $I_{OL} = 3\ mA$		-	-	0.4	V

Table 7. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{OH}	HIGH-level output current	2.5 V ≤ V_{DD} ≤ 3.6 V; V_{OH} = V_{DD} − 0.4 V		20	-	-	mA
		2.0 V ≤ V_{DD} < 2.5 V; V_{OH} = V_{DD} − 0.4 V;		12	-	-	mA
I_{OL}	LOW-level output current	2.5 V ≤ V_{DD} ≤ 3.6 V; V_{OL} = 0.4 V		4	-	-	mA
		2.0 V ≤ V_{DD} < 2.5 V; V_{OL} = 0.4 V		3	-	-	mA
I_{pd}	pull-down current	V_I = 5 V		10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V		−15	−50	−85	µA
		V_{DD} < V_I < 5 V		0	0	0	µA
I^2C-bus pins (PIO0_4 and PIO0_5); see Figure 20							
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3V_{DD}	V
V_{hys}	hysteresis voltage			-	0.05V_{DD}	-	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as standard mode pins					
		2.5 V ≤ V_{DD} ≤ 3.6 V		3.5	-	-	mA
		2.0 V ≤ V_{DD} < 2.5 V		3.0	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as Fast-mode Plus pins					
		2.5 V ≤ V_{DD} ≤ 3.6 V		20	-	-	mA
		2.0 V ≤ V_{DD} < 2.5 V		16	-	-	
I_{LI}	input leakage current	V_I = V_{DD}	[16]	-	2	4	µA
		V_I = 5 V		-	10	22	µA
Oscillator pins							
$V_{i(xtal)}$	crystal input voltage			−0.5	+1.8	+1.95	V
$V_{o(xtal)}$	crystal output voltage			−0.5	+1.8	+1.95	V
USB pins (LPC1342/43 only)							
I_{OZ}	OFF-state output current	0 V < V_I < 3.3 V	[17]	-	-	±10	µA
V_{BUS}	bus supply voltage		[17]	-	-	5.25	V
V_{DI}	differential input sensitivity voltage	|(D+) − (D−)|	[17]	0.2	-	-	V
V_{CM}	differential common mode voltage range	includes V_{DI} range	[17]	0.8	-	2.5	V
$V_{th(rs)se}$	single-ended receiver switching threshold voltage		[17]	0.8	-	2.0	V
V_{OL}	LOW-level output voltage	for low-/full-speed; R_L of 1.5 kΩ to 3.6 V	[17]	-	-	0.18	V

9.1 BOD static characteristics for LPC1300 series

Remark: Applies to parts LPC1311/13/42/43 and all their packages.

Table 9. BOD static characteristics[1]
T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 0				
		assertion	-	1.69	-	V
		de-assertion	-	1.84	-	V
		interrupt level 1				
		assertion	-	2.29	-	V
		de-assertion	-	2.44	-	V
		interrupt level 2				
		assertion	-	2.59	-	V
		de-assertion	-	2.74	-	V
		interrupt level 3				
		assertion	-	2.87	-	V
		de-assertion	-	2.98	-	V
		reset level 0				
		assertion	-	1.49	-	V
		de-assertion	-	1.64	-	V

[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see *LPC13xx user manual*.

9.2 BOD static characteristics for LPC1300L series (LPC1311/01 and LPC1313/01)

Remark: Applies to parts LPC1311/01 and LPC1313/01 and all packages.

Table 10. BOD static characteristics[1]
T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 0				
		assertion	-	1.65	-	V
		de-assertion	-	1.80	-	V
		interrupt level 1				
		assertion	-	2.22	-	V
		de-assertion	-	2.35	-	V
		interrupt level 2				
		assertion	-	2.52	-	V
		de-assertion	-	2.66	-	V
		interrupt level 3				
		assertion	-	2.80	-	V
		de-assertion	-	2.90	-	V
		reset level 0				
		assertion	-	1.46	-	V
		de-assertion	-	1.63	-	V
		reset level 1				
		assertion	-	2.06	-	V
		de-assertion	-	2.15	-	V
		reset level 2				
		assertion	-	2.35	-	V
		de-assertion	-	2.43	-	V
		reset level 3				
		assertion	-	2.63	-	V
		de-assertion	-	2.71	-	V

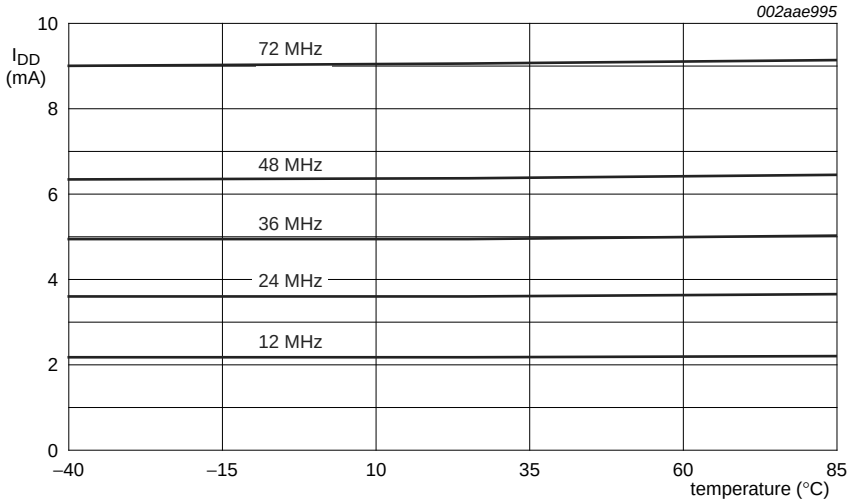
[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL, see *LPC13xx user manual*.

9.3 Power consumption for LPC1300 series

Remark: Applies to parts LPC1311/13/42/43 and all their packages.

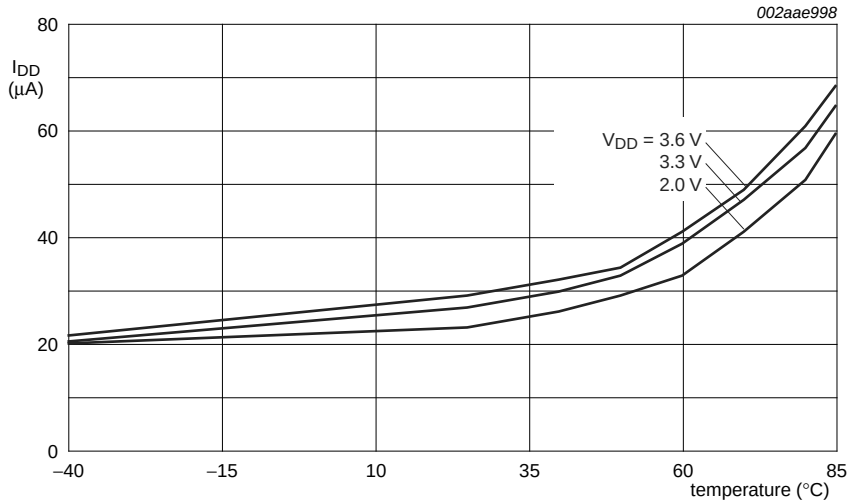
Power measurements in Active, Sleep, and Deep-sleep modes were performed under the following conditions (see *LPC13xx user manual*):

- Configure all pins as GPIO with pull-up resistor disabled in the IOCONFIG block.
- Configure GPIO pins as outputs using the GPIOnDIR registers.
- Write 0 to all GPIOnDATA registers to drive the outputs LOW.



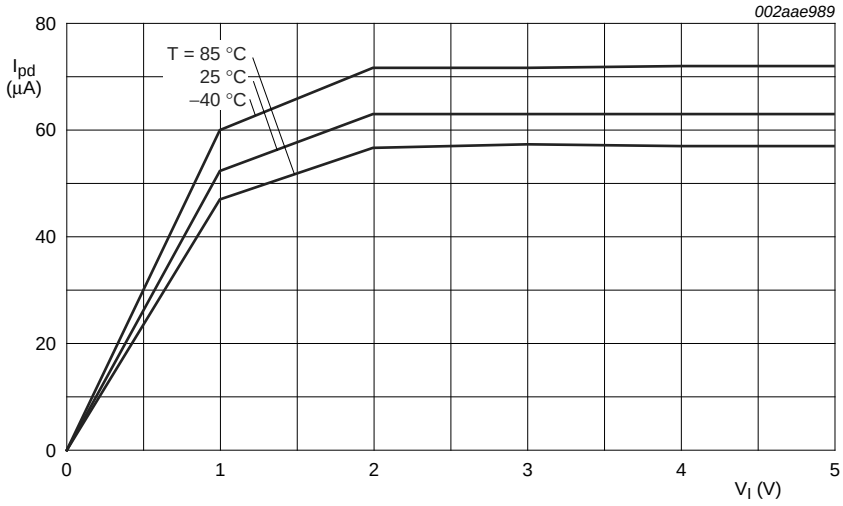
Conditions: V_{DD} = 3.3 V; Sleep mode entered from flash; internal pull-up resistors disabled; system oscillator and system PLL enabled; IRC, BOD disabled; all peripherals disabled in the SYSAHBCLKCTRL register (SYSAHBCLKCTRL = 0x1F); all peripheral clocks disabled; USB_DP and USB_DM pulled LOW externally (LPC1342/43).

Fig 11. Typical supply current versus temperature in Sleep mode (LPC1311/13/42/43)



Conditions: BOD disabled; all oscillators and analog blocks turned off in the PDSLEEPCFG register; PDSLEEPCFG = 0x0000 0FFF; USB_DP and USB_DM pulled LOW externally (LPC1342/43).

Fig 12. Typical supply current versus temperature in Deep-sleep mode (analog blocks disabled; LPC1311/13/42/43)



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 24. Typical pull-down current I_{pd} versus input voltage V_i

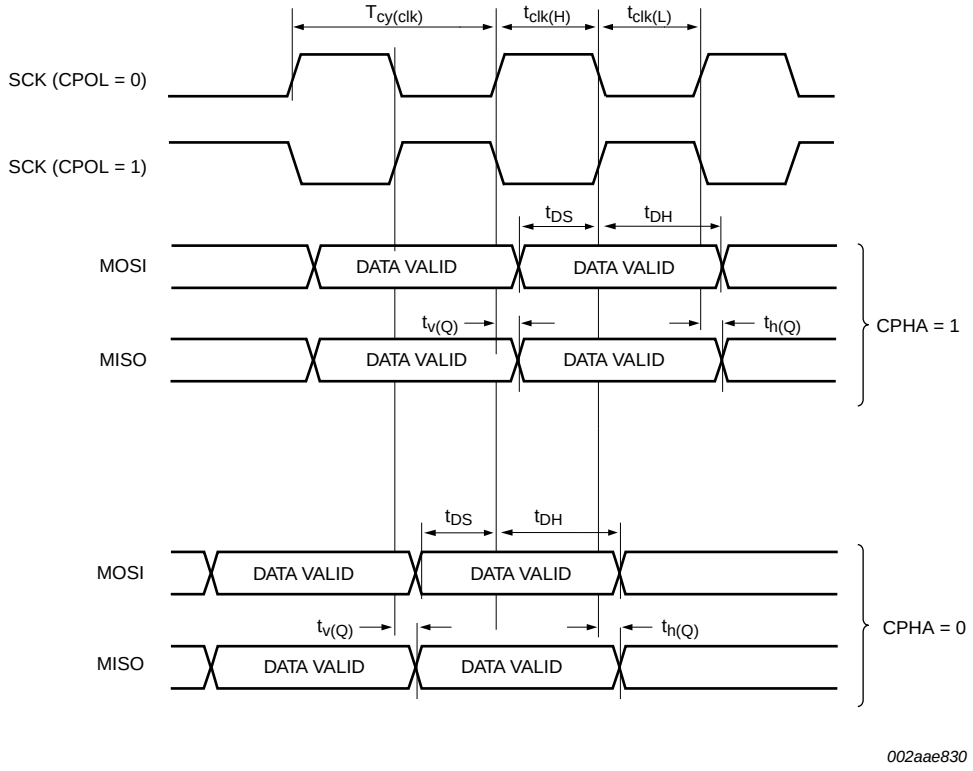
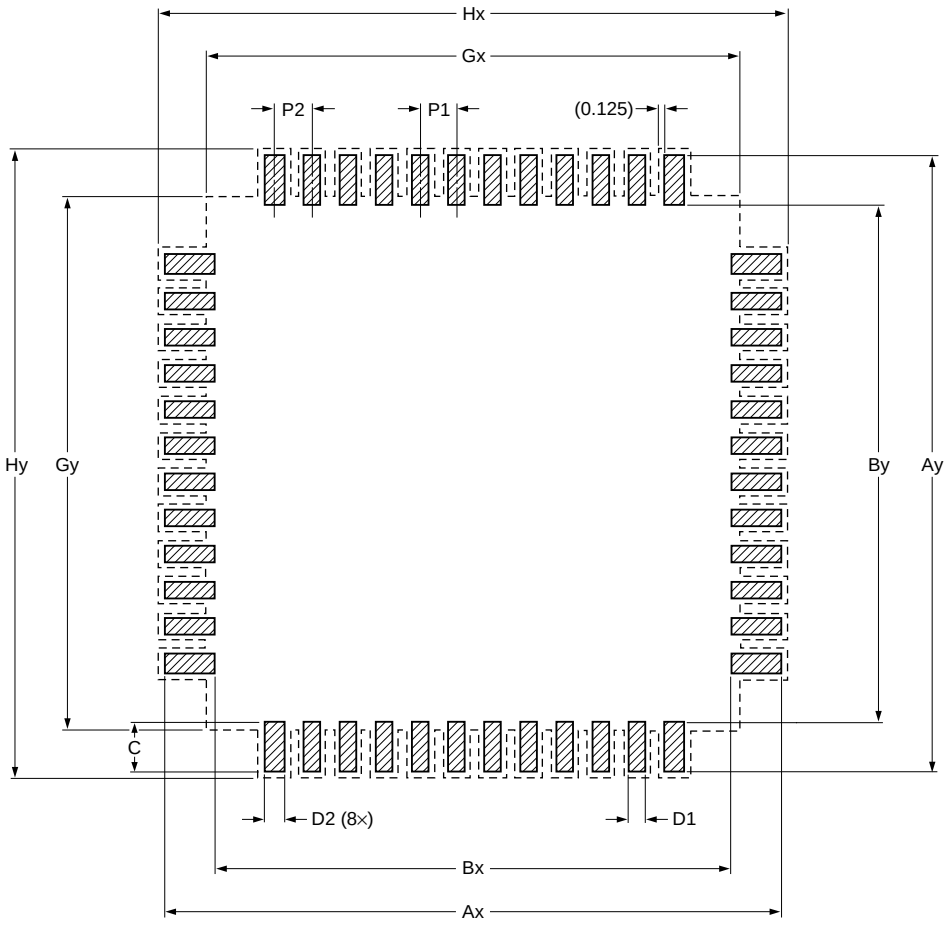


Fig 30. SSP slave timing in SPI mode

13. Soldering

Footprint information for reflow soldering of LQFP48 package **SOT313-2**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy
0.500	0.560	10.350	10.350	7.350	7.350	1.500	0.280	0.500	7.500	7.500	10.650	10.650

sot313-2_fr

Fig 40. Reflow soldering of the LQFP48 package

Footprint information for reflow soldering of HVQFN33 package

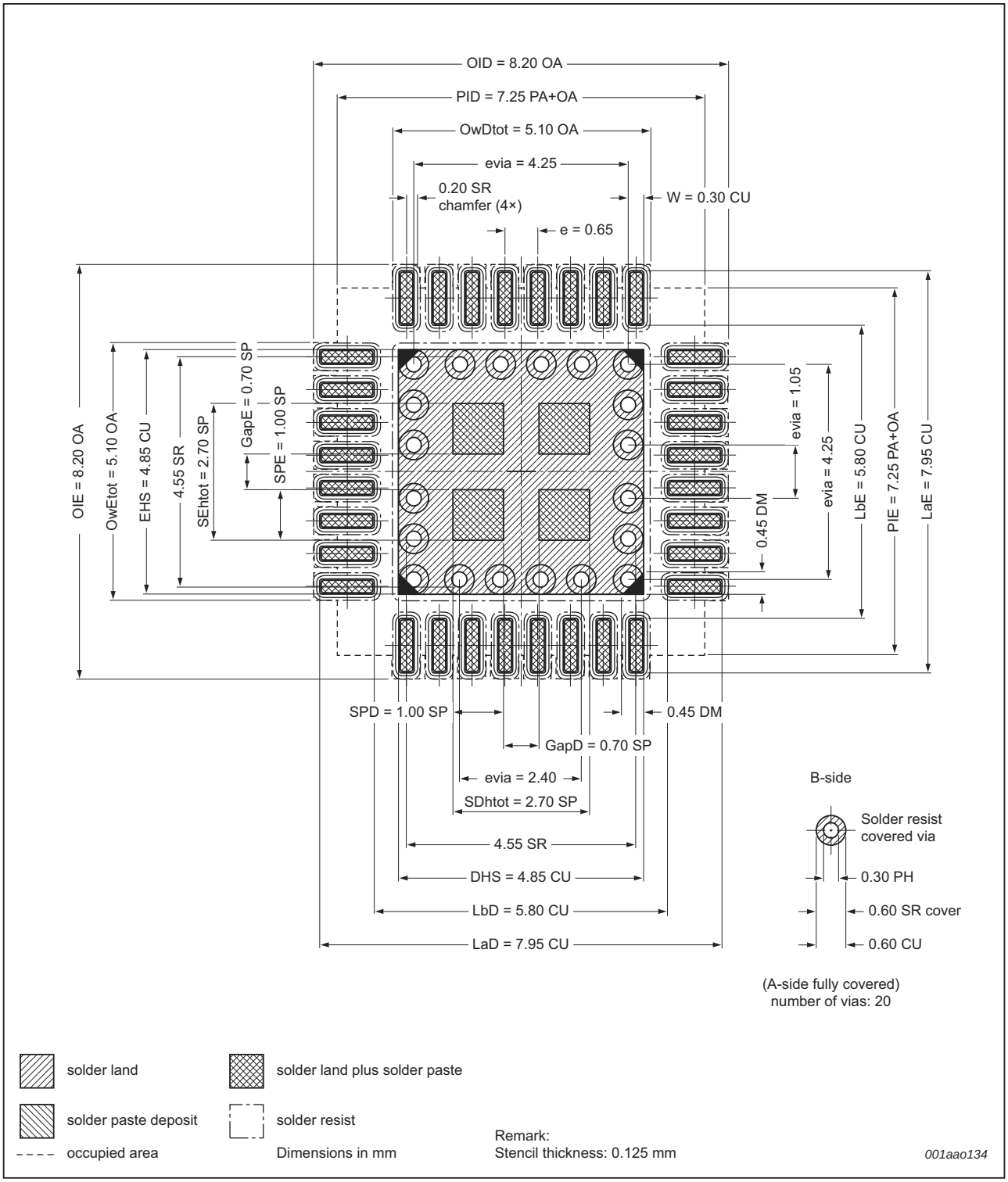


Fig 41. Reflow soldering of the HVQFN33 package

14. Abbreviations

Table 24. Abbreviations

Acronym	Description
A/D	Analog-to-Digital
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
EOP	End Of Packet
ETM	Embedded Trace Macrocell
FIFO	First-In, First-Out
GPIO	General Purpose Input/Output
HID	Human Interface Device
I/O	Input/Output
LSB	Least Significant Bit
MSC	Mass Storage Class
PHY	Physical Layer
PLL	Phase-Locked Loop
SE0	Single Ended Zero
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
SSP	Synchronous Serial Port
SoF	Start-of-Frame
TCM	Tightly-Coupled Memory
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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