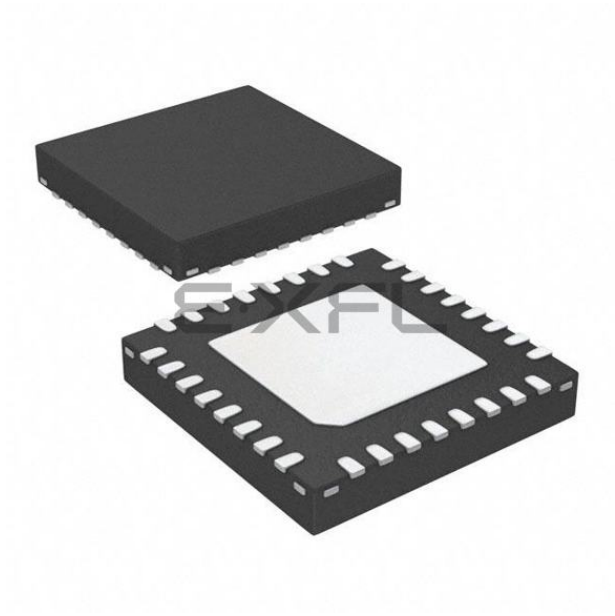

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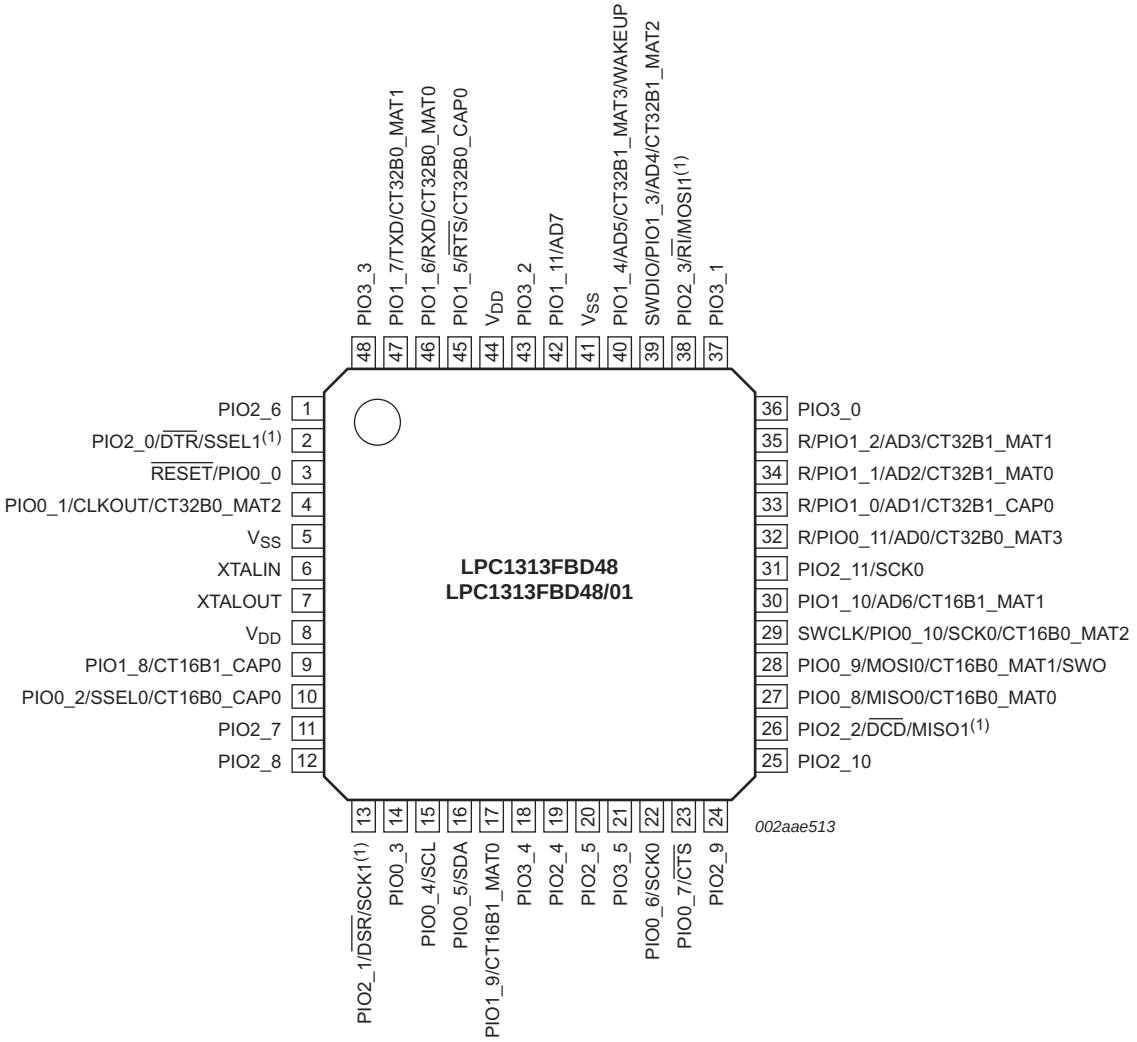
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	28
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VQFN Exposed Pad
Supplier Device Package	32-HVQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1343fhn33-518

- Serial interfaces:
  - USB 2.0 full-speed device controller with on-chip PHY for device (LPC1342/43 only).
  - UART with fractional baud rate generation, modem, internal FIFO, and RS-485/EIA-485 support.
  - SSP controller with FIFO and multi-protocol capabilities.
  - Additional SSP controller on LPC1313FBD48/01.
  - I^2C-bus interface supporting full I^2C-bus specification and Fast-mode Plus with a data rate of 1 Mbit/s with multiple address recognition and monitor mode.
- Other peripherals:
  - Up to 42 General Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors.
  - Four general purpose counter/timers with a total of four capture inputs and 13 match outputs.
  - Programmable WatchDog Timer (WDT).
  - Programmable Windowed Watchdog Timer (WWDT) on LPC1311/01 and LPC1313/01.
  - System tick timer.
- Serial Wire Debug and Serial Wire Trace port.
- High-current output driver (20 mA) on one pin.
- High-current sink drivers (20 mA) on two I^2C-bus pins in Fast-mode Plus.
- Integrated PMU (Power Management Unit) to minimize power consumption during Sleep, Deep-sleep, and Deep power-down modes.
- Power profiles residing in boot ROM allowing to optimize performance and minimize power consumption for any given application through one simple function call. (LPC1300L series, on LPC1311/01 and LPC1313/01 only.)
- Three reduced power modes: Sleep, Deep-sleep, and Deep power-down.
- Single power supply (2.0 V to 3.6 V).
- 10-bit ADC with input multiplexing among 8 pins.
- GPIO pins can be used as edge and level sensitive interrupt sources.
- Clock output function with divider that can reflect the system oscillator clock, IRC clock, CPU clock, or the watchdog clock.
- Processor wake-up from Deep-sleep mode via a dedicated start logic using up to 40 of the functional pins.
- Brownout detect with four separate thresholds for interrupt and one threshold for forced reset (four thresholds for forced reset on the LPC1311/01 and LPC1313/01 parts).
- Power-On Reset (POR).
- Integrated oscillator with an operating range of 1 MHz to 25 MHz.
- 12 MHz internal RC oscillator trimmed to 1 % accuracy over the entire temperature and voltage range that can optionally be used as a system clock.
- Programmable watchdog oscillator with a frequency range of 7.8 kHz to 1.8 MHz.
- System PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the system oscillator or the internal RC oscillator.
- For USB (LPC1342/43), a second, dedicated PLL is provided.
- Code Read Protection (CRP) with different security levels.



(1) SSP1 or UART function on LPC1313FBD48/01 only.

Fig 4. LPC1313 LQFP48 package

6.2 Pin description

Table 3. LPC1313/42/43 LQFP48 pin description table

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
$\overline{\text{RESET}}$/PIO0_0	3[2]	yes	I	I; PU	**$\overline{\text{RESET}}$ —** External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0.
			I/O	-	**PIO0_0 —** General purpose digital input/output pin with 10 ns glitch filter.
PIO0_1/CLKOUT/ CT32B0_MAT2/ USB_FTOGGLE	4[3]	yes	I/O	I; PU	**PIO0_1 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler or the USB device enumeration (USB on LPC1342/43 only, see description of PIO0_3).
			O	-	**CLKOUT —** Clockout pin.
			O	-	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
			O	-	**USB_FTOGGLE —** USB 1 ms Start-of-Frame signal (LPC1342/43 only).
PIO0_2/SSEL0/ CT16B0_CAP0	10[3]	yes	I/O	I; PU	**PIO0_2 —** General purpose digital input/output pin.
			I/O	-	**SSEL0 —** Slave select for SSP0.
			I	-	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
PIO0_3/USB_VBUS	14[3]	yes	I/O	I; PU	**PIO0_3 —** General purpose digital input/output pin. LPC1342/43 only: A LOW level on this pin during reset starts the ISP command handler, a HIGH level starts the USB device enumeration.
			I	-	**USB_VBUS —** Monitors the presence of USB bus power (LPC1342/43 only).
PIO0_4/SCL	15[4]	yes	I/O	I; IA	**PIO0_4 —** General purpose digital input/output pin (open-drain).
			I/O	-	**SCL —** I^2C-bus clock input/output (open-drain). High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_5/SDA	16[4]	yes	I/O	I; IA	**PIO0_5 —** General purpose digital input/output pin (open-drain).
			I/O	-	**SDA —** I^2C-bus data input/output (open-drain). High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_6/ $\overline{\text{USB\_CONNECT}}$/ SCK0	22[3]	yes	I/O	I; PU	**PIO0_6 —** General purpose digital input/output pin.
			O	-	**$\overline{\text{USB\_CONNECT}}$ —** Signal used to switch an external 1.5 kΩ resistor under software control. Used with the SoftConnect USB feature (LPC1342/43 only).
			I/O	-	**SCK0 —** Serial clock for SSP0.
PIO0_7/$\overline{\text{CTS}}$	23[3]	yes	I/O	I; PU	**PIO0_7 —** General purpose digital input/output pin (high-current output driver).
			I	-	**$\overline{\text{CTS}}$ —** Clear To Send input for UART.
PIO0_8/MISO0/ CT16B0_MAT0	27[3]	yes	I/O	I; PU	**PIO0_8 —** General purpose digital input/output pin.
			I/O	-	**MISO0 —** Master In Slave Out for SSP0.
			O	-	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.

Table 3. LPC1313/42/43 LQFP48 pin description table *…continued*

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
PIO1_5/$\overline{\text{RTS}}$/ CT32B0_CAP0	45[3]	yes	I/O	I; PU	**PIO1_5 —** General purpose digital input/output pin.
			O	-	**$\overline{\text{RTS}}$ —** Request To Send output for UART.
			I	-	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
PIO1_6/RXD/ CT32B0_MAT0	46[3]	yes	I/O	I; PU	**PIO1_6 —** General purpose digital input/output pin.
			I	-	**RXD —** Receiver input for UART.
			O	-	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.
PIO1_7/TXD/ CT32B0_MAT1	47[3]	yes	I/O	I; PU	**PIO1_7 —** General purpose digital input/output pin.
			O	-	**TXD —** Transmitter output for UART.
			O	-	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
PIO1_8/CT16B1_CAP0	9[3]	yes	I/O	I; PU	**PIO1_8 —** General purpose digital input/output pin.
			I	-	**CT16B1_CAP0 —** Capture input 0 for 16-bit timer 1.
PIO1_9/CT16B1_MAT0	17[3]	yes	I/O	I; PU	**PIO1_9 —** General purpose digital input/output pin.
			O	-	**CT16B1_MAT0 —** Match output 0 for 16-bit timer 1.
PIO1_10/AD6/ CT16B1_MAT1	30[5]	yes	I/O	I; PU	**PIO1_10 —** General purpose digital input/output pin.
			I	-	**AD6 —** A/D converter, input 6.
			O	-	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
PIO1_11/AD7	42[5]	yes	I/O	I; PU	**PIO1_11 —** General purpose digital input/output pin.
			I	-	**AD7 —** A/D converter, input 7.
PIO2_0/$\overline{\text{DTR}}$/SSEL1	2[3]	yes	I/O	I; PU	**PIO2_0 —** General purpose digital input/output pin.
			O	-	**$\overline{\text{DTR}}$ —** Data Terminal Ready output for UART.
			I/O	-	**SSEL1 —** Slave Select for SSP1 (LPC1313FBD48/01 only).
PIO2_1/$\overline{\text{DSR}}$/SCK1	13[3]	yes	I/O	I; PU	**PIO2_1 —** General purpose digital input/output pin.
			I	-	**$\overline{\text{DSR}}$ —** Data Set Ready input for UART.
			I/O	-	**SCK1 —** Serial clock for SSP1 (LPC1313FBD48/01 only).
PIO2_2/$\overline{\text{DCD}}$/MISO1	26[3]	yes	I/O	I; PU	**PIO2_2 —** General purpose digital input/output pin.
			I	-	**$\overline{\text{DCD}}$ —** Data Carrier Detect input for UART.
			I/O	-	**MISO1 —** Master In Slave Out for SSP1 (LPC1313FBD48/01 only).
PIO2_3/$\overline{\text{RI}}$/MOSI1	38[3]	yes	I/O	I; PU	**PIO2_3 —** General purpose digital input/output pin.
			I	-	**$\overline{\text{RI}}$ —** Ring Indicator input for UART.
			I/O	-	**MOSI1 —** Master Out Slave In for SSP1 (LPC1313FBD48/01 only).
PIO2_4	18[3]	yes	I/O	I; PU	**PIO2_4 —** General purpose digital input/output pin (LPC1342/43 only).
PIO2_4	19[3]	yes	I/O	I; PU	**PIO2_4 —** General purpose digital input/output pin (LPC1313 only).
PIO2_5	21[3]	yes	I/O	I; PU	**PIO2_5 —** General purpose digital input/output pin (LPC1342/43 only).
PIO2_5	20[3]	yes	I/O	I; PU	**PIO2_5 —** General purpose digital input/output pin (LPC1313 only).
PIO2_6	1[3]	yes	I/O	I; PU	**PIO2_6 —** General purpose digital input/output pin.
PIO2_7	11[3]	yes	I/O	I; PU	**PIO2_7 —** General purpose digital input/output pin.
PIO2_8	12[3]	yes	I/O	I; PU	**PIO2_8 —** General purpose digital input/output pin.
PIO2_9	24[3]	yes	I/O	I; PU	**PIO2_9 —** General purpose digital input/output pin.

7.10 UART

The LPC1311/13/42/43 contains one UART.

Support for RS-485/9-bit mode allows both software address detection and automatic address detection using 9-bit mode.

The UART includes a fractional baud rate generator. Standard baud rates such as 115200 Bd can be achieved with any crystal frequency above 2 MHz.

7.10.1 Features

- Maximum UART data bit rate of 4.5 MBit/s.
- 16-byte receive and transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B.
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Fractional divider for baud rate control, auto baud capabilities and FIFO control mechanism that enables software flow control implementation.
- Support for RS-485/9-bit mode.
- Support for modem control.

7.11 SSP serial I/O controller

The LPC1311/13/42/43 contain one SSP controller. An additional SSP controller is available on the LPC1313FBD48/01 package.

The SSP controller is capable of operation on a SSP, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

7.11.1 Features

- Maximum SSP speed of 36 Mbit/s (master) or 6 Mbit/s (slave)
- Compatible with Motorola SPI, 4-wire Texas Instruments SSI, and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame

7.12 I^2C-bus serial I/O controller

The LPC1311/13/42/43 contain one I^2C-bus controller.

7.14 General purpose external event counter/timers

The LPC1311/13/42/43 includes two 32-bit counter/timers and two 16-bit counter/timers. The counter/timer is designed to count cycles of the system derived clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. Each counter/timer also includes one capture input to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.14.1 Features

- A 32-bit/16-bit counter/timer with a programmable 32-bit/16-bit prescaler.
- Counter or timer operation.
- One capture channel per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also generate an interrupt.
- Four match registers per timer that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to four external outputs corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

7.15 System tick timer

The ARM Cortex-M3 includes a system tick timer (SYSTICK) that is intended to generate a dedicated SYSTICK exception at a fixed time interval, normally set to 10 ms.

7.16 Watchdog timer

Remark: The standard Watchdog timer is available on parts LPC1311/13/42/43.

The purpose of the watchdog is to reset the microcontroller within a selectable time period. When enabled, the watchdog will generate a system reset if the user program fails to ‘feed’ (or reload) the watchdog within a predetermined amount of time.

7.16.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect/incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.

Upon power-up, any chip reset, or wake-up from Deep power-down mode, the LPC1311/13/42/43 use the IRC as the clock source. Software may later switch to one of the other available clock sources.

7.18.1.2 System oscillator

The system oscillator can be used as the clock source for the CPU, with or without using the PLL. On the LPC1342/43, the system oscillator must be used to provide the clock source to USB.

The system oscillator operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

7.18.1.3 Watchdog oscillator

The watchdog oscillator can be used as a clock source that directly drives the CPU, the watchdog timer, or the CLKOUT pin. The watchdog oscillator nominal frequency is programmable between 7.8 kHz and 1.7 MHz. The frequency spread over processing and temperature is ±40 % (see also Table 16).

7.18.2 System PLL and USB PLL

The LPC1342/43 contain a system PLL and a dedicated PLL for generating the 48 MHz USB clock. The LPC131x contain the system PLL only. The system and USB PLLs are identical.

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. The PLL output frequency must be lower than 100 MHz. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is 100 µs.

7.18.3 Clock output

The LPC1311/13/42/43 features a clock output function that routes the IRC oscillator, the system oscillator, the watchdog oscillator, or the main clock to an output pin.

7.18.4 Wake-up process

The LPC1311/13/42/43 begin operation at power-up and when awakened from Deep power-down mode by using the 12 MHz IRC oscillator as the clock source. This allows chip operation to resume quickly. If the main oscillator or the PLL is needed by the application, software will need to enable these features and wait for them to stabilize before they are used as a clock source.

7.18.5 Power control

The LPC1311/13/42/43 support a variety of power control features. There are three special modes of processor power reduction: Sleep mode, Deep-sleep mode, and Deep power-down mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals, allowing fine tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

7.18.5.1 Power profiles (LPC1300L series, LPC1311/01 and LPC1313/01 only)

The power consumption in Active and Sleep modes can be optimized for the application through simple calls to the power profile. The power configuration routine configures the LPC1311/01 and the LPC1313/01 for one of the following power modes:

- Default mode corresponding to power configuration after reset.
- CPU performance mode corresponding to optimized processing capability.
- Efficiency mode corresponding to optimized balance of current consumption and CPU performance.
- Low-current mode corresponding to lowest power consumption.

In addition, the power profile includes routines to select the optimal PLL settings for a given system clock and PLL input clock.

7.18.5.2 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

7.18.5.3 Deep-sleep mode

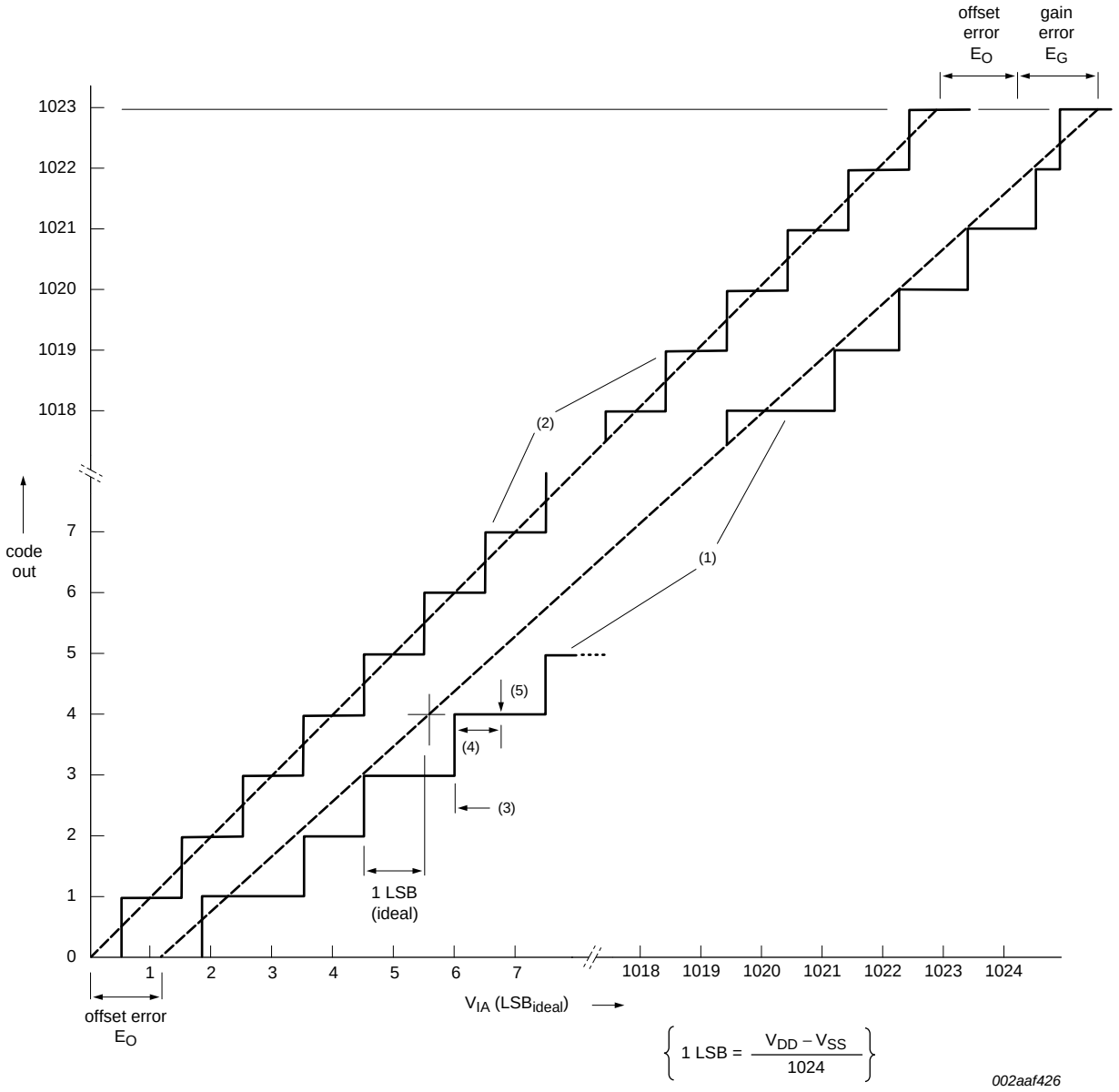
In Deep-sleep mode, the chip is in Sleep mode, and in addition all analog blocks are shut down. As an exception, the user has the option to keep the watchdog oscillator and the BOD circuit running for self-timed wake-up and BOD protection. Deep-sleep mode allows for additional power savings.

Up to 40 pins total can serve as external wake-up pins to the start logic to wake up the chip from Deep-sleep mode (see Section 7.19.1).

Unless the watchdog oscillator is selected to run in Deep-sleep mode, the clock source should be switched to IRC before entering Deep-sleep mode, because the IRC can be switched on and off glitch-free.

Table 7. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{OH}	HIGH-level output current	2.5 V ≤ V_{DD} ≤ 3.6 V; V_{OH} = V_{DD} − 0.4 V		20	-	-	mA
		2.0 V ≤ V_{DD} < 2.5 V; V_{OH} = V_{DD} − 0.4 V;		12	-	-	mA
I_{OL}	LOW-level output current	2.5 V ≤ V_{DD} ≤ 3.6 V; V_{OL} = 0.4 V		4	-	-	mA
		2.0 V ≤ V_{DD} < 2.5 V; V_{OL} = 0.4 V		3	-	-	mA
I_{pd}	pull-down current	V_I = 5 V		10	50	150	µA
I_{pu}	pull-up current	V_I = 0 V		−15	−50	−85	µA
		V_{DD} < V_I < 5 V		0	0	0	µA
I^2C-bus pins (PIO0_4 and PIO0_5); see Figure 20							
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.3V_{DD}	V
V_{hys}	hysteresis voltage			-	0.05V_{DD}	-	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as standard mode pins					
		2.5 V ≤ V_{DD} ≤ 3.6 V		3.5	-	-	mA
		2.0 V ≤ V_{DD} < 2.5 V		3.0	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; I^2C-bus pins configured as Fast-mode Plus pins					
		2.5 V ≤ V_{DD} ≤ 3.6 V		20	-	-	mA
		2.0 V ≤ V_{DD} < 2.5 V		16	-	-	
I_{LI}	input leakage current	V_I = V_{DD}	[16]	-	2	4	µA
		V_I = 5 V		-	10	22	µA
Oscillator pins							
$V_{i(xtal)}$	crystal input voltage			−0.5	+1.8	+1.95	V
$V_{o(xtal)}$	crystal output voltage			−0.5	+1.8	+1.95	V
USB pins (LPC1342/43 only)							
I_{OZ}	OFF-state output current	0 V < V_I < 3.3 V	[17]	-	-	±10	µA
V_{BUS}	bus supply voltage		[17]	-	-	5.25	V
V_{DI}	differential input sensitivity voltage	|(D+) − (D−)|	[17]	0.2	-	-	V
V_{CM}	differential common mode voltage range	includes V_{DI} range	[17]	0.8	-	2.5	V
$V_{th(rs)se}$	single-ended receiver switching threshold voltage		[17]	0.8	-	2.0	V
V_{OL}	LOW-level output voltage	for low-/full-speed; R_L of 1.5 kΩ to 3.6 V	[17]	-	-	0.18	V



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 8. ADC characteristics

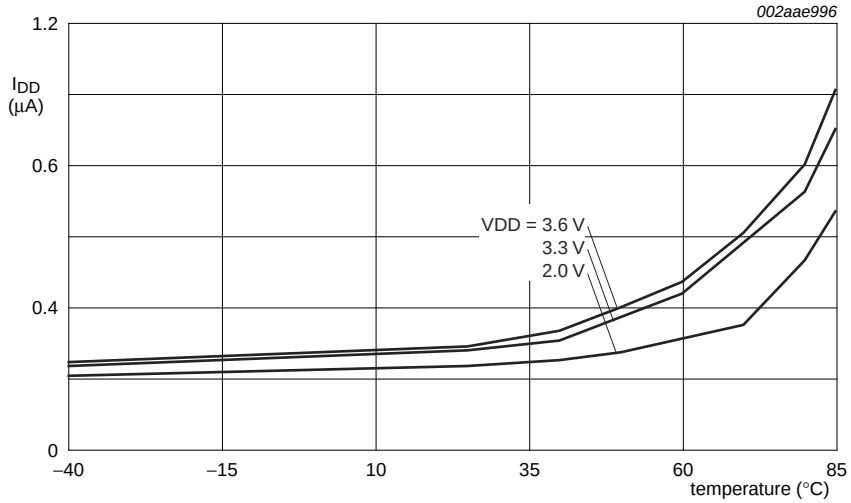


Fig 13. Typical supply current versus temperature in Deep power-down mode (LPC1311/13/42/43)

9.4 Power consumption for LPC1300L series (LPC1311/01 and LPC1313/01)

Remark: Applies to parts LPC1311/01 and LPC1313/01 and all their packages.

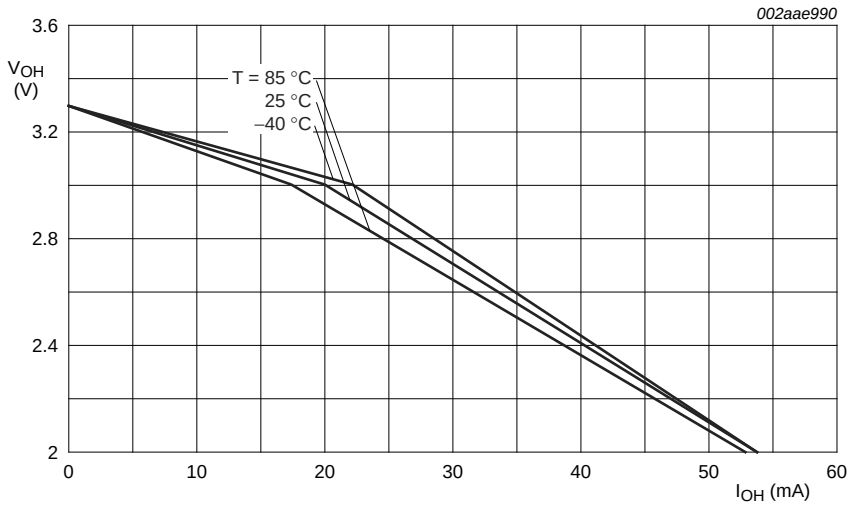
Power measurements in Active, Sleep, and Deep-sleep modes were performed under the following conditions (see *LPC13xx user manual*):

- Configure all pins as GPIO with pull-up resistor disabled in the IOCONFIG block.
- Configure GPIO pins as outputs using the GPIOnDIR registers.
- Write 0 to all GPIOnDATA registers to drive the outputs LOW.

Table 11. Power consumption for individual analog and digital blocks *…continued*

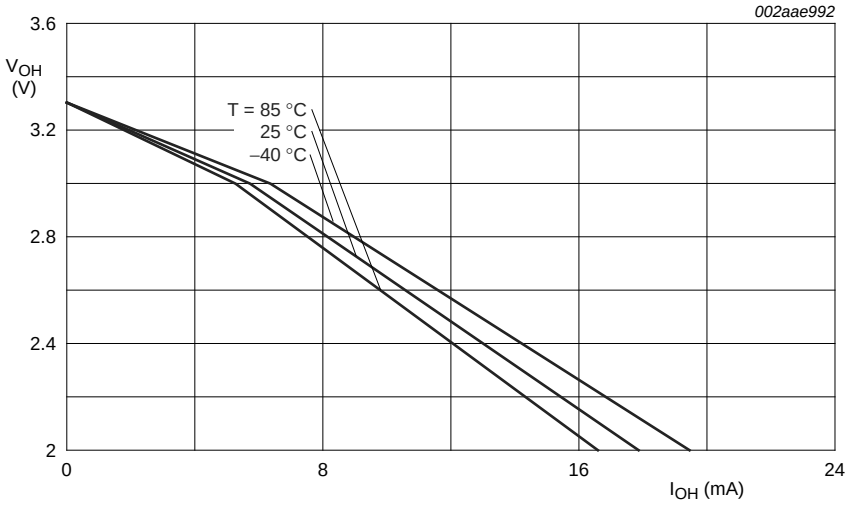
Peripheral	Typical supply current in mA				Notes
	n/a	12 MHz	48 MHz	72 MHz	
GPIO	-	0.21	0.80	1.17	GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register.
IOCONFIG	-	0.00	0.02	0.02	-
I2C	-	0.03	0.12	0.17	-
ROM	-	0.04	0.15	0.22	-
SSP0	-	0.11	0.41	0.60	-
SSP1	-	0.11	0.41	0.60	On LPC1313FBD48/01 only.
UART	-	0.20	0.76	1.11	-
WDT	-	0.01	0.05	0.08	Main clock selected as clock source for the WDT.
USB	-	-	3.91	-	Main clock selected as clock source for the USB. USB_DP and USB_DM pulled LOW externally.
USB	-	1.84	4.19	5.71	Dedicated USB PLL selected as clock source for the USB. USB_DP and USB_DM pulled LOW externally.

9.6 Electrical pin characteristics



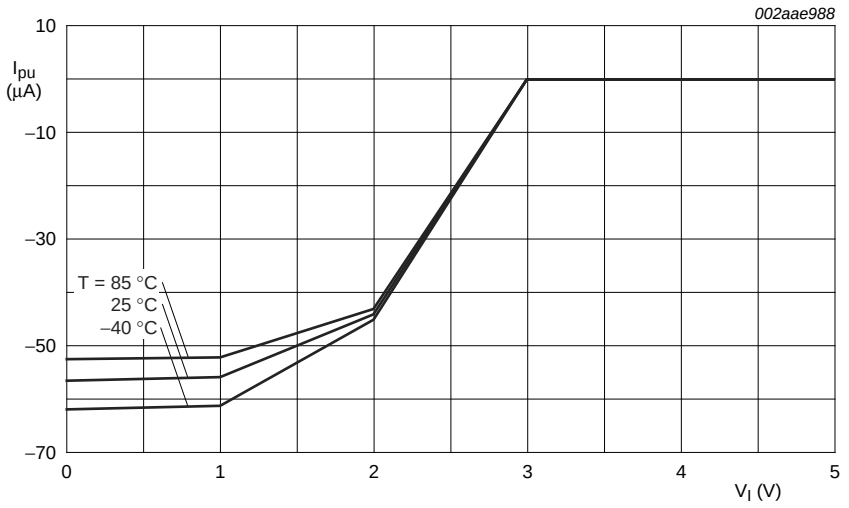
Conditions: V_{DD} = 3.3 V; on pin PIO0_7.

Fig 19. High-drive output: Typical HIGH-level output voltage V_{OH} versus HIGH-level output current I_{OH}.



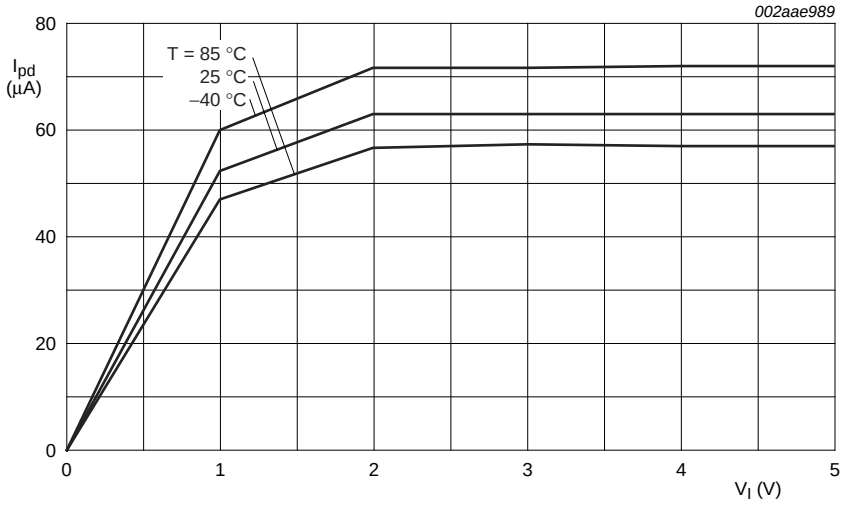
Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 22. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 23. Typical pull-up current I_{pu} versus input voltage V_i



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 24. Typical pull-down current I_{pd} versus input voltage V_i

10.4 Internal oscillators

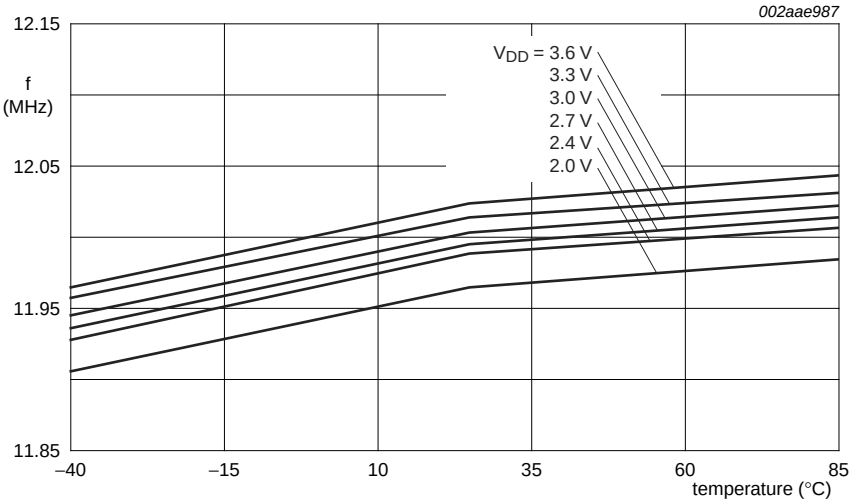
Table 15. Dynamic characteristics: IRC

T_{amb} = –40 °C to +85 °C; 2.7 V ≤ V_{DD} ≤ 3.6 V[1].

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	-	11.88	12	12.12	MHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.



Conditions: Frequency values are typical values. 12 MHz ± 1 % accuracy is guaranteed for 2.7 V ≤ V_{DD} ≤ 3.6 V and T_{amb} = –40 °C to +85 °C. Variations between parts may cause the IRC to fall outside the 12 MHz ± 1 % accuracy specification for voltages below 2.7 V.

Fig 27. Internal RC oscillator frequency f versus temperature

Table 16. Dynamic characteristics: Watchdog oscillator

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$f_{osc(int)}$	internal oscillator frequency	DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register;	[2][3]	-	7.8	-	kHz
		DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register	[2][3]	-	1700	-	kHz

[1] Typical ratings are not guaranteed. The values listed are at nominal supply voltages.

[2] The typical frequency spread over processing and temperature (T_{amb} = –40 °C to +85 °C) is ±40 %.

[3] See the *LPC13xx user manual.*

10.5 I/O pins

Table 17. Dynamic characteristics: I/O pins[1]
T_{amb} = –40 °C to +85 °C; 3.0 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	pin configured as output	3.0	-	5.0	ns
t_f	fall time	pin configured as output	2.5	-	5.0	ns

[1] Applies to standard port pins and $\overline{\text{RESET}}$ pin.

10.6 I²C-bus

Table 18. Dynamic characteristic: I²C-bus pins[1]
T_{amb} = –40 °C to +85 °C.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency		Standard-mode	0	100	kHz
			Fast-mode	0	400	kHz
			Fast-mode Plus	0	1	MHz
t_f	fall time	[4][5][6][7]	of both SDA and SCL signals	-	300	ns
			Standard-mode			
			Fast-mode	$20 + 0.1 \times C_b$	300	ns
			Fast-mode Plus	-	120	ns
t_{LOW}	LOW period of the SCL clock		Standard-mode	4.7	-	µs
			Fast-mode	1.3	-	µs
			Fast-mode Plus	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	µs
			Fast-mode	0.6	-	µs
			Fast-mode Plus	0.26	-	µs
$t_{HD;DAT}$	data hold time	[3][4][8]	Standard-mode	0	-	µs
			Fast-mode	0	-	µs
			Fast-mode Plus	0	-	µs
$t_{SU;DAT}$	data set-up time	[9][10]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns
			Fast-mode Plus	50	-	ns

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

[8] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see *UM10204*). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[9] $t_{SU;DAT}$ is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.

[10] A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system but the requirement $t_{SU;DAT}$ = 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-mode I^2C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

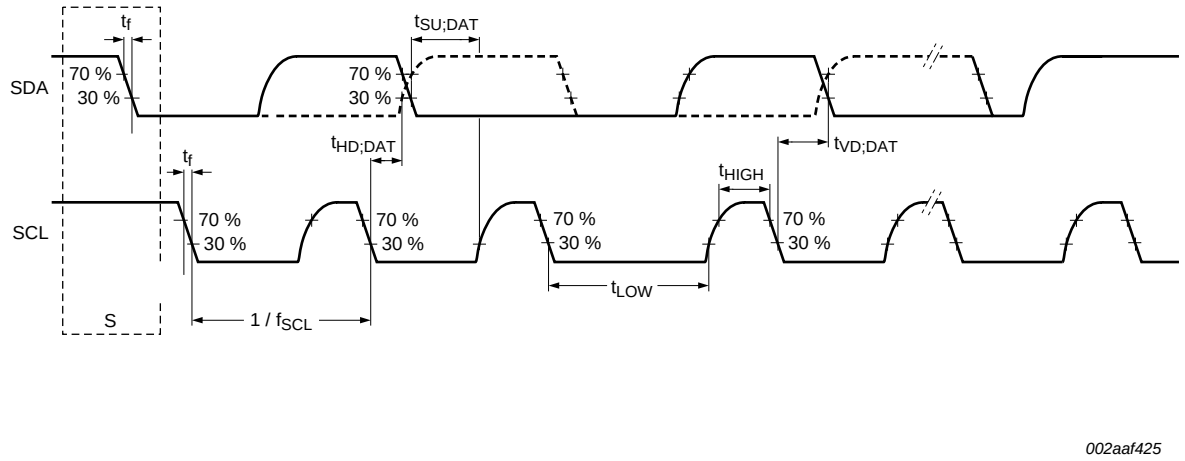


Fig 28. I^2C-bus pins clock timing

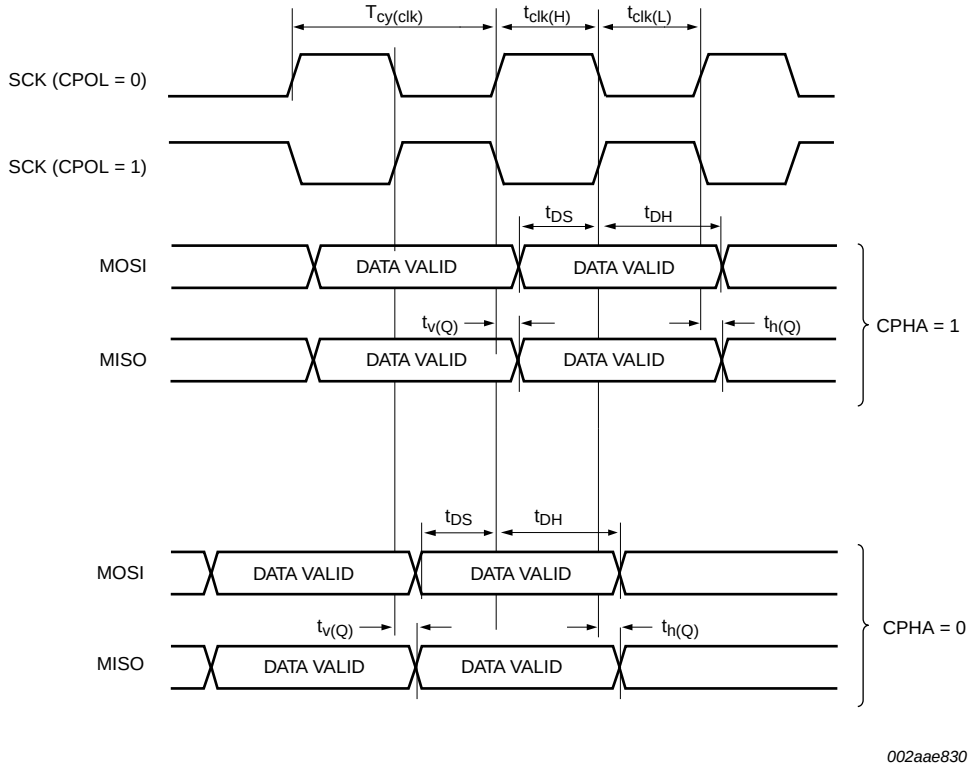


Fig 30. SSP slave timing in SPI mode

11. Application information

11.1 Suggested USB interface solutions (LPC1342/43 only)

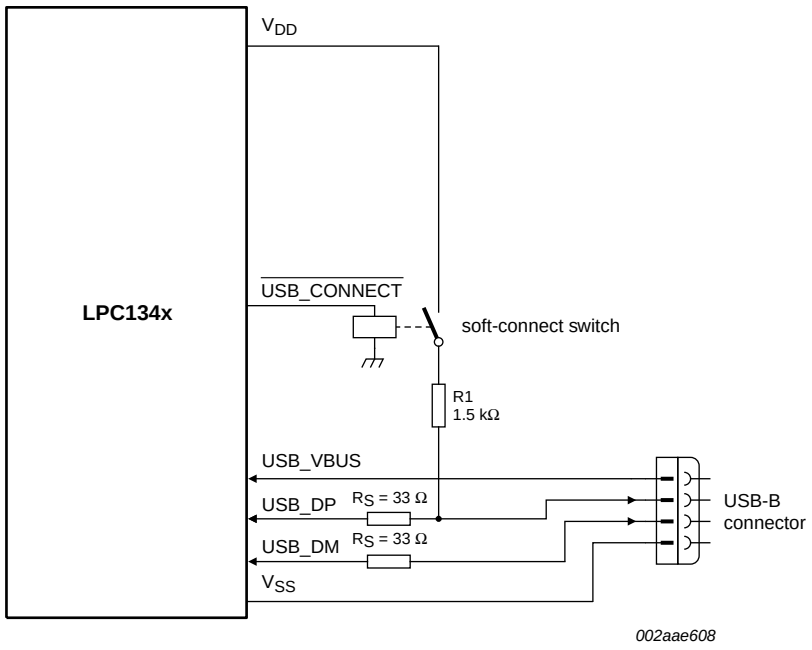


Fig 32. LPC1342/43 USB interface on a self-powered device

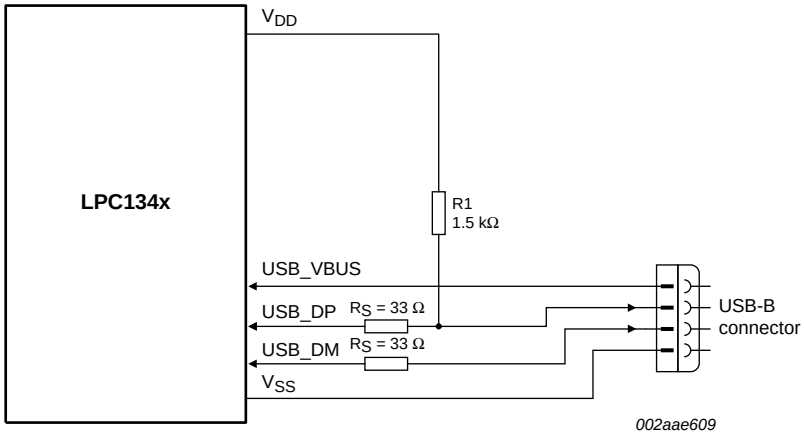


Fig 33. LPC1342/43 USB interface on a bus-powered device

11.2 XTAL input

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with C_i = 100 pF. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV(RMS) is needed.

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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