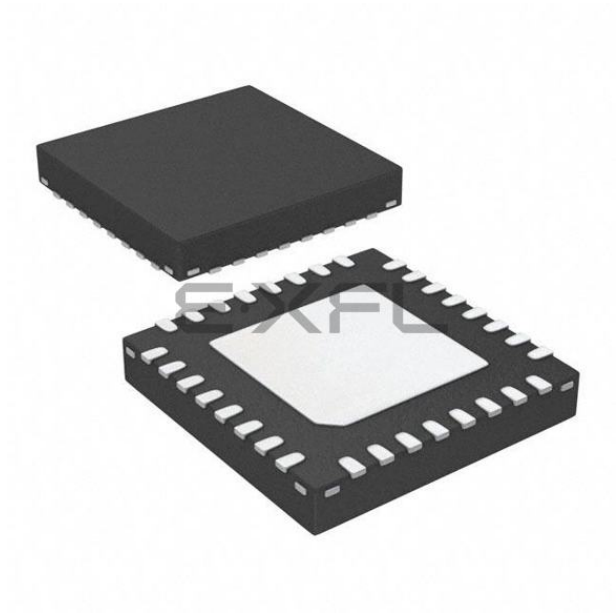

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	28
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VQFN Exposed Pad
Supplier Device Package	32-HVQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc1343fhn33-551

6. Pinning information

6.1 Pinning

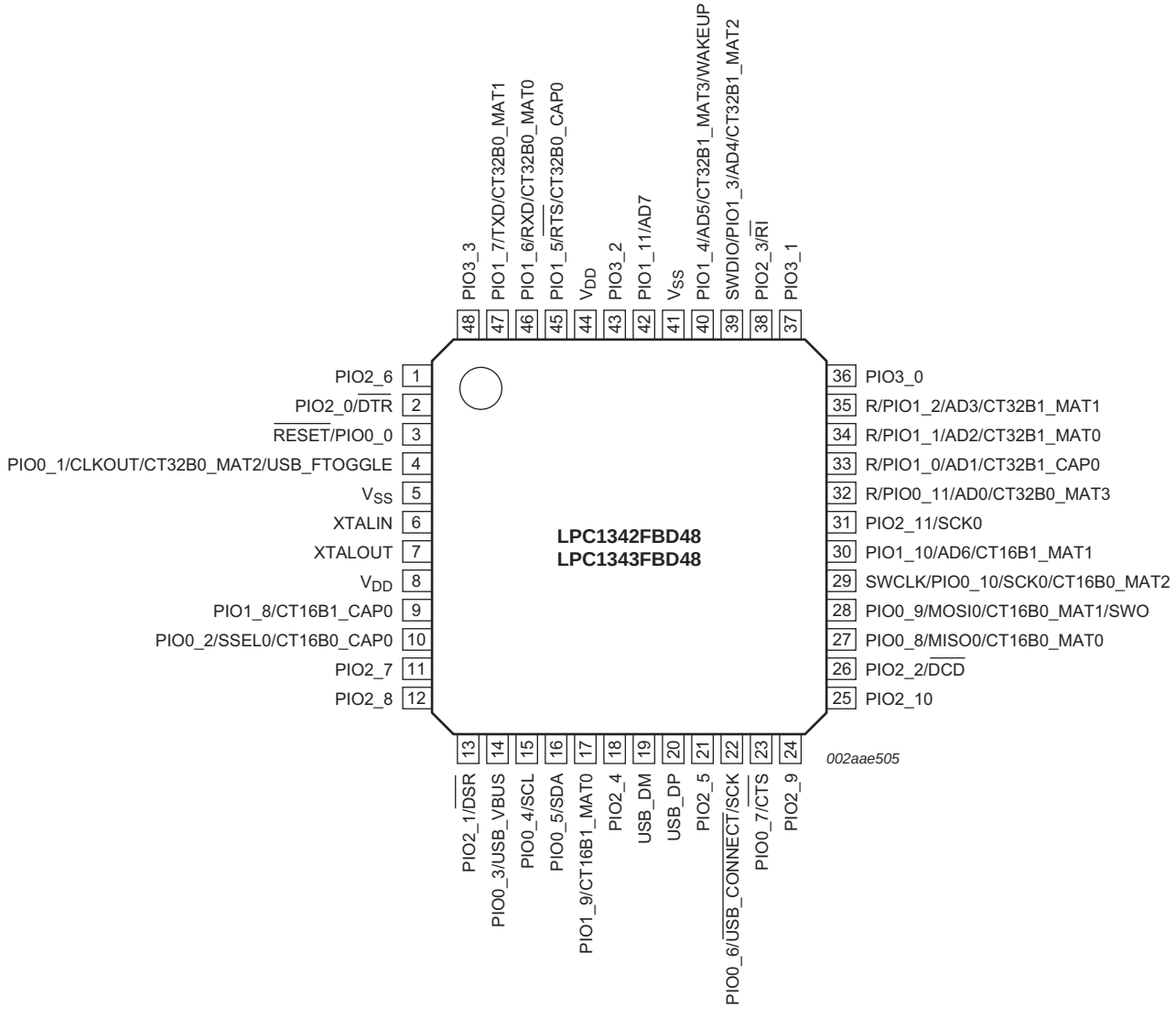

Fig 2. LPC1342/43 LQFP48 package

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6.2 Pin description

Table 3. LPC1313/42/43 LQFP48 pin description table

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
$\overline{\text{RESET}}$/PIO0_0	3[2]	yes	I	I; PU	**$\overline{\text{RESET}}$ —** External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0.
			I/O	-	**PIO0_0 —** General purpose digital input/output pin with 10 ns glitch filter.
PIO0_1/CLKOUT/ CT32B0_MAT2/ USB_FTOGGLE	4[3]	yes	I/O	I; PU	**PIO0_1 —** General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler or the USB device enumeration (USB on LPC1342/43 only, see description of PIO0_3).
			O	-	**CLKOUT —** Clockout pin.
			O	-	**CT32B0_MAT2 —** Match output 2 for 32-bit timer 0.
			O	-	**USB_FTOGGLE —** USB 1 ms Start-of-Frame signal (LPC1342/43 only).
PIO0_2/SSEL0/ CT16B0_CAP0	10[3]	yes	I/O	I; PU	**PIO0_2 —** General purpose digital input/output pin.
			I/O	-	**SSEL0 —** Slave select for SSP0.
			I	-	**CT16B0_CAP0 —** Capture input 0 for 16-bit timer 0.
PIO0_3/USB_VBUS	14[3]	yes	I/O	I; PU	**PIO0_3 —** General purpose digital input/output pin. LPC1342/43 only: A LOW level on this pin during reset starts the ISP command handler, a HIGH level starts the USB device enumeration.
			I	-	**USB_VBUS —** Monitors the presence of USB bus power (LPC1342/43 only).
PIO0_4/SCL	15[4]	yes	I/O	I; IA	**PIO0_4 —** General purpose digital input/output pin (open-drain).
			I/O	-	**SCL —** I^2C-bus clock input/output (open-drain). High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_5/SDA	16[4]	yes	I/O	I; IA	**PIO0_5 —** General purpose digital input/output pin (open-drain).
			I/O	-	**SDA —** I^2C-bus data input/output (open-drain). High-current sink only if I^2C Fast-mode Plus is selected in the I/O configuration register.
PIO0_6/ $\overline{\text{USB\_CONNECT}}$/ SCK0	22[3]	yes	I/O	I; PU	**PIO0_6 —** General purpose digital input/output pin.
			O	-	**$\overline{\text{USB\_CONNECT}}$ —** Signal used to switch an external 1.5 kΩ resistor under software control. Used with the SoftConnect USB feature (LPC1342/43 only).
			I/O	-	**SCK0 —** Serial clock for SSP0.
PIO0_7/$\overline{\text{CTS}}$	23[3]	yes	I/O	I; PU	**PIO0_7 —** General purpose digital input/output pin (high-current output driver).
			I	-	**$\overline{\text{CTS}}$ —** Clear To Send input for UART.
PIO0_8/MISO0/ CT16B0_MAT0	27[3]	yes	I/O	I; PU	**PIO0_8 —** General purpose digital input/output pin.
			I/O	-	**MISO0 —** Master In Slave Out for SSP0.
			O	-	**CT16B0_MAT0 —** Match output 0 for 16-bit timer 0.

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Table 3. LPC1313/42/43 LQFP48 pin description table *…continued*

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
PIO1_5/$\overline{\text{RTS}}$/ CT32B0_CAP0	45[3]	yes	I/O	I; PU	**PIO1_5 —** General purpose digital input/output pin.
			O	-	**$\overline{\text{RTS}}$ —** Request To Send output for UART.
			I	-	**CT32B0_CAP0 —** Capture input 0 for 32-bit timer 0.
PIO1_6/RXD/ CT32B0_MAT0	46[3]	yes	I/O	I; PU	**PIO1_6 —** General purpose digital input/output pin.
			I	-	**RXD —** Receiver input for UART.
			O	-	**CT32B0_MAT0 —** Match output 0 for 32-bit timer 0.
PIO1_7/TXD/ CT32B0_MAT1	47[3]	yes	I/O	I; PU	**PIO1_7 —** General purpose digital input/output pin.
			O	-	**TXD —** Transmitter output for UART.
			O	-	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
PIO1_8/CT16B1_CAP0	9[3]	yes	I/O	I; PU	**PIO1_8 —** General purpose digital input/output pin.
			I	-	**CT16B1_CAP0 —** Capture input 0 for 16-bit timer 1.
PIO1_9/CT16B1_MAT0	17[3]	yes	I/O	I; PU	**PIO1_9 —** General purpose digital input/output pin.
			O	-	**CT16B1_MAT0 —** Match output 0 for 16-bit timer 1.
PIO1_10/AD6/ CT16B1_MAT1	30[5]	yes	I/O	I; PU	**PIO1_10 —** General purpose digital input/output pin.
			I	-	**AD6 —** A/D converter, input 6.
			O	-	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
PIO1_11/AD7	42[5]	yes	I/O	I; PU	**PIO1_11 —** General purpose digital input/output pin.
			I	-	**AD7 —** A/D converter, input 7.
PIO2_0/$\overline{\text{DTR}}$/SSEL1	2[3]	yes	I/O	I; PU	**PIO2_0 —** General purpose digital input/output pin.
			O	-	**$\overline{\text{DTR}}$ —** Data Terminal Ready output for UART.
			I/O	-	**SSEL1 —** Slave Select for SSP1 (LPC1313FBD48/01 only).
PIO2_1/$\overline{\text{DSR}}$/SCK1	13[3]	yes	I/O	I; PU	**PIO2_1 —** General purpose digital input/output pin.
			I	-	**$\overline{\text{DSR}}$ —** Data Set Ready input for UART.
			I/O	-	**SCK1 —** Serial clock for SSP1 (LPC1313FBD48/01 only).
PIO2_2/$\overline{\text{DCD}}$/MISO1	26[3]	yes	I/O	I; PU	**PIO2_2 —** General purpose digital input/output pin.
			I	-	**$\overline{\text{DCD}}$ —** Data Carrier Detect input for UART.
			I/O	-	**MISO1 —** Master In Slave Out for SSP1 (LPC1313FBD48/01 only).
PIO2_3/$\overline{\text{RI}}$/MOSI1	38[3]	yes	I/O	I; PU	**PIO2_3 —** General purpose digital input/output pin.
			I	-	**$\overline{\text{RI}}$ —** Ring Indicator input for UART.
			I/O	-	**MOSI1 —** Master Out Slave In for SSP1 (LPC1313FBD48/01 only).
PIO2_4	18[3]	yes	I/O	I; PU	**PIO2_4 —** General purpose digital input/output pin (LPC1342/43 only).
PIO2_4	19[3]	yes	I/O	I; PU	**PIO2_4 —** General purpose digital input/output pin (LPC1313 only).
PIO2_5	21[3]	yes	I/O	I; PU	**PIO2_5 —** General purpose digital input/output pin (LPC1342/43 only).
PIO2_5	20[3]	yes	I/O	I; PU	**PIO2_5 —** General purpose digital input/output pin (LPC1313 only).
PIO2_6	1[3]	yes	I/O	I; PU	**PIO2_6 —** General purpose digital input/output pin.
PIO2_7	11[3]	yes	I/O	I; PU	**PIO2_7 —** General purpose digital input/output pin.
PIO2_8	12[3]	yes	I/O	I; PU	**PIO2_8 —** General purpose digital input/output pin.
PIO2_9	24[3]	yes	I/O	I; PU	**PIO2_9 —** General purpose digital input/output pin.

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Table 3. LPC1313/42/43 LQFP48 pin description table *…continued*

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
PIO2_10	25[3]	yes	I/O	I; PU	**PIO2_10 —** General purpose digital input/output pin.
PIO2_11/SCK0	31[3]	yes	I/O	I; PU	**PIO2_11 —** General purpose digital input/output pin.
			I/O	-	**SCK0 —** Serial clock for SSP0.
PIO3_0/$\overline{\text{DTR}}$	36[3]	yes	I/O	I; PU	**PIO3_0 —** General purpose digital input/output pin.
			O	-	**$\overline{\text{DTR}}$ —** Data Terminal Ready output for UART (LPC1311/01 and LPC1313/01 only).
PIO3_1/$\overline{\text{DSR}}$	37[3]	yes	I/O	I; PU	**PIO3_1 —** General purpose digital input/output pin.
			I	-	**$\overline{\text{DSR}}$ —** Data Set Ready input for UART (LPC1311/01 and LPC1313/01 only).
PIO3_2/$\overline{\text{DCD}}$	43[3]	yes	I/O	I; PU	**PIO3_2 —** General purpose digital input/output pin.
			I	-	**$\overline{\text{DCD}}$ —** Data Carrier Detect input for UART (LPC1311/01 and LPC1313/01 only).
PIO3_3/$\overline{\text{RI}}$	48[3]	yes	I/O	I; PU	**PIO3_3 —** General purpose digital input/output pin.
			I	-	**$\overline{\text{RI}}$ —** Ring Indicator input for UART (LPC1311/01 and LPC1313/01 only).
PIO3_4	18[3]	no	I/O	I; PU	**PIO3_4 —** General purpose digital input/output pin (LPC1313 only).
PIO3_5	21[3]	no	I/O	I; PU	**PIO3_5 —** General purpose digital input/output pin (LPC1313 only).
USB_DM	19[6]	no	I/O	F	**USB_DM —** USB bidirectional D− line (LPC1342/43 only).
USB_DP	20[6]	no	I/O	F	**USB_DP —** USB bidirectional D+ line (LPC1342/43 only).
V_{DD}	8; 44	-	I	-	3.3 V supply voltage to the internal regulator, the external rail, and the ADC. Also used as the ADC reference voltage.
XTALIN	6[7]	-	I	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	7[7]	-	O	-	Output from the oscillator amplifier.
V_{SS}	5; 41	-	I	-	Ground.

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled (for V_{DD} = 3.3 V, pin is pulled up to 2.6 V for parts LPC1311/13/42/43 and pulled up to 3.3 V for parts LPC1311/01 and LPC1313/01); IA = inactive, no pull-up/down enabled; F = floating; floating pins, if not used, should be tied to ground or power to minimize power consumption.

[2] 5 V tolerant pad. See Figure 37 for pad characteristics. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 36).

[4] I^2C-bus pads compliant with the I^2C-bus specification for I^2C standard mode and I^2C Fast-mode Plus.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see Figure 36).

[6] Pad provides USB functions. It is designed in accordance with the USB specification, revision 2.0 (Full-speed and Low-speed mode only). This pad is not 5 V tolerant.

[7] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

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Table 4. LPC1311/13/42/43 HVQFN33 pin description table *…continued*

Symbol	Pin	Start logic input	Type	Reset state [1]	Description
PIO1_7/TXD/ CT32B0_MAT1	32[3]	yes	I/O	I; PU	**PIO1_7 —** General purpose digital input/output pin.
			O	-	**TXD —** Transmitter output for UART.
			O	-	**CT32B0_MAT1 —** Match output 1 for 32-bit timer 0.
PIO1_8/ CT16B1_CAP0	7[3]	yes	I/O	I; PU	**PIO1_8 —** General purpose digital input/output pin.
			I	-	**CT16B1_CAP0 —** Capture input 0 for 16-bit timer 1.
PIO1_9/ CT16B1_MAT0	12[3]	yes	I/O	I; PU	**PIO1_9 —** General purpose digital input/output pin.
			O	-	**CT16B1_MAT0 —** Match output 0 for 16-bit timer 1.
PIO1_10/AD6/ CT16B1_MAT1	20[5]	yes	I/O	I; PU	**PIO1_10 —** General purpose digital input/output pin.
			I	-	**AD6 —** A/D converter, input 6.
			O	-	**CT16B1_MAT1 —** Match output 1 for 16-bit timer 1.
PIO1_11/AD7	27[5]	yes	I/O	I; PU	**PIO1_11 —** General purpose digital input/output pin.
			I	-	**AD7 —** A/D converter, input 7.
PIO2_0/$\overline{\text{DTR}}$	1[3]	yes	I/O	I; PU	**PIO2_0 —** General purpose digital input/output pin.
			O	-	**$\overline{\text{DTR}}$ —** Data Terminal Ready output for UART.
PIO3_2	28[3]	yes	I/O	I; PU	**PIO3_2 —** General purpose digital input/output pin.
PIO3_4	13[3]	no	I/O	I; PU	**PIO3_4 —** General purpose digital input/output pin (LPC1311/13 only).
PIO3_5	14[3]	no	I/O	I; PU	**PIO3_5 —** General purpose digital input/output pin (LPC1311/13 only).
USB_DM	13[6]	no	I/O	F	**USB_DM —** USB bidirectional D− line (LPC1342/43 only).
USB_DP	14[6]	no	I/O	F	**USB_DP —** USB bidirectional D+ line (LPC1342/43 only).
V_{DD}	6; 29	-	I	-	3.3 V supply voltage to the internal regulator, the external rail, and the ADC. Also used as the ADC reference voltage.
XTALIN	4[7]	-	I	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	5[7]	-	O	-	Output from the oscillator amplifier.
V_{SS}	33	-	-	-	Thermal pad. Connect to ground.

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled (for V_{DD} = 3.3 V, pin is pulled up to 2.6 V for parts LPC1311/13/42/43 and pulled up to 3.3 V for parts LPC1311/01 and LPC1313/01); IA = inactive, no pull-up/down enabled. F = floating; floating pins, if not used, should be tied to ground or power to minimize power consumption.

[2] 5 V tolerant pad. See Figure 37 for pad characteristics. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see Figure 36).

[4] I^2C-bus pads compliant with the I^2C-bus specification for I^2C standard mode and I^2C Fast-mode Plus.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled, and the pin is not 5 V tolerant (see Figure 36).

[6] Pad provides USB functions. It is designed in accordance with the USB specification, revision 2.0 (Full-speed and Low-speed mode only). This pad is not 5 V tolerant.

[7] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.

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7.6.1 Features

- Controls system exceptions and peripheral interrupts.
- On the LPC1311/13/42/43, the NVIC supports up to 17 vectored interrupts. In addition, up to 40 of the individual GPIO inputs are NVIC-vector capable.
- 8 programmable interrupt priority levels, with hardware priority level masking
- Relocatable vector table.
- Software interrupt generation.

7.6.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Any GPIO pin (total of up to 42 pins) regardless of the selected function, can be programmed to generate an interrupt on a level, or rising edge or falling edge, or both.

7.7 IOCONFIG block

The IOCONFIG block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on-chip peripherals.

Peripherals should be connected to the appropriate pins prior to being activated and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

7.8 Fast general purpose parallel I/O

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC1311/13/42/43 use accelerated GPIO functions:

- GPIO block is a dedicated AHB peripheral so that the fastest possible I/O timing can be achieved.
- Entire port value can be written in one instruction.

Additionally, any GPIO pin (total of up to 42 pins) providing a digital function can be programmed to generate an interrupt on a level, a rising or falling edge, or both.

7.8.1 Features

- Bit level port registers allow a single instruction to set or clear any number of bits in one write operation.
- Direction control of individual bits.
- All I/O default to inputs with pull-up resistors enabled after reset with the exception of the I^2C-bus pins PIO0_4 and PIO0_5.
- Pull-up/pull-down resistor configuration can be programmed through the IOCONFIG block for each GPIO pin.

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- On the LPC1311/13/42/43, all GPIO pins (except PIO0_4 and PIO0_5) are pulled up to 2.6 V (V_{DD} = 3.3 V) if their pull-up resistor is enabled in the IOCONFIG block.
- On the LPC1311/01 and LPC1313/01, all GPIO pins (except PIO0_4 and PIO0_5) are pulled up to 3.3 V (V_{DD} = 3.3 V) if their pull-up resistor is enabled in the IOCONFIG block.

7.9 USB interface (LPC1342/43 only)

The Universal Serial Bus (USB) is a 4-wire bus that supports communication between a host and one or more (up to 127) peripherals. The host controller allocates the USB bandwidth to attached devices through a token-based protocol. The bus supports hot-plugging and dynamic configuration of the devices. All transactions are initiated by the host controller.

The LPC1342/43 USB interface is a device controller with on-chip PHY for device functions.

7.9.1 Full-speed USB device controller

The device controller enables 12 Mbit/s data exchange with a USB Host controller. It consists of a register interface, serial interface engine, and endpoint buffer memory. The serial interface engine decodes the USB data stream and writes data to the appropriate endpoint buffer. The status of a completed USB transfer or error condition is indicated via status registers. An interrupt is also generated if enabled.

7.9.1.1 Features

- Dedicated USB PLL available.
- Fully compliant with *USB 2.0 specification (full speed)*.
- Supports 10 physical (5 logical) endpoints with up to 64 bytes buffer RAM per endpoint (see Table 5).
- Supports Control, Bulk, Isochronous, and Interrupt endpoints.
- Supports SoftConnect feature.
- Double buffer implementation for Bulk and Isochronous endpoints.

Table 5. USB device endpoint configuration

Logical endpoint	Physical endpoint	Endpoint type	Direction	Packet size (byte)	Double buffer
0	0	Control	out	64	no
0	1	Control	in	64	no
1	2	Interrupt/Bulk	out	64	no
1	3	Interrupt/Bulk	in	64	no
2	4	Interrupt/Bulk	out	64	no
2	5	Interrupt/Bulk	in	64	no
3	6	Interrupt/Bulk	out	64	yes
3	7	Interrupt/Bulk	in	64	yes
4	8	Isochronous	out	512	yes
4	9	Isochronous	in	512	yes

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7.18.5 Power control

The LPC1311/13/42/43 support a variety of power control features. There are three special modes of processor power reduction: Sleep mode, Deep-sleep mode, and Deep power-down mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals, allowing fine tuning of power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

7.18.5.1 Power profiles (LPC1300L series, LPC1311/01 and LPC1313/01 only)

The power consumption in Active and Sleep modes can be optimized for the application through simple calls to the power profile. The power configuration routine configures the LPC1311/01 and the LPC1313/01 for one of the following power modes:

- Default mode corresponding to power configuration after reset.
- CPU performance mode corresponding to optimized processing capability.
- Efficiency mode corresponding to optimized balance of current consumption and CPU performance.
- Low-current mode corresponding to lowest power consumption.

In addition, the power profile includes routines to select the optimal PLL settings for a given system clock and PLL input clock.

7.18.5.2 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

7.18.5.3 Deep-sleep mode

In Deep-sleep mode, the chip is in Sleep mode, and in addition all analog blocks are shut down. As an exception, the user has the option to keep the watchdog oscillator and the BOD circuit running for self-timed wake-up and BOD protection. Deep-sleep mode allows for additional power savings.

Up to 40 pins total can serve as external wake-up pins to the start logic to wake up the chip from Deep-sleep mode (see Section 7.19.1).

Unless the watchdog oscillator is selected to run in Deep-sleep mode, the clock source should be switched to IRC before entering Deep-sleep mode, because the IRC can be switched on and off glitch-free.

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There are three levels of Code Read Protection:

1. CRP1 disables access to chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors can not be erased.
2. CRP2 disables access to chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected fully disables any access to chip via the SWD pins and the ISP. This mode effectively disables ISP override using PIO0_1 pin, too. It is up to the user's application to provide (if needed) flash update mechanism using IAP calls or call reinvoke ISP command to enable flash update via UART.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

7.19.5 Boot loader

The boot loader controls initial operation after reset and also provides the means to program the flash memory. This could be initial programming of a blank device, erasure and re-programming of a previously programmed device, or programming of the flash memory by the application program in a running system.

The boot loader code is executed every time the part is reset or powered up. The loader can either execute the ISP command handler or the user application code, or, on the LPC1342/43, it can program the flash image via an attached MSC device through USB (Windows operating system only). A LOW level during reset applied to the PIO0_1 pin is considered as an external hardware request to start the ISP command handler or the USB device enumeration. The state of PIO0_3 determines whether the UART or USB interface will be used (LPC1342/43 only).

7.19.6 APB interface

The APB peripherals are located on one APB bus.

7.19.7 AHB-Lite

The AHB-Lite connects the instruction (I-code) and data (D-code) CPU buses of the ARM Cortex-M3 to the flash memory, the main static RAM, and the boot ROM.

7.19.8 External interrupt inputs

All GPIO pins can be level or edge sensitive interrupt inputs. In addition, start logic inputs serve as external interrupts (see Section 7.19.1).

7.19.9 Memory mapping control

The Cortex-M3 incorporates a mechanism that allows remapping the interrupt vector table to alternate locations in the memory map. This is controlled via the Vector Table Offset Register contained in the NVIC.

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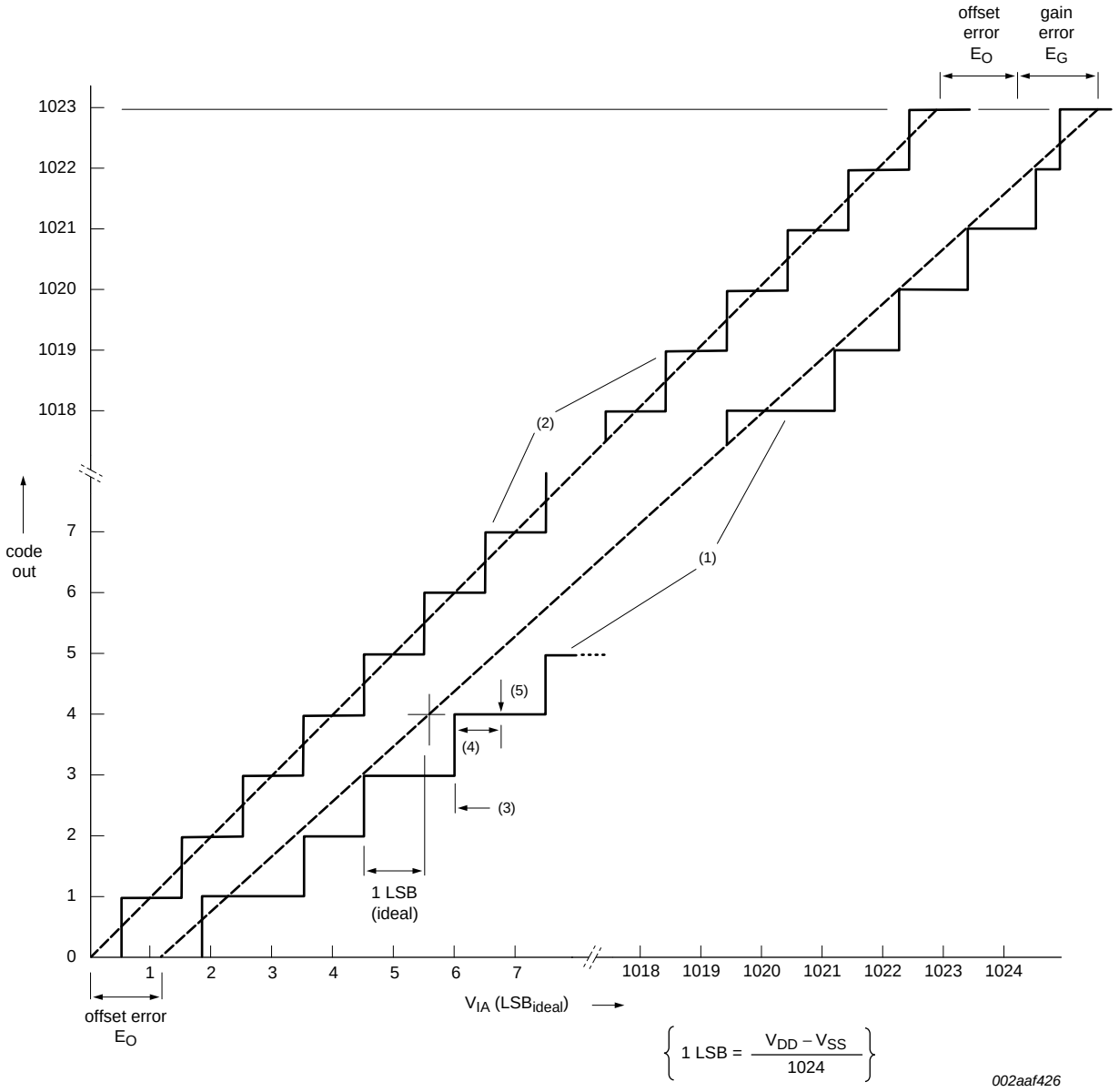

(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 8. ADC characteristics

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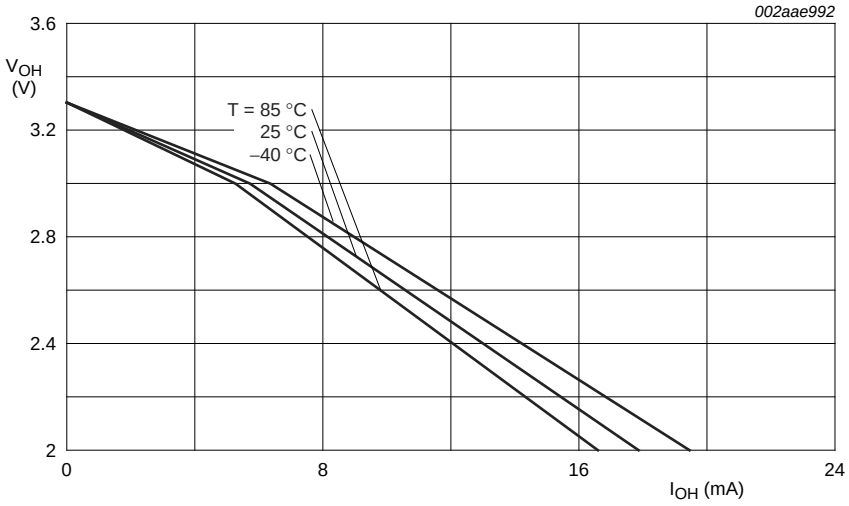
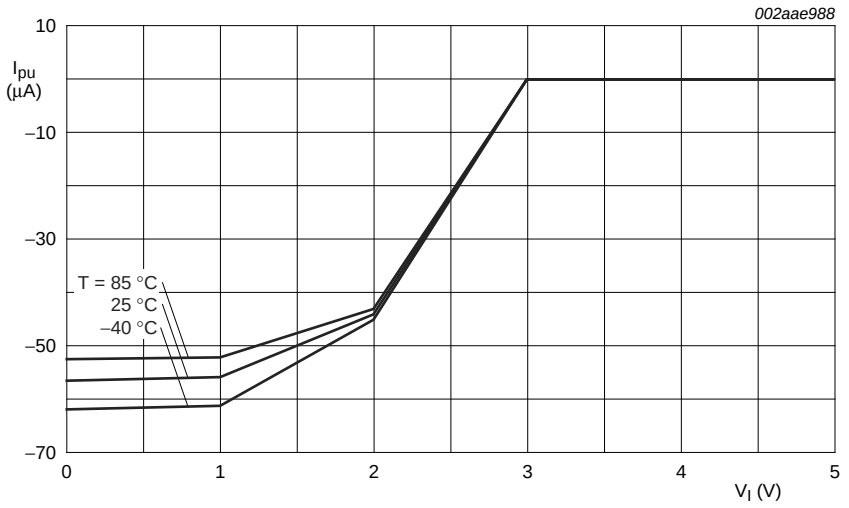


Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 22. Typical HIGH-level output voltage V_{OH} versus HIGH-level output source current I_{OH}



Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 23. Typical pull-up current I_{pu} versus input voltage V_i

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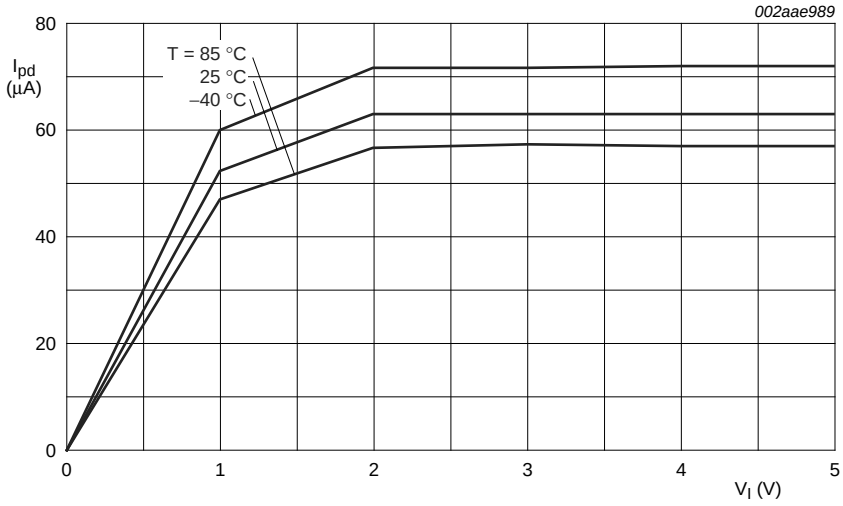

Conditions: V_{DD} = 3.3 V; standard port pins.

Fig 24. Typical pull-down current I_{pd} versus input voltage V_i

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10.3 External clock

Table 14. Dynamic characteristic: external clock
T_{amb} = –40 °C to +85 °C; V_{DD} over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
f_{osc}	oscillator frequency		1	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	1000	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

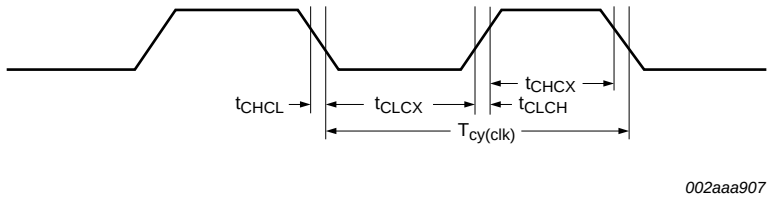

Fig 26. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

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10.4 Internal oscillators

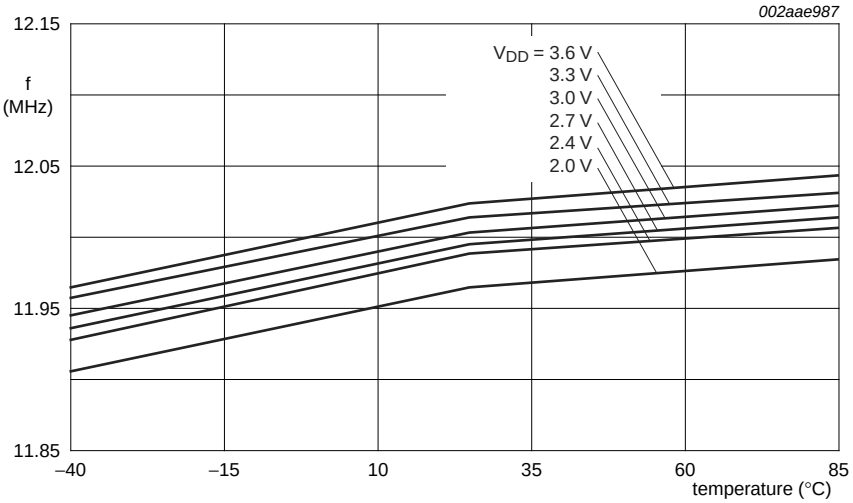
Table 15. Dynamic characteristics: IRC

T_{amb} = –40 °C to +85 °C; 2.7 V ≤ V_{DD} ≤ 3.6 V[1].

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	-	11.88	12	12.12	MHz

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.



Conditions: Frequency values are typical values. 12 MHz ± 1 % accuracy is guaranteed for 2.7 V ≤ V_{DD} ≤ 3.6 V and T_{amb} = –40 °C to +85 °C. Variations between parts may cause the IRC to fall outside the 12 MHz ± 1 % accuracy specification for voltages below 2.7 V.

Fig 27. Internal RC oscillator frequency f versus temperature

Table 16. Dynamic characteristics: Watchdog oscillator

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$f_{osc(int)}$	internal oscillator frequency	DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register;	[2][3]	-	7.8	-	kHz
		DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register	[2][3]	-	1700	-	kHz

[1] Typical ratings are not guaranteed. The values listed are at nominal supply voltages.

[2] The typical frequency spread over processing and temperature (T_{amb} = –40 °C to +85 °C) is ±40 %.

[3] See the *LPC13xx user manual.*

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10.5 I/O pins

Table 17. Dynamic characteristics: I/O pins[1]
T_{amb} = –40 °C to +85 °C; 3.0 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	pin configured as output	3.0	-	5.0	ns
t_f	fall time	pin configured as output	2.5	-	5.0	ns

[1] Applies to standard port pins and $\overline{\text{RESET}}$ pin.

10.6 I²C-bus

Table 18. Dynamic characteristic: I²C-bus pins[1]
T_{amb} = –40 °C to +85 °C.[2]

Symbol	Parameter		Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency		Standard-mode	0	100	kHz
			Fast-mode	0	400	kHz
			Fast-mode Plus	0	1	MHz
t_f	fall time	[4][5][6][7]	of both SDA and SCL signals	-	300	ns
			Standard-mode			
			Fast-mode	$20 + 0.1 \times C_b$	300	ns
			Fast-mode Plus	-	120	ns
t_{LOW}	LOW period of the SCL clock		Standard-mode	4.7	-	µs
			Fast-mode	1.3	-	µs
			Fast-mode Plus	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		Standard-mode	4.0	-	µs
			Fast-mode	0.6	-	µs
			Fast-mode Plus	0.26	-	µs
$t_{HD;DAT}$	data hold time	[3][4][8]	Standard-mode	0	-	µs
			Fast-mode	0	-	µs
			Fast-mode Plus	0	-	µs
$t_{SU;DAT}$	data set-up time	[9][10]	Standard-mode	250	-	ns
			Fast-mode	100	-	ns
			Fast-mode Plus	50	-	ns

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

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Table 21. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) low frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
1 MHz - 5 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 300 Ω	39 pF, 39 pF
	30 pF	< 300 Ω	57 pF, 57 pF
5 MHz - 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz - 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz - 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

Table 22. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) high frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz - 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz - 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

11.3 XTAL Printed-Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{x1}, C_{x2}, and C_{x3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plain. Loops must be made as small as possible in order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Values of C_{x1} and C_{x2} should be chosen smaller accordingly to the increase in parasitics of the PCB layout.

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11.5 Reset pad configuration

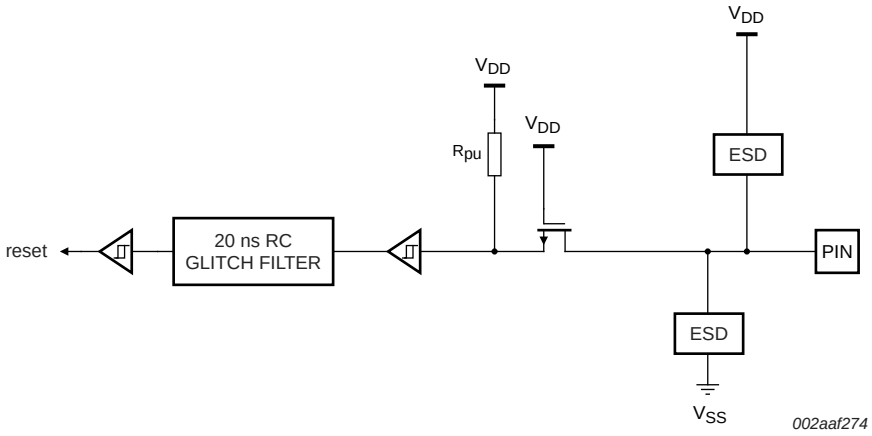

Fig 37. Reset pad configuration

11.6 ADC usage notes

The following guidelines show how to increase the performance of the ADC in a noisy environment beyond the ADC specifications listed in Table 8:

- The ADC input trace must be short and as close as possible to the LPC1311/13/42/43 chip.
- The ADC input traces must be shielded from fast switching digital signals and noisy power supply lines.
- Because the ADC and the digital core share the same power supply, the power supply line must be adequately filtered.
- To improve the ADC performance in a very noisy environment, put the device in Sleep mode during the ADC conversion.

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11.7 ElectroMagnetic Compatibility (EMC)

Radiated emission measurements according to the IEC61967-2 standard using the TEM-cell method are shown for the LPC1343FBD48 in Table 23.

Table 23. ElectroMagnetic Compatibility (EMC) for part LPC1343FBD48 (TEM-cell method)
V_{DD} = 3.3 V; T_{amb} = 25 °C.

Parameter	Frequency band	System clock =				Unit
		12 MHz	24 MHz	48 MHz	72 MHz	
Input clock: IRC (12 MHz)						
maximum peak level	150 kHz - 30 MHz	–6	–5	–7	–7	dBµV
	30 MHz - 150 MHz	–1	+3	+9	+13	dBµV
	150 MHz - 1 GHz	+3	+7	+15	+19	dBµV
IEC level[1]	-	O	N	M	L	-
Input clock: crystal oscillator (12 MHz)						
maximum peak level	150 kHz - 30 MHz	-5	–5	–7	–7	dBµV
	30 MHz - 150 MHz	0	+4	+9	+13	dBµV
	150 MHz - 1 GHz	3	+8	+15	+20	dBµV
IEC level[1]	-	O	N	M	L	-

[1] IEC levels refer to Appendix D in the IEC61967-2 Specification.

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Footprint information for reflow soldering of HVQFN33 package

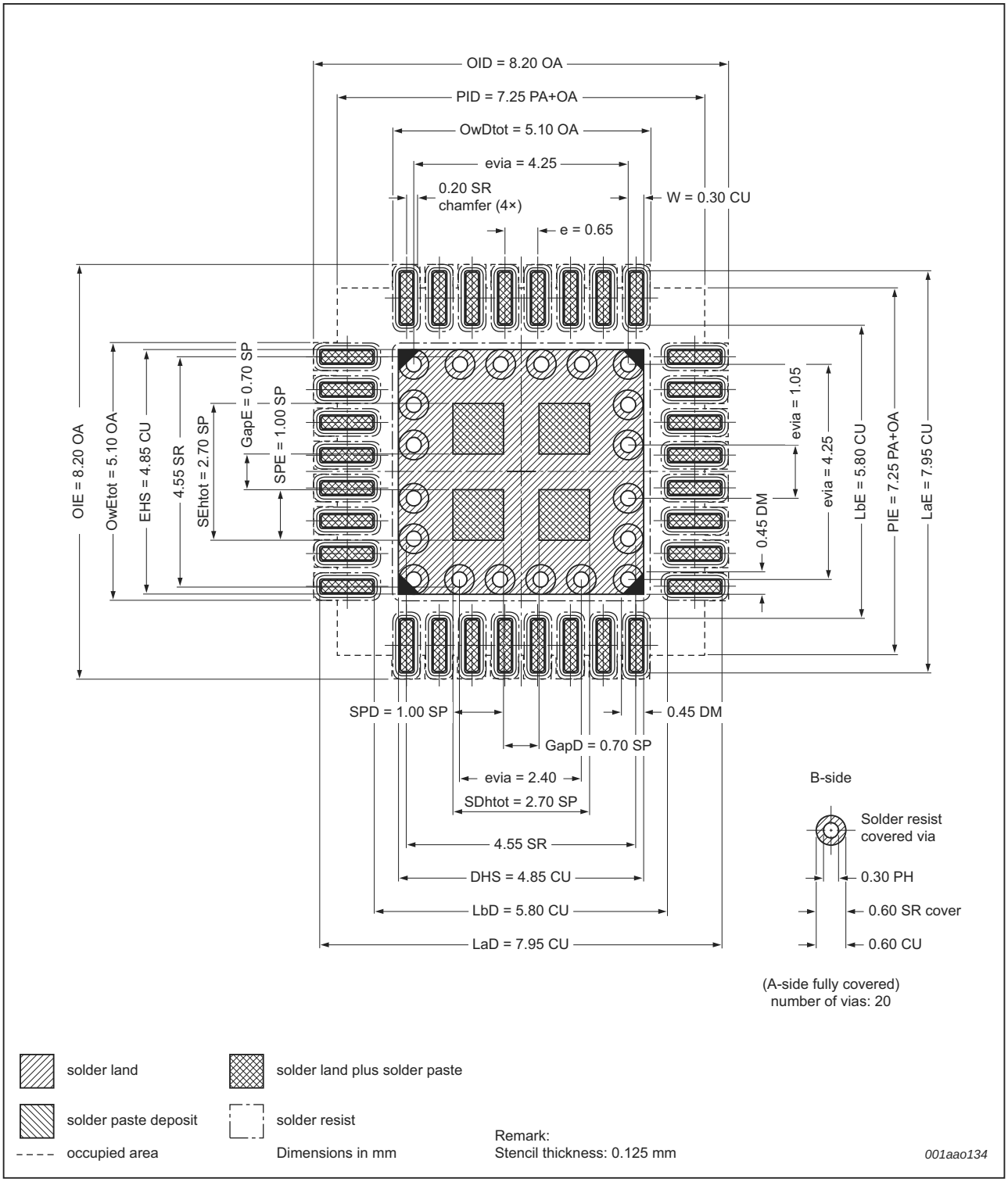

Fig 41. Reflow soldering of the HVQFN33 package

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