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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, I²S, POR, PWM, WDT
Number of I/O	109
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	12K x 8
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 40x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	132-UFBGA
Supplier Device Package	132-UFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l151qdh6

- **Stop** mode without RTC

  Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks are stopped, the PLL, MSI RC, HSI and LSI RC, LSE and HSE crystal oscillators are disabled. The voltage regulator is in the low-power mode. The device can be woken up from Stop mode by any of the EXTI line, in 8 µs. The EXTI line source can be one of the 16 external lines. It can be the PVD output, the Comparator 1 event or Comparator 2 event (if internal reference voltage is on). It can also be wakened by the USB wakeup.
- **Standby** mode with RTC

  Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI RC and HSE crystal oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC_CSR).

  The device exits Standby mode in 60 µs when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.
- **Standby** mode without RTC

  Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC_CSR).

  The device exits Standby mode in 60 µs when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped automatically by entering Stop or Standby mode.

Table 3. Functionalities depending on the operating power supply range

	Functionalities depending on the operating power supply range			
Operating power supply range	**DAC and ADC operation**	**USB**	**Dynamic voltage scaling range**	**I/O operation**
V_{DD}= V_{DDA} = 1.65 to 1.71 V	Not functional	Not functional	Range 2 or Range 3	Degraded speed performance
V_{DD}=V_{DDA}= 1.71 to 1.8 V(1)	Not functional	Not functional	Range 1, Range 2 or Range 3	Degraded speed performance
V_{DD}=V_{DDA}= 1.8 to 2.0 V(1)	Conversion time up to 500 Ksps	Not functional	Range 1, Range 2 or Range 3	Degraded speed performance

Table 3. Functionalities depending on the operating power supply range (continued)

	Functionalities depending on the operating power supply range			
Operating power supply range	**DAC and ADC operation**	**USB**	**Dynamic voltage scaling range**	**I/O operation**
V_{DD}=V_{DDA} = 2.0 to 2.4 V	Conversion time up to 500 Ksps	Functional(2)	Range 1, Range 2 or Range 3	Full speed operation
V_{DD}=V_{DDA} = 2.4 to 3.6 V	Conversion time up to 1 Msps	Functional(2)	Range 1, Range 2 or Range 3	Full speed operation

1. CPU frequency changes from initial to final must respect “F_{CPU} initial < 4*F_{CPU} final” to limit V_{CORE} drop due to current consumption peak when frequency increases. It must also respect 5 µs delay between two changes. For example to switch from 4.2 MHz to 32 MHz, the user can switch from 4.2 MHz to 16 MHz, wait 5 µs, then switch from 16 MHz to 32 MHz.
2. Should be USB compliant from I/O voltage standpoint, the minimum V_{DD} is 3.0 V.

Table 4. CPU frequency range depending on dynamic voltage scaling

CPU frequency range	Dynamic voltage scaling range
16 MHz to 32 MHz (1ws) 32 kHz to 16 MHz (0ws)	Range 1
8 MHz to 16 MHz (1ws) 32 kHz to 8 MHz (0ws)	Range 2
2.1MHz to 4.2 MHz (1ws) 32 kHz to 2.1 MHz (0ws)	Range 3

The operational amplifiers feature:

- Low input bias current
- Low offset voltage
- Low-power mode
- Rail-to-rail input

3.14 Ultra-low-power comparators and reference voltage

The STM32L151xD and STM32L152xD devices embed two comparators sharing the same current bias and reference voltage. The reference voltage can be internal or external (coming from an I/O).

- One comparator with fixed threshold
- One comparator with rail-to-rail inputs, fast or slow mode. The threshold can be one of the following:
  – DAC output
  – External I/O
  – Internal reference voltage (V_{REFINT}) or a sub-multiple (1/4, 1/2, 3/4)

Both comparators can wake up from Stop mode, and be combined into a window comparator.

The internal reference voltage is available externally via a low-power / low-current output buffer (driving current capability of 1 µA typical).

3.15 System configuration controller and routing interface

The system configuration controller provides the capability to remap some alternate functions on different I/O ports.

The highly flexible routing interface allows the application firmware to control the routing of different I/Os to the TIM2, TIM3 and TIM4 timer input captures. It also controls the routing of internal analog signals to ADC1, COMP1 and COMP2 and the internal reference voltage V_{REFINT}.

3.16 Touch sensing

The STM32L151xD and STM32L152xD devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 34 capacitive sensing channels distributed over 11 analog I/O groups. Both software and timer capacitive sensing acquisition modes are supported.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. The capacitive sensing acquisition only requires few external components to

3.18.2 Universal synchronous/asynchronous receiver transmitter (USART)

The three USART and two UART interfaces are able to communicate at speeds of up to 4 Mbit/s. They support IrDA SIR ENDEC and have LIN Master/Slave capability. The three USARTs provide hardware management of the CTS and RTS signals and are ISO 7816 compliant.

All USART/UART interfaces can be served by the DMA controller.

3.18.3 Serial peripheral interface (SPI)

Up to three SPIs are able to communicate at up to 16 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

The SPIs can be served by the DMA controller.

3.18.4 Inter-integrated sound (I^2S)

Two standard I2S interfaces (multiplexed with SPI2 and SPI3) are available. They can operate in master or slave mode, and can be configured to operate with a 16-/32-bit resolution as input or output channels. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

The I2Ss can be served by the DMA controller.

3.18.5 SDIO

An SD/SDIO/MMC host interface is available, that supports MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit.

The interface allows data transfer at up to 24 MHz in 8-bit mode, and is compliant with the SD Memory Card Specification Version 2.0.

The SDIO Card Specification Version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDIO/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

In addition to SD/SDIO/MMC, this interface is fully compliant with the CE-ATA digital protocol Rev1.1.

3.18.6 Universal serial bus (USB)

The STM32L151xD and STM32L152xD devices embed a USB device peripheral compatible with the USB full-speed 12 Mbit/s. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and supports suspend/resume. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

3.20 Development support

3.20.1 Serial wire JTAG debug port (SWJ-DP)

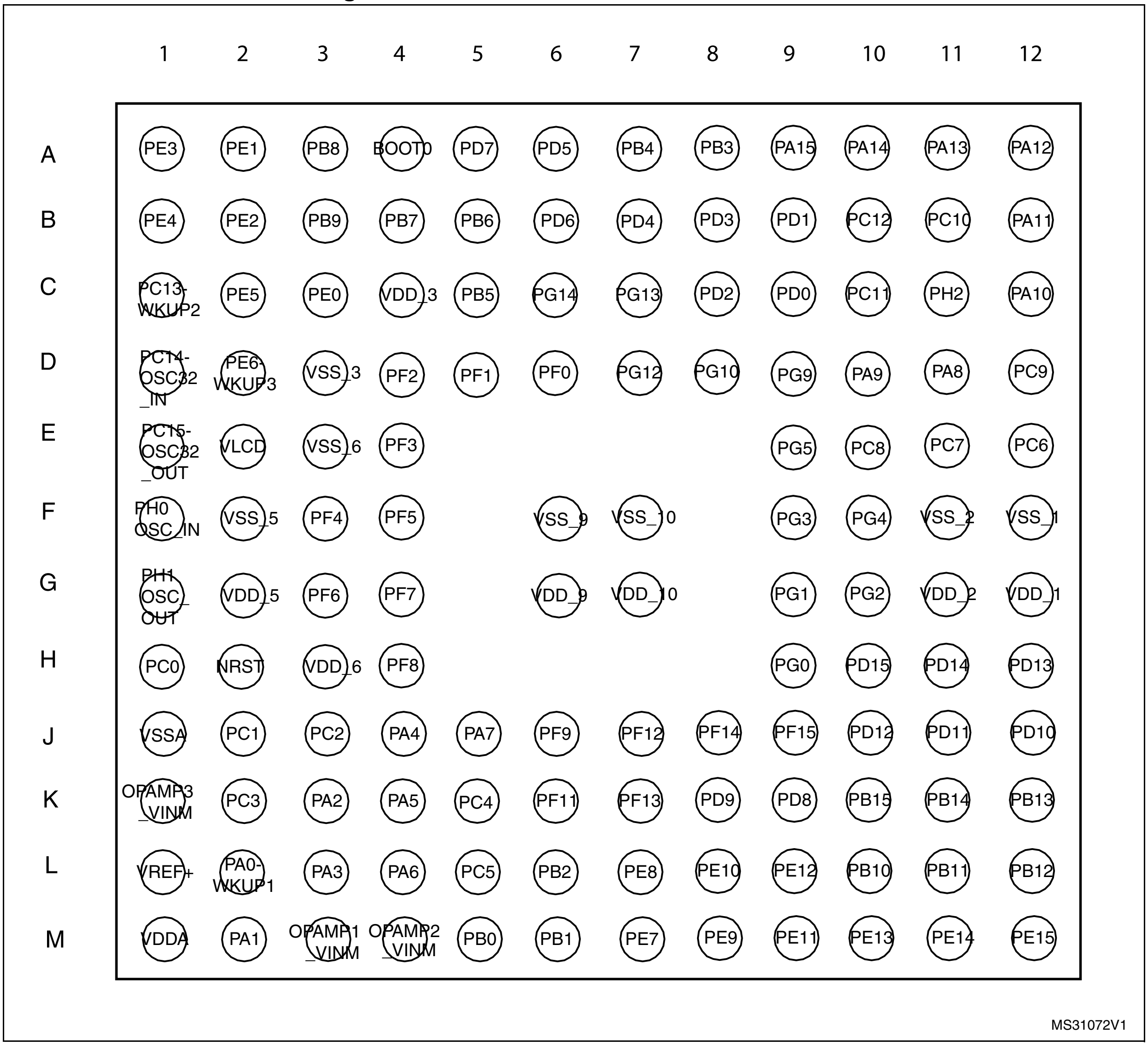
The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG JTMS and JTCK pins are shared with SWDAT and SWCLK, respectively, and a specific sequence on the JTMS pin is used to switch between JTAG-DP and SW-DP.

The JTAG port can be permanently disabled with a JTAG fuse.

3.20.2 Embedded Trace Macrocell™

The ARM® Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32L151xD and STM32L152xD device through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using USB, Ethernet, or any other high-speed channel. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer running debugger software. TPA hardware is commercially available from common development tool vendors. It operates with third party debugger software tools.

Figure 4. STM32L15xQD UFBGA132 ballout



1. This figure shows the package top view.

Table 8. STM32L151xD and STM32L152xD pin definitions (continued)

Pins					Pin name	Pin Type[1]	I / O structure	Main function[2] (after reset)	Pin functions	
LQFP144	UFBGA132	LQFP100	LQFP64	WLCSP64					Alternate functions	Additional functions
-	J5	-	-	-	PA7	I/O	FT	PA7	TIM3_CH2/TIM11_CH1/ SPI1_MOSI/ LCD_SEG4	ADC_IN7/ COMP1_INP
-	M4	-	-	-	OPAMP2_VINM	I	TC	OPAMP2_VINM	-	-
44	K5	33	24	H6	PC4	I/O	FT	PC4	LCD_SEG22	ADC_IN14/ COMP1_INP
45	L5	34	25	H5	PC5	I/O	FT	PC5	LCD_SEG23	ADC_IN15/ COMP1_INP
46	M5	35	26	H4	PB0	I/O	TC	PB0	TIM3_CH3/LCD_SEG5	ADC_IN8/ COMP1_INP/ OPAMP2_VOUT/ VREF_OUT
47	M6	36	27	F4	PB1	I/O	FT	PB1	TIM3_CH4/LCD_SEG6	ADC_IN9/ COMP1_INP/ VREF_OUT
48	L6	37	28	H3	PB2	I/O	FT	PB2/ BOOT1	BOOT1	ADC_IN0b
49	K6	-	-	-	PF11	I/O	FT	PF11	-	ADC_IN1b
50	J7	-	-	-	PF12	I/O	FT	PF12	FSMC_A6	ADC_IN2b
51	E3	-	-	-	V_{SS_6}	S	-	V_{SS_6}	-	-
52	H3	-	-	-	V_{DD_6}	S	-	V_{DD_6}	-	-
53	K7	-	-	-	PF13	I/O	FT	PF13	FSMC_A7	ADC_IN3b
54	J8	-	-	-	PF14	I/O	FT	PF14	FSMC_A8	ADC_IN6b
55	J9	-	-	-	PF15	I/O	FT	PF15	FSMC_A9	ADC_IN7b
56	H9	-	-	-	PG0	I/O	FT	PG0	FSMC_A10	ADC_IN8b
57	G9	-	-	-	PG1	I/O	FT	PG1	FSMC_A11	ADC_IN9b
58	M7	38	-	-	PE7	I/O	TC	PE7	FSMC_D4	ADC_IN22/ COMP1_INP
59	L7	39	-	-	PE8	I/O	TC	PE8	FSMC_D5	ADC_IN23/ COMP1_INP
60	M8	40	-	-	PE9	I/O	TC	PE9	TIM2_CH1_ETR /FSMC_D6	ADC_IN24/ COMP1_INP

Table 9. Alternate function input/output (continued)

Port name	Digital alternate function number														
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFIO6	AFIO7	AFIO8	..	AFIO11	AFIO12	..	AFIO14	AFIO15
	Alternate function														
	SYSTEM	TIM2	TIM3/4/5	TIM9/ 10/11	I2C1/2	SPI1/2	SPI3	USART1/2/3	UART4/5		LCD	FSMC/ SDIO		CPRI	SYSTEM
PD8	-	-	-	-	-	-	-	USART3_TX	-		SEG28	D13/DA13		TIMx_IC1	EVENT OUT
PD9	-	-	-	-	-	-	-	USART3_RX	-		SEG29	D14/DA14		TIMx_IC2	EVENT OUT
PD10	-	-	-	-	-	-	-	USART3_CK	-		SEG30	D15/DA15		TIMx_IC3	EVENT OUT
PD11	-	-	-	-	-	-	-	USART3_CTS	-		SEG31	A16		TIMx_IC4	EVENT OUT
PD12	-	-	TIM4_CH1	-	-	-	-	USART3_RTS	-		SEG32	A17		TIMx_IC1	EVENT OUT
PD13	-	-	TIM4_CH2	-	-	-	-	-	-		SEG33	A18		TIMx_IC2	EVENT OUT
PD14	-	-	TIM4_CH3	-	-	-	-	-	-		SEG34	D0/DA0		TIMx_IC3	EVENT OUT
PD15	-	-	TIM4_CH4	-	-	-	-	-	-		SEG35	D1/DA1		TIMx_IC4	EVENT OUT
PE0	-	-	TIM4_ETR	TIM10_CH1	-	-	-	-	-		SEG36	NBL0		TIMx_IC1	EVENT OUT
PE1	-	-	-	TIM11_CH1	-	-	-	-	-		SEG37	NBL1		TIMx_IC2	EVENT OUT
PE2	TRACECK	-	TIM3_ETR	-	-	-	-	-	-		SEG 38	A23		TIMx_IC3	EVENT OUT
PE3	TRACED0	-	TIM3_CH1	-	-	-	-	-	-		SEG 39	A19		TIMx_IC4	EVENT OUT
PE4	TRACED1	-	TIM3_CH2	-	-	-	-	-	-		-	A20		TIMx_IC1	EVENT OUT
PE5	TRACED2	-	-	TIM9_CH1	-	-	-	-	-		-	A21		TIMx_IC2	EVENT OUT
PE6-WKUP3	TRACED3	-	-	TIM9_CH2	-	-	-	-	-		-	-		TIMx_IC3	EVENT OUT

6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 10: Voltage characteristics*, *Table 11: Current characteristics*, and *Table 12: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 10. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
$V_{DD}–V_{SS}$	External main supply voltage (including V_{DDA} and V_{DD})(1)	–0.3	4.0	V
V_{IN}(2)	Input voltage on five-volt tolerant pin	V_{SS} –0.3	V_{DD}+4.0	
	Input voltage on any other pin	V_{SS} –0.3	4.0	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{SSX} – V_{SS}\rvert$	Variations between all different ground pins(3)	-	50	
$V_{REF+} – V_{DDA}$	Allowed voltage difference for $V_{REF+} > V_{DDA}$	-	0.4	V
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.12*		

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 11* for maximum allowed injected current values.
3. Include V_{REF-} pin.

Table 11. Current characteristics

Symbol	Ratings	Max.	Unit
$I_{VDD(\Sigma)}$	Total current into sum of all V_{DD_x} power lines (source)(1)	100	mA
$I_{VSS(\Sigma)}$(2)	Total current out of sum of all V_{SS_x} ground lines (sink)(1)	100	
$I_{VDD(PIN)}$	Maximum current into each V_{DD_x} power pin (source)(1)	70	
$I_{VSS(PIN)}$	Maximum current out of each VSS_x ground pin (sink)(1)	-70	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current sourced by any I/O and control pin	- 25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all IOs and control pins(2)	60	
	Total output current sourced by sum of all IOs and control pins(2)	-60	
$I_{INJ(PIN)}$ (3)	Injected current on five-volt tolerant I/O(4), RST and B pins	-5/+0	
	Injected current on any other pin (5)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(6)	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Negative injection disturbs the analog performance of the device. See note in *Section 6.3.19*.

Table 17. Current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions		f_{HCLK} [MHz]	Typ	Max (1)	Unit
I_{DD} (Run from Flash)	Supply current in Run mode code executed from Flash	$f_{HSE} = f_{HCLK}$ up to 16MHz, included $f_{HSE} = f_{HCLK}/2$ above 16 MHz (PLL ON)(2)	Range3, V_{CORE}=1.2 V VOS[1:0]=11	1	290	500	µA
				2	505	750	
				4	955	1200	
			Range2, V_{CORE}=1.5 V VOS[1:0]=10	4	1.15	1.6	mA
				8	2.3	2.9	
				16	4.25	5.2	
			Range1, V_{CORE}=1.8 V VOS[1:0]=01	8	2.65	3.5	
				16	5.35	6.5	
				32	10.5	12	
		HSI clock source (16 MHz)	Range2, V_{CORE}=1.5 V VOS[1:0]=10	16	4.35	5.2	
			Range1, V_{CORE}=1.8 V VOS[1:0]=01	32	10.5	12.3	
		MSI clock, 65 kHZ	Range3, V_{CORE}=1.2 V VOS[1:0]=11	0.065	46	130	µA
		MSI clock, 524 kHZ		0.524	160	250	
		MSI clock, 4.2 MHZ		4.2	965	1200	

1. Guaranteed by characterization results, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 18. Current consumption in Run mode, code with data processing running from RAM

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max	Unit
I_{DD} (Run from RAM)	Supply current in Run mode code executed from RAM	$f_{HSE} = f_{HCLK}$ up to 16 MHz, included $f_{HSE} = f_{HCLK}/2$ above 16MHz (PLL ON)[1]	Range3, V_{CORE}=1.2 V VOS[1:0]=11	1	230	470	µA
				2	415	780	
				4	800	1200	
			Range2, V_{CORE}=1.5 V VOS[1:0]=10	4	0.935	1.5	mA
				8	1.9	3	
				16	3.75	5	
			Range1, V_{CORE}=1.8 V VOS[1:0]=01	8	2.25	3.5	
				16	4.45	5.55	
				32	9.05	10.9	
		HSI clock source (16 MHz)	Range2, V_{CORE}=1.5 V VOS[1:0]=10	16	3.75	4.8	
			Range1, V_{CORE}=1.8 V VOS[1:0]=01	32	8.95	11.7	
		MSI clock, 65 kHZ	Range3, V_{CORE}=1.2 V VOS[1:0]=11	0.065	43.5	100	µA
		MSI clock, 524 kHZ		0.524	135	215	
		MSI clock, 4.2 MHZ		4.2	835	1100	

1. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 24. Peripheral current consumption(1) (continued)

Peripheral		Typical consumption, V_{DD} = 3.0 V, T_A = 25 °C				Unit
		Range 1, V_{CORE}= 1.8 V VOS[1:0] = 01	Range 2, V_{CORE}= 1.5 V VOS[1:0] = 10	Range 3, V_{CORE}= 1.2 V VOS[1:0] = 11	Low-power sleep and run	
APB2	SYSCFG & RI	3.5	2.9	2.4	2.9	µA/MHz (f_{HCLK})
	TIM9	9.0	7.4	5.8	7.4	
	TIM10	7.1	5.8	4.6	5.8	
	TIM11	6.5	5.3	4.3	5.3	
	ADC(2)	11.0	9.1	7.2	9.1	
	SDIO	28.4	24.2	19.1	24.2	
	SPI1	5.1	4.2	3.3	4.2	
	USART1	9.4	7.8	6.1	7.8	
AHB	GPIOA	7.3	6.1	4.8	6.1	
	GPIOB	7.5	6.1	4.8	6.1	
	GPIOC	8.2	6.8	5.3	6.8	
	GPIOD	8.7	7.1	5.7	7.1	
	GPIOE	7.6	6.2	4.9	6.2	
	GPIOF	7.7	6.3	5.0	6.3	
	GPIOG	8.4	7.0	5.4	7.0	
	GPIOH	1.8	1.3	1.1	1.3	
	CRC	0.8	0.6	0.4	0.6	
	FLASH	26.3	19.3	18.3	-(3)	
	DMA1	19.0	16.0	12.8	16.0	
	DMA2	17.0	14.5	11.5	14.5	
	FSMC	16.0	13.4	10.6	13.4	
All enabled		310	246	217	226.7	

Table 28. HSE oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	1		24	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
C	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_S = 30 Ω	-	20	-	pF
I_{HSE}	HSE driving current	V_{DD}= 3.3 V, V_{IN} = V_{SS} with 30 pF load	-	-	3	mA
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF f_{OSC} = 16 MHz	-	-	2.5 (startup) 0.7 (stabilized)	mA
		C = 10 pF f_{OSC} = 16 MHz	-	-	2.5 (startup) 0.46 (stabilized)	
g_m	Oscillator transconductance	Startup	3.5	-	-	mA /V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	1	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by characterization results.
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 16*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}. Refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website *www.st.com*.

Table 42. Synchronous multiplexed PSRAM write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	$2*T_{HCLK}$	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x = 0...2)	-	0	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x = 0...2)	0	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	0	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	0	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 16...25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x = 16...25)	$T_{HCLK} + 4$	-	ns
$t_{d(CLKL-NWEL)}$	FSMC_CLK low to FSMC_NWE low	-	0	ns
$t_{d(CLKL-NWEH)}$	FSMC_CLK low to FSMC_NWE high	1	-	ns
$t_{d(CLKL-ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	5	-	ns
$t_{d(CLKL-DATA)}$	FSMC_A/D[15:0] valid after FSMC_CLK low	-	6	ns
$t_{su(NWAITV-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	6	-	ns
$t_{h(CLKH-NWAITV)}$	FSMC_NWAIT valid after FSMC_CLK high	0	-	ns
$t_{d(CLKL-NBLH)}$	FSMC_CLK low to FSMC_NBL high	1	-	ns

1. C_L = 30 pF.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 46. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. frequency range			Unit
				4 MHz voltage range 3	16 MHz voltage range 2	32 MHz voltage range 1	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C, LQFP100 package compliant with IEC 61967-2	0.1 to 30 MHz	3	-6	-5	dBµV
			30 to 130 MHz	18	4	-7	
			130 MHz to 1GHz	15	5	-7	
			SAE EMI Level	2.5	2	1	-

6.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

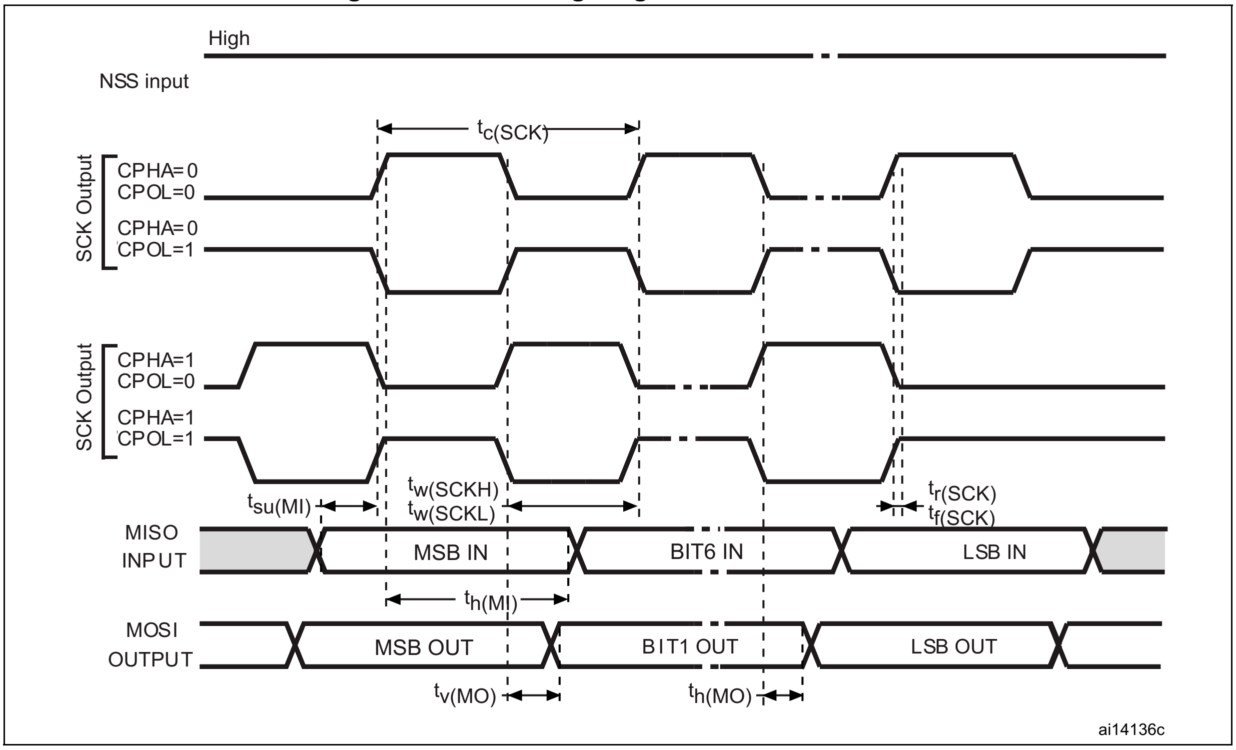
Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 47. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to JESD22-C101	III	500	V

1. Guaranteed by characterization results.

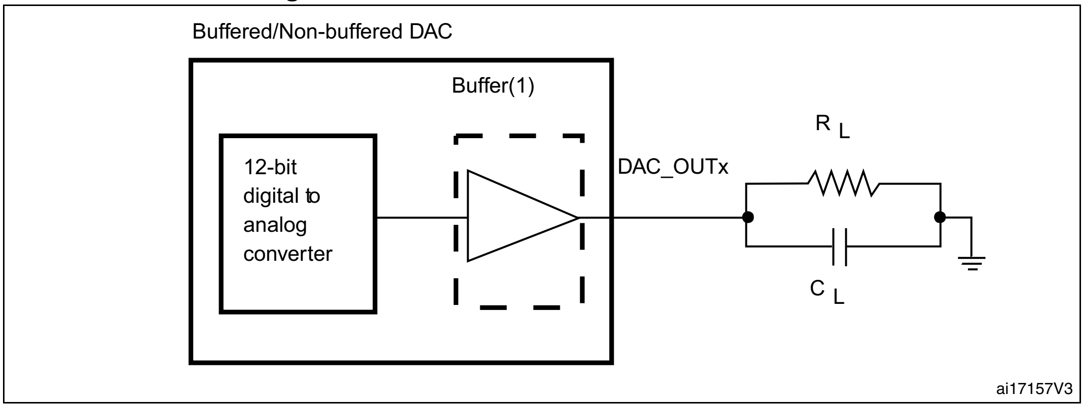
Figure 31. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

4. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095.
5. Difference between the value measured at Code (0x800) and the ideal value = $V_{REF+}/2$.
6. Difference between the value measured at Code (0x001) and the ideal value.
7. Difference between ideal slope of the transfer function and measured slope computed from code 0x000 and 0xFFF when buffer is OFF, and from code giving 0.2 V and (V_{DDA} – 0.2) V when buffer is ON.
8. In buffered mode, the output can overshoot above the final value for low input code (starting from min value).

Figure 39. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

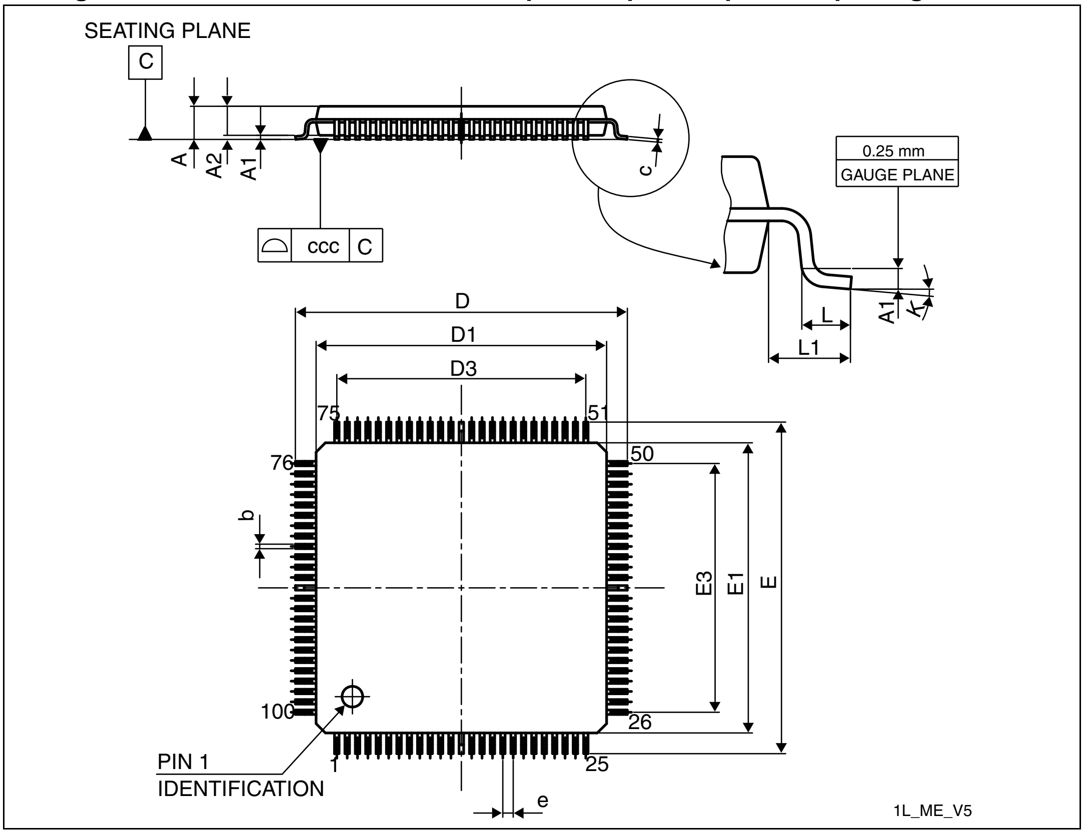
6.3.21 Operational amplifier characteristics

Table 68. Operational amplifier characteristics

Symbol	Parameter		Condition(1)	Min(2)	Typ	Max(2)	Unit
CMIR	Common mode input range		-	0	-	V_{DD}	
VI_{OFFSET}	Input offset voltage	Maximum calibration range	-	-	-	±15	mV
		After offset calibration	-	-	-	±1.5	
ΔVI_{OFFSET}	Input offset voltage drift	Normal mode	-	-	-	±40	µV/°C
		Low-power mode	-	-	-	±80	
I_{IB}	Input current bias	Dedicated input	75 °C	-	-	1	nA
		General purpose input		-	-	10	
I_{LOAD}	Drive current	Normal mode	-	-	-	500	µA
		Low-power mode	-	-	-	100	
I_{DD}	Consumption	Normal mode	No load, quiescent mode	-	100	220	µA
		Low-power mode		-	30	60	
CMRR	Common mode rejection ration	Normal mode	-	-	-85	-	dB
		Low-power mode	-	-	-90	-	

7.2 LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package information

Figure 43. LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 75. LQPF100, 14 x 14 mm, 100-pin low-profile quad flat package mechanical data

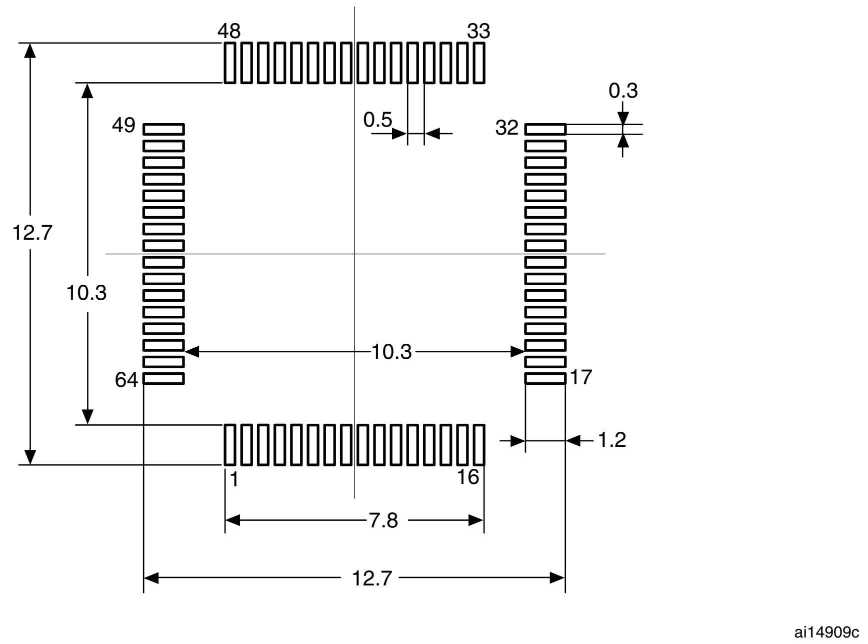
Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591

Table 76. LQFP64, 10 x 10 mm 64-pin low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 47. LQFP64, 10 x 10 mm, 64-pin low-profile quad flat package recommended footprint



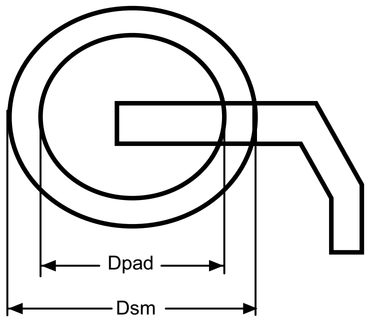
1. Dimensions are in millimeters.

Table 77. UFBGA132, 7 x 7 mm, 132-ball ultra thin, fine-pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 50. UFBGA132, 7 x 7 mm, 132-ball ultra thin, fine-pitch ball grid array package recommended footprint



Pitch	0.5 mm
D pad	0.27 mm
Dsm	0.35 mm typ (depends on the soldermask registration tolerance)
Solder paste	0.27 mm aperture diameter

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