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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, Cap Sense, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 109 |
| Program Memory Size | 384KB (384K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 12K x 8 |
| RAM Size | 48K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 40x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 132-UFBGA |
| Supplier Device Package | 132-UFBGA (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l151qdh6tr |

## 2.1 Device overview

**Table 2. Ultra-low-power STM32L151xD and STM32L152xD device features and peripheral counts**

| Peripheral | | STM32L15xRD | STM32L15xVD | STM32L15xQD | STM32L15xZD |
|---|---|---|---|---|---|
| Flash (Kbytes) | | 384 | | | |
| Data EEPROM (Kbytes) | | 12 | | | |
| RAM (Kbytes) | | 48 | | | |
| FSMC | | No | multiplexed only | Yes | |
| Timers | 32 bit | 1 | | | |
| | General-purpose | 6 | | | |
| | Basic | 2 | | | |
| Communi-cation interfaces | SPI | 8(3)(1) | | | |
| | $I^2S$ | 2 | | | |
| | $I^2C$ | 2 | | | |
| | USART | 5 | | | |
| | USB | 1 | | | |
| | SDIO | 1 | | | |
| GPIOs | | 51 | 83 | 109 | 115 |
| Operation amplifiers | | 3 | | | |
| 12-bit synchronized ADC<br>Number of channels | | 1<br>21 | 1<br>25 | 1<br>40 | 1<br>40 |
| 12-bit DAC<br>Number of channels | | 2<br>2 | | | |
| LCD (STM32L152xx devices only)<br>COM x SEG | | 1<br>4x32 or 8x28 | 1<br>4x44 or 8x40 | | |
| Comparators | | 2 | | | |
| Capacitive sensing channels | | 23 | | 33 | 34 |
| Max. CPU frequency | | 32 MHz | | | |
| Operating voltage | | 1.8 V to 3.6 V (down to 1.65 V at power-down) with BOR option<br>1.65 V to 3.6 V without BOR option | | | |

## 3.5 Low-power real-time clock and backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Dedicated registers contain the sub-second, second, minute, hour (12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day of the month are made automatically. The RTC provides two programmable alarms and programmable periodic interrupts with wakeup from Stop and Standby modes.

The programmable wakeup time ranges from 120 µs to 36 hours.

The RTC can be calibrated with an external 512 Hz output, and a digital compensation circuit helps reduce drift due to crystal deviation.

The RTC can also be automatically corrected with a 50/60Hz stable powerline.

The RTC calendar can be updated on the fly down to sub second precision, which enables network system synchronization.

A time stamp can record an external event occurrence, and generates an interrupt.

There are thirty-two 32-bit backup registers provided to store 128 bytes of user application data. They are cleared in case of tamper detection.

Three pins can be used to detect tamper events. A change on one of these pins can reset backup register and generate an interrupt. To prevent false tamper event, like ESD event, these three tamper inputs can be digitally filtered.

## 3.6 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions, and can be individually remapped using dedicated AFIO registers. All GPIOs are high current capable. The alternate function configuration of I/Os can be locked if needed following a specific sequence in order to avoid spurious writing to the I/O registers. The I/O controller is connected to the AHB with a toggling speed of up to 16 MHz.

### External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 24 edge detector lines used to generate interrupt/event requests. Each line can be individually configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 115 GPIOs can be connected to the 16 external interrupt lines. The 8 other lines are connected to RTC, PVD, USB, comparator events or capacitive sensing acquisition.

operate. This acquisition is managed directly by the GPIOs, timers and analog I/O groups (see *Section 3.15: System configuration controller and routing interface*).

Reliable touch sensing functionality can be quickly and easily implemented using the free STM32L1xx STMTouch touch sensing firmware library.

## 3.17 Timers and watchdogs

The ultra-low-power STM32L151xD and STM32L152xD devices include seven general-purpose timers, two basic timers, and two watchdog timers.

*Table 6* compares the features of the general-purpose and basic timers.

**Table 6. Timer feature comparison**

| Timer | Counter resolution | Counter type | Prescaler factor | DMA request generation | Capture/compare channels | Complementary outputs |
|---|---|---|---|---|---|---|
| TIM2, TIM3, TIM4 | 16-bit | Up, down, up/down | Any integer between 1 and 65536 | Yes | 4 | No |
| TIM5 | 32-bit | Up, down, up/down | Any integer between 1 and 65536 | Yes | 4 | No |
| TIM9 | 16-bit | Up, down, up/down | Any integer between 1 and 65536 | No | 2 | No |
| TIM10, TIM11 | 16-bit | Up | Any integer between 1 and 65536 | No | 1 | No |
| TIM6, TIM7 | 16-bit | Up | Any integer between 1 and 65536 | Yes | 0 | No |

### 3.17.1 General-purpose timers (TIM2, TIM3, TIM4, TIM5, TIM9, TIM10 and TIM11)

There are seven synchronizable general-purpose timers embedded in the STM32L151xD and STM32L152xD devices (see *Table 6* for differences).

#### TIM2, TIM3, TIM4, TIM5

TIM2, TIM3, TIM4 are based on 16-bit auto-reload up/down counter. TIM5 is based on a 32-bit auto-reload up/down counter. They include a 16-bit prescaler. They feature four independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input captures/output compares/PWMs on the largest packages.

TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together or with the TIM10, TIM11 and TIM9 general-purpose timers via the Timer Link feature for synchronization or event chaining. Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs.

TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

### 3.18.2 Universal synchronous/asynchronous receiver transmitter (USART)

The three USART and two UART interfaces are able to communicate at speeds of up to 4 Mbit/s. They support IrDA SIR ENDEC and have LIN Master/Slave capability. The three USARTs provide hardware management of the CTS and RTS signals and are ISO 7816 compliant.

All USART/UART interfaces can be served by the DMA controller.

### 3.18.3 Serial peripheral interface (SPI)

Up to three SPIs are able to communicate at up to 16 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

The SPIs can be served by the DMA controller.

### 3.18.4 Inter-integrated sound ($I^2S$)

Two standard I2S interfaces (multiplexed with SPI2 and SPI3) are available. They can operate in master or slave mode, and can be configured to operate with a 16-/32-bit resolution as input or output channels. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

The I2Ss can be served by the DMA controller.

### 3.18.5 SDIO

An SD/SDIO/MMC host interface is available, that supports MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit.

The interface allows data transfer at up to 24 MHz in 8-bit mode, and is compliant with the SD Memory Card Specification Version 2.0.

The SDIO Card Specification Version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDIO/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

In addition to SD/SDIO/MMC, this interface is fully compliant with the CE-ATA digital protocol Rev1.1.

### 3.18.6 Universal serial bus (USB)

The STM32L151xD and STM32L152xD devices embed a USB device peripheral compatible with the USB full-speed 12 Mbit/s. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and supports suspend/resume. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

Table 8. STM32L151xD and STM32L152xD pin definitions (continued)

| Pins | | | | | Pin name | Pin Type(1) | I / O structure | Main function(2) (after reset) | Pin functions | |
|---|---|---|---|---|---|---|---|---|---|---|
| LQFP144 | UFBGA132 | LQFP100 | LQFP64 | WLCSP64 | | | | | Alternate functions | Additional functions |
| 14 | F3 | - | - | - | PF4 | I/O | FT | PF4 | FSMC_A4 | - |
| 15 | F4 | - | - | - | PF5 | I/O | FT | PF5 | FSMC_A5 | - |
| 16 | F2 | 10 | - | - | $V_{SS\_5}$ | S | - | $V_{SS\_5}$ | - | - |
| 17 | G2 | 11 | - | - | $V_{DD\_5}$ | S | - | $V_{DD\_5}$ | - | - |
| 18 | G3 | - | - | - | PF6 | I/O | FT | PF6 | TIM5_CH1/TIM5_ETR | ADC_IN27 |
| 19 | G4 | - | - | - | PF7 | I/O | FT | PF7 | TIM5_CH2 | ADC_IN28/ COMP1_INP |
| 20 | H4 | - | - | - | PF8 | I/O | FT | PF8 | TIM5_CH3 | ADC_IN29/ COMP1_INP |
| 21 | J6 | - | - | - | PF9 | I/O | FT | PF9 | TIM5_CH4 | ADC_IN30/ COMP1_INP |
| 22 | - | - | - | - | PF10 | I/O | FT | PF10 | - | ADC_IN31/ COMP1_INP |
| 23 | F1 | 12 | 5 | D8 | PH0-OSC_IN(5) | I/O | TC | PH0 | - | OSC_IN |
| 24 | G1 | 13 | 6 | D7 | PH1-OSC_OUT(5) | I/O | TC | PH1 | - | OSC_OUT |
| 25 | H2 | 14 | 7 | C7 | NRST | I/O | RST | NRST | - | - |
| 26 | H1 | 15 | 8 | E8 | PC0 | I/O | FT | PC0 | LCD_SEG18 | ADC_IN10/ COMP1_INP |
| 27 | J2 | 16 | 9 | F8 | PC1 | I/O | FT | PC1 | LCD_SEG19 | ADC_IN11/ COMP1_INP OPAMP3_VINP |
| 28 | - | 17 | 10 | D6 | PC2 | I/O | FT | PC2 | LCD_SEG20 | ADC_IN12/ COMP1_INP OPAMP3_VINM |
| - | J3 | - | - | - | PC2 | I/O | FT | PC2 | LCD_SEG20 | ADC_IN12/ COMP1_INP |
| - | K1 | - | - | - | OPAMP3_VINM | I | - | OPAMP3_VINM | - | - |
| 29 | K2 | 18 | 11 | F7 | PC3 | I/O | TC | PC3 | LCD_SEG21 | ADC_IN13/ COMP1_INP/ OPAMP3_VOUT |
| 30 | J1 | 19 | 12 | E7 | $V_{SSA}$ | S | - | $V_{SSA}$ | - | - |

Table 8. STM32L151xD and STM32L152xD pin definitions (continued)

| Pins | | | | | Pin name | Pin Type(1) | I / O structure | Main function(2) (after reset) | Pin functions | |
|---|---|---|---|---|---|---|---|---|---|---|
| LQFP144 | UFBGA132 | LQFP100 | LQFP64 | WLCSP64 | | | | | Alternate functions | Additional functions |
| 79 | J12 | 57 | - | - | PD10 | I/O | FT | PD10 | USART3_CK/LCD_SEG30/ FSMC_D15 | - |
| 80 | J11 | 58 | - | - | PD11 | I/O | FT | PD11 | USART3_CTS/LCD_SEG31 /FSMC_A16 | - |
| 81 | J10 | 59 | - | - | PD12 | I/O | FT | PD12 | TIM4_CH1/USART3_RTS/ LCD_SEG32/ FSMC_A17 | - |
| 82 | H12 | 60 | - | - | PD13 | I/O | FT | PD13 | TIM4_CH2/LCD_SEG33/ FSMC_A18 | - |
| 83 | - | - | - | - | $V_{SS\_8}$ | S | - | $V_{SS\_8}$ | - | - |
| 84 | - | - | - | - | $V_{DD\_8}$ | S | - | $V_{DD\_8}$ | - | - |
| 85 | H11 | 61 | - | - | PD14 | I/O | FT | PD14 | TIM4_CH3/LCD_SEG34/ FSMC_D0 | - |
| 86 | H10 | 62 | - | - | PD15 | I/O | FT | PD15 | TIM4_CH4/LCD_SEG35 /FSMC_D1 | - |
| 87 | G10 | - | - | - | PG2 | I/O | FT | PG2 | FSMC_A12 | ADC_IN10b |
| 88 | F9 | - | - | - | PG3 | I/O | FT | PG3 | FSMC_A13 | ADC_IN11b |
| 89 | F10 | - | - | - | PG4 | I/O | FT | PG4 | FSMC_A14 | ADC_IN12b |
| 90 | E9 | - | - | - | PG5 | I/O | FT | PG5 | FSMC_A15 | - |
| 91 | - | - | - | - | PG6 | I/O | FT | PG6 | - | - |
| 92 | - | - | - | - | PG7 | I/O | FT | PG7 | - | - |
| 93 | - | - | - | - | PG8 | I/O | FT | PG8 | - | - |
| 94 | F6 | - | - | - | $V_{SS\_9}$ | S | | $V_{SS\_9}$ | - | - |
| 95 | G6 | - | - | - | $V_{DD\_9}$ | S | | $V_{DD\_9}$ | - | - |
| 96 | E12 | 63 | 37 | E1 | PC6 | I/O | FT | PC6 | TIM3_CH1/I2S2_MCK/ LCD_SEG24/SDIO_D6 | - |
| 97 | E11 | 64 | 38 | E2 | PC7 | I/O | FT | PC7 | TIM3_CH2/I2S3_MCK/ LCD_SEG25/SDIO_D7 | - |
| 98 | E10 | 65 | 39 | E3 | PC8 | I/O | FT | PC8 | TIM3_CH3/LCD_SEG26/ SDIO_D0 | - |
| 99 | D12 | 66 | 40 | D1 | PC9 | I/O | FT | PC9 | TIM3_CH4/LCD_SEG27/ SDIO_D1 | - |

Table 9. Alternate function input/output (continued)

| Port name | Digital alternate function number | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | AFIO0 | AFIO1 | AFIO2 | AFIO3 | AFIO4 | AFIO5 | AFIO6 | AFIO7 | AFIO8 | .. | AFIO11 | AFIO12 | .. | AFIO14 | AFIO15 |
| | Alternate function | | | | | | | | | | | | | | |
| | SYSTEM | TIM2 | TIM3/4/5 | TIM9/ 10/11 | I2C1/2 | SPI1/2 | SPI3 | USART1/2/3 | UART4/5 | | LCD | FSMC/ SDIO | | CPRI | SYSTEM |
| PG5 | - | - | - | - | - | - | - | - | - | | - | A15 | | - | EVENT OUT |
| PG6 | - | - | - | - | - | - | - | - | - | | - | - | | - | EVENT OUT |
| PG7 | - | - | - | - | - | - | - | - | - | | - | - | | - | EVENT OUT |
| PG8 | - | - | - | - | - | - | - | - | - | | - | - | | - | EVENT OUT |
| PG9 | - | - | - | - | - | - | - | - | - | | - | NE2 | | - | EVENT OUT |
| PG10 | - | - | - | - | - | - | - | - | - | | - | NE3 | | - | EVENT OUT |
| PG11 | - | - | - | - | - | - | - | - | - | | - | - | | - | EVENT OUT |
| PG12 | - | - | - | - | - | - | - | - | - | | - | NE4 | | - | EVENT OUT |
| PG13 | - | - | - | - | - | - | - | - | - | | - | A24 | | - | EVENT OUT |
| PG14 | - | - | - | - | - | - | - | - | - | | - | A25 | | - | EVENT OUT |
| PG15 | - | - | - | - | - | - | - | - | - | | - | - | | - | EVENT OUT |
| PH0OSC_IN | - | - | - | - | - | - | - | - | - | | - | - | | - | - |
| PH1OSC_OUT | - | - | - | - | - | - | - | - | - | | - | - | | - | - |
| PH2 | - | - | - | - | - | - | - | - | - | | - | A22 | | - | - |

**Table 17. Current consumption in Run mode, code with data processing running from Flash**

| Symbol | Parameter | Conditions | | $f_{HCLK}$ [MHz] | Typ | Max (1) | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD}$ (Run from Flash) | Supply current in Run mode code executed from Flash | $f_{HSE} = f_{HCLK}$ up to 16MHz, included $f_{HSE} = f_{HCLK}/2$ above 16 MHz (PLL ON)(2) | Range3, $V_{CORE}$=1.2 V VOS[1:0]=11 | 1 | 290 | 500 | µA |
| | | | | 2 | 505 | 750 | |
| | | | | 4 | 955 | 1200 | |
| | | | Range2, $V_{CORE}$=1.5 V VOS[1:0]=10 | 4 | 1.15 | 1.6 | mA |
| | | | | 8 | 2.3 | 2.9 | |
| | | | | 16 | 4.25 | 5.2 | |
| | | | Range1, $V_{CORE}$=1.8 V VOS[1:0]=01 | 8 | 2.65 | 3.5 | |
| | | | | 16 | 5.35 | 6.5 | |
| | | | | 32 | 10.5 | 12 | |
| | | HSI clock source (16 MHz) | Range2, $V_{CORE}$=1.5 V VOS[1:0]=10 | 16 | 4.35 | 5.2 | |
| | | | Range1, $V_{CORE}$=1.8 V VOS[1:0]=01 | 32 | 10.5 | 12.3 | |
| | | MSI clock, 65 kHZ | Range3, $V_{CORE}$=1.2 V VOS[1:0]=11 | 0.065 | 46 | 130 | µA |
| | | MSI clock, 524 kHZ | | 0.524 | 160 | 250 | |
| | | MSI clock, 4.2 MHZ | | 4.2 | 965 | 1200 | |

1. Guaranteed by characterization results, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

**Table 24. Peripheral current consumption(1) (continued)**

| Peripheral | | Typical consumption, $V_{DD}$ = 3.0 V, $T_A$ = 25 °C | | | | Unit |
|---|---|---|---|---|---|---|
| | | Range 1, $V_{CORE}$= 1.8 V VOS[1:0] = 01 | Range 2, $V_{CORE}$= 1.5 V VOS[1:0] = 10 | Range 3, $V_{CORE}$= 1.2 V VOS[1:0] = 11 | Low-power sleep and run | |
| $I_{DD\ (RTC)}$ | | 0.4 | | | | µA |
| $I_{DD\ (LCD)}$ | | 3.1 | | | | |
| $I_{DD\ (ADC)}$(4) | | 1450 | | | | |
| $I_{DD\ (DAC)}$(5) | | 340 | | | | |
| $I_{DD\ (COMP1)}$ | | 0.16 | | | | |
| $I_{DD\ (COMP2)}$ | Slow mode | 2 | | | | |
| | Fast mode | 5 | | | | |
| $I_{DD\ (PVD / BOR)}$(6) | | 2.6 | | | | |
| $I_{DD\ (IWDG)}$ | | 0.25 | | | | |

1. Data based on differential $I_{DD}$ measurement between all peripherals OFF an one peripheral with clock enabled, in the following conditions: $f_{HCLK}$ = 32 MHz (range 1), $f_{HCLK}$ = 16 MHz (range 2), $f_{HCLK}$ = 4 MHz (range 3), $f_{HCLK}$ = 64kHz (Low-power run/sleep), $f_{APB1} = f_{HCLK}$, $f_{APB2} = f_{HCLK}$, default prescaler value for each peripheral. The CPU is in Sleep mode in both cases. No I/O pins toggling.
2. HSI oscillator is OFF for this measure.
3. In Low-power sleep and run mode, the Flash memory must always be in power-down mode.
4. Data based on a differential $I_{DD}$ measurement between ADC in reset configuration and continuous ADC conversion (HSI consumption not included).
5. Data based on a differential $I_{DD}$ measurement between DAC in reset configuration and continuous DAC conversion of $V_{DD}$/2. DAC is in buffered mode, output is left floating.
6. Including supply current of internal reference voltage.

### 6.3.5 Wakeup time from low-power mode

The wakeup times given in the following table are measured with the MSI RC oscillator. The clock source used to wake up the device depends on the current operating mode:

- Sleep mode: the clock source is the clock that was set before entering Sleep mode
- Stop mode: the clock source is the MSI oscillator in the range configured before entering Stop mode
- Standby mode: the clock source is the MSI oscillator running at 2.1 MHz

All timings are derived from tests performed under the conditions summarized in *Table 13*.

### Multi-speed internal (MSI) RC oscillator

**Table 32. MSI oscillator characteristics**

| Symbol | Parameter | Condition | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{MSI}$ | Frequency after factory calibration, done at $V_{DD}$= 3.3 V and $T_A$ = 25 °C | MSI range 0 | 65.5 | - | kHz |
| | | MSI range 1 | 131 | - | |
| | | MSI range 2 | 262 | - | |
| | | MSI range 3 | 524 | - | |
| | | MSI range 4 | 1.05 | - | MHz |
| | | MSI range 5 | 2.1 | - | |
| | | MSI range 6 | 4.2 | - | |
| $ACC_{MSI}$ | Frequency error after factory calibration | - | ±0.5 | - | % |
| $D_{TEMP(MSI)}$(1) | MSI oscillator frequency drift 0 °C ≤$T_A$ ≤105 °C | - | ±3 | - | % |
| $D_{VOLT(MSI)}$(1) | MSI oscillator frequency drift 1.65 V ≤$V_{DD}$ ≤3.6 V, $T_A$ = 25 °C | - | - | 2.5 | %/V |
| $I_{DD(MSI)}$(2) | MSI oscillator power consumption | MSI range 0 | 0.75 | - | µA |
| | | MSI range 1 | 1 | - | |
| | | MSI range 2 | 1.5 | - | |
| | | MSI range 3 | 2.5 | - | |
| | | MSI range 4 | 4.5 | - | |
| | | MSI range 5 | 8 | - | |
| | | MSI range 6 | 15 | - | |
| $t_{SU(MSI)}$ | MSI oscillator startup time | MSI range 0 | 30 | - | µs |
| | | MSI range 1 | 20 | - | |
| | | MSI range 2 | 15 | - | |
| | | MSI range 3 | 10 | - | |
| | | MSI range 4 | 6 | - | |
| | | MSI range 5 | 5 | - | |
| | | MSI range 6, Voltage range 1 and 2 | 3.5 | - | |
| | | MSI range 6, Voltage range 3 | 5 | - | |

## Flash memory and data EEPROM

**Table 35. Flash memory and data EEPROM characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Operating voltage Read / Write / Erase | - | 1.65 | - | 3.6 | V |
| $t_{prog}$ | Programming/ erasing time for byte / word / double word / half-page | Erasing | - | 3.28 | 3.94 | ms |
| | | Programming | - | 3.28 | 3.94 | |
| $I_{DD}$ | Average current during the whole programming / erase operation | $T_A$ = 25 °C, $V_{DD}$ = 3.6 V | - | 600 | 900 | µA |
| | Maximum current (peak) during the whole programming / erase operation | | - | 1.5 | 2.5 | mA |

1. Guaranteed by design.

**Table 36. Flash memory and data EEPROM endurance and retention**

| Symbol | Parameter | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min(1) | Typ | Max | |
| $N_{CYC}$(2) | Cycling (erase / write) Program memory | $T_A$ = -40°C to 105 °C | 10 | - | - | kcycles |
| | Cycling (erase / write) EEPROM data memory | | 300 | - | - | |
| $t_{RET}$(2) | Data retention (program memory) after 10 kcycles at $T_A$ = 85 °C | $T_{RET}$ = +85 °C | 30 | - | - | years |
| | Data retention (EEPROM data memory) after 300 kcycles at $T_A$ = 85 °C | | 30 | - | - | |
| | Data retention (program memory) after 10 kcycles at $T_A$ = 105 °C | $T_{RET}$ = +105 °C | 10 | - | - | |
| | Data retention (EEPROM data memory) after 300 kcycles at $T_A$ = 105 °C | | 10 | - | - | |

1. Guaranteed by characterization results.
2. Characterization is done according to JEDEC JESD22-A117.

**Table 40. Asynchronous multiplexed PSRAM/NOR write timings(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FSMC_NE low time | $4*T_{HCLK} - 3$ | $4*T_{HCLK} + 2$ | ns |
| $t_{v(NWE\_NE)}$ | FSMC_NEx low to FSMC_NWE low | $T_{HCLK}$ | $T_{HCLK} + 1$ | ns |
| $t_{w(NWE)}$ | FSMC_NWE low time | $2*T_{HCLK} - 2$ | $2*T_{HCLK} + 4$ | ns |
| $t_{h(NE\_NWE)}$ | FSMC_NWE high to FSMC_NE high hold time | $T_{HCLK} - 2.5$ | - | ns |
| $t_{v(A\_NE)}$ | FSMC_NEx low to FSMC_A valid | - | 6 | ns |
| $t_{v(NADV\_NE)}$ | FSMC_NEx low to FSMC_NADV low | 1.5 | 2 | ns |
| $t_{w(NADV)}$ | FSMC_NADV low time | $T_{HCLK} - 4$ | $T_{HCLK} + 4$ | ns |
| $t_{h(AD\_NADV)}$ | FSMC_AD (address) valid hold time after FSMC_NADV high | $T_{HCLK} - 5$ | - | ns |
| $t_{h(A\_NWE)}$ | Address hold time after FSMC_NWE high | $T_{HCLK} - 2.5$ | - | ns |
| $t_{h(BL\_NWE)}$ | FSMC_BL hold time after FSMC_NWE high | $T_{HCLK} - 3$ | - | ns |
| $t_{v(BL\_NE)}$ | FSMC_NEx low to FSMC_BL valid | - | 0.5 | ns |
| $t_{v(Data\_NADV)}$ | FSMC_NADV high to Data valid | - | $T_{HCLK} + 6$ | ns |
| $t_{h(Data\_NWE)}$ | Data hold time after FSMC_NWE high | $T_{HCLK} - 2.5$ | - | ns |

1. $C_L$ = 30 pF.

## 6.3.14 I/O port characteristics

### General input/output characteristics

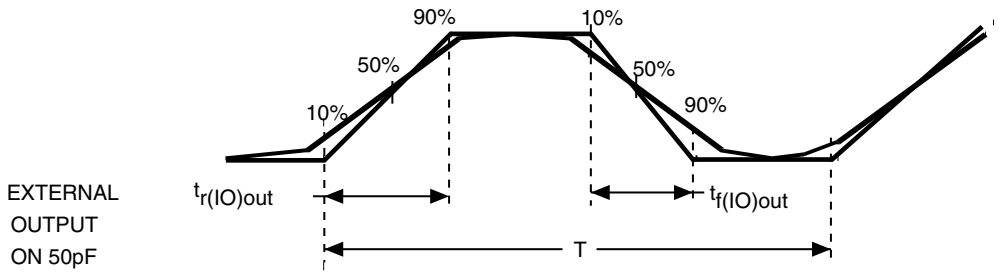
Unless otherwise specified, the parameters given in *Table 56* are derived from tests performed under the conditions summarized in *Table 13*. All I/Os are CMOS and TTL compliant.

**Table 50. I/O static characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input low level voltage | - | - | - | $0.3V_{DD}$ (1) | V |
| $V_{IH}$ | Input high level voltage | Standard I/O | 0.7 $V_{DD}$ | - | - | |
| | | FT I/O | | - | - | |
| | | BOOT0 I/O | | - | - | |
| $V_{hys}$ | I/O Schmitt trigger voltage hysteresis(2) | Standard I/O | - | 10% $V_{DD}$(3) | - | |
| $I_{lkg}$ | Input leakage current(4) | $V_{SS} \le V_{IN} \le V_{DD}$ I/Os with LCD | - | - | ±50 | nA |
| | | $V_{SS} \le V_{IN} \le V_{DD}$ I/Os with analog switches | - | - | ±50 | |
| | | $V_{SS} \le V_{IN} \le V_{DD}$ I/Os with analog switches and LCD | - | - | ±50 | |
| | | $V_{SS} \le V_{IN} \le V_{DD}$ I/Os with USB | - | - | ±250 | |
| | | $V_{SS} \le V_{IN} \le V_{DD}$ Standard I/Os | - | - | ±50 | |
| | | FT I/O $V_{DD} \le V_{IN} \le 5V$ | - | - | ±10 | uA |
| $R_{PU}$ | Weak pull-up equivalent resistor(1)(5) | $V_{IN} = V_{SS}$ | 30 | 45 | 60 | kΩ |
| $R_{PD}$ | Weak pull-down equivalent resistor(5) | $V_{IN} = V_{DD}$ | 30 | 45 | 60 | kΩ |
| $C_{IO}$ | I/O pin capacitance | - | - | 5 | - | pF |

1. Guaranteed by test in production
2. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results.
3. With a minimum of 200 mV. Guaranteed by characterization results.
4. The max. value may be exceeded if negative current is injected on adjacent pins.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS.

**Figure 26. I/O AC characteristics definition**




Maximum frequency is achieved if $(t_r + t_f) \leq 2/3)T$ and if the duty cycle is (45-55%)
when loaded by 50pF

ai14131c

## 6.3.15 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, $R_{PU}$ (see *Table 53*)

Unless otherwise specified, the parameters given in *Table 53* are derived from tests performed under the conditions summarized in *Table 13*.

**Table 53. NRST pin characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL(NRST)}$(1) | NRST input low level voltage | - | - | - | 0.3 $V_{DD}$ | V |
| $V_{IH(NRST)}$(1) | NRST input high level voltage | - | 0.7 $V_{DD}$ | - | - | |
| $V_{OL(NRST)}$(1) | NRST output low level voltage | $I_{OL}$ = 2 mA<br>2.7 V < $V_{DD}$ < 3.6 V | - | - | 0.4 | |
| | | $I_{OL}$ = 1.5 mA<br>1.65 V < $V_{DD}$ < 2.7 V | - | - | | |
| $V_{hys(NRST)}$(1) | NRST Schmitt trigger voltage hysteresis | - | - | 10%$V_{DD}$(2) | - | mV |
| $R_{PU}$ | Weak pull-up equivalent resistor(3) | $V_{IN}$ = $V_{SS}$ | 30 | 45 | 60 | kΩ |
| $V_{F(NRST)}$(1) | NRST input filtered pulse | - | - | - | 50 | ns |
| $V_{NF(NRST)}$(3) | NRST input not filtered pulse | - | 350 | - | - | ns |

1. Guaranteed by design.
2. With a minimum of 200 mV.
3. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is around 10%.

### 6.3.19 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 64* are guaranteed by design.

**Table 63. ADC clock frequency**

| Symbol | Parameter | Conditions | | | Min | Max | Unit |
|---|---|---|---|---|---|---|---|
| $f_{ADC}$ | ADC clock frequency | Voltage range 1 & 2 | 2.4 V ≤$V_{DDA}$ ≤3.6 V | $V_{REF+}$ = $V_{DDA}$ | 0.480 | 16 | MHz |
| | | | | $V_{REF+}$ < $V_{DDA}$ $V_{REF+}$ > 2.4 V | | 8 | |
| | | | | $V_{REF+}$ < $V_{DDA}$ $V_{REF+}$ ≤2.4 V | | 4 | |
| | | | 1.8 V ≤$V_{DDA}$ ≤2.4 V | $V_{REF+}$ = $V_{DDA}$ | | 8 | |
| | | | | $V_{REF+}$ < $V_{DDA}$ | | 4 | |
| | | Voltage range 3 | | | | 4 | |

**Table 64. ADC characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Power supply | - | 1.8 | - | 3.6 | V |
| $V_{REF+}$ | Positive reference voltage | - | 1.8(1) | - | $V_{DDA}$ | |
| $V_{REF-}$ | Negative reference voltage | - | - | $V_{SSA}$ | - | |
| $I_{VDDA}$ | Current on the $V_{DDA}$ input pin | - | - | 1000 | 1450 | µA |
| $I_{VREF}$(2) | Current on the $V_{REF}$ input pin | Peak | - | 400 | 700 | |
| | | Average | - | | 450 | |
| $V_{AIN}$ | Conversion voltage range(3) | - | 0(4) | - | $V_{REF+}$ | V |
| $f_S$ | 12-bit sampling rate | Direct channels | - | - | 1 | Msps |
| | | Multiplexed channels | - | - | 0.76 | |
| | 10-bit sampling rate | Direct channels | - | - | 1.07 | Msps |
| | | Multiplexed channels | - | - | 0.8 | |
| | 8-bit sampling rate | Direct channels | - | - | 1.23 | Msps |
| | | Multiplexed channels | - | - | 0.89 | |
| | 6-bit sampling rate | Direct channels | - | - | 1.45 | Msps |
| | | Multiplexed channels | - | - | 1 | |

**Table 67. DAC characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| dOffset/dT(1) | Offset error temperature coefficient (code 0x800) | $V_{DDA}$ = 3.3V<br>$V_{REF+}$ = 3.0V<br>$T_A$ = 0 to 50 °C<br>DAC output buffer OFF | -20 | -10 | 0 | µV/°C |
| | | $V_{DDA}$ = 3.3V<br>$V_{REF+}$ = 3.0V<br>$T_A$ = 0 to 50 °C<br>DAC output buffer ON | 0 | 20 | 50 | |
| Gain(1) | Gain error(7) | $C_L \leq 50$ pF, $R_L \geq 5$ kΩ<br>DAC output buffer ON | - | +0.1 / -0.2% | +0.2 / -0.5% | % |
| | | No $R_L$, $C_L \leq 50$ pF<br>DAC output buffer OFF | - | +0 / -0.2% | +0 / -0.4% | |
| dGain/dT(1) | Gain error temperature coefficient | $V_{DDA}$ = 3.3V<br>$V_{REF+}$ = 3.0V<br>$T_A$ = 0 to 50 °C<br>DAC output buffer OFF | -10 | -2 | 0 | µV/°C |
| | | $V_{DDA}$ = 3.3V<br>$V_{REF+}$ = 3.0V<br>$T_A$ = 0 to 50 °C<br>DAC output buffer ON | -40 | -8 | 0 | |
| TUE(1) | Total unadjusted error | $C_L \leq 50$ pF, $R_L \geq 5$ kΩ<br>DAC output buffer ON | - | 12 | 30 | LSB |
| | | No $R_L$, $C_L \leq 50$ pF<br>DAC output buffer OFF | - | 8 | 12 | |
| $t_{SETTLING}$ | Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes till DAC_OUT reaches final value ±1LSB | $C_L \leq 50$ pF, $R_L \geq 5$ kΩ | - | 7 | 12 | µs |
| Update rate | Max frequency for a correct DAC_OUT change (95% of final value) with 1 LSB variation in the input code | $C_L \leq 50$ pF, $R_L \geq 5$ kΩ | - | - | 1 | Msps |
| $t_{WAKEUP}$ | Wakeup time from off state (setting the ENx bit in the DAC Control register)(8) | $C_L \leq 50$ pF, $R_L \geq 5$ kΩ | - | 9 | 15 | µs |
| PSRR+ | $V_{DDA}$ supply rejection ratio (static DC measurement) | $C_L \leq 50$ pF, $R_L \geq 5$ kΩ | - | -60 | -35 | dB |

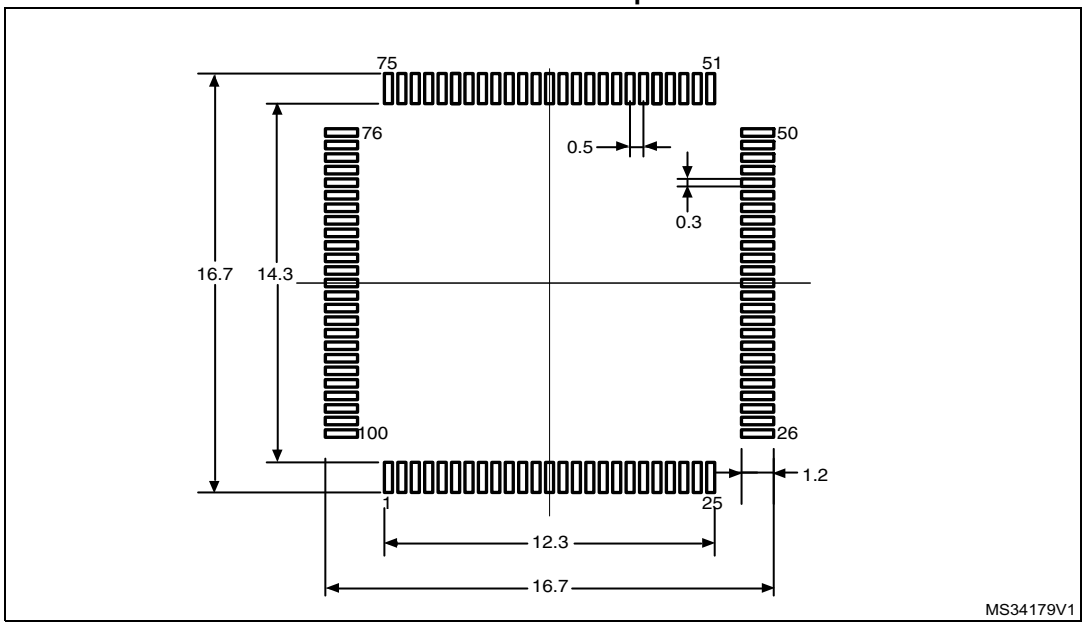
1. Data based on characterization results.
2. Connected between DAC_OUT and $V_{SSA}$.
3. Difference between two consecutive codes - 1 LSB.

**Table 75. LQPF100, 14 x 14 mm, 100-pin low-profile quad flat package mechanical data (continued)**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| E3 | - | 12.000 | - | - | 0.4724 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0.0° | 3.5° | 7.0° | 0.0° | 3.5° | 7.0° |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 44. LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package recommended footprint**

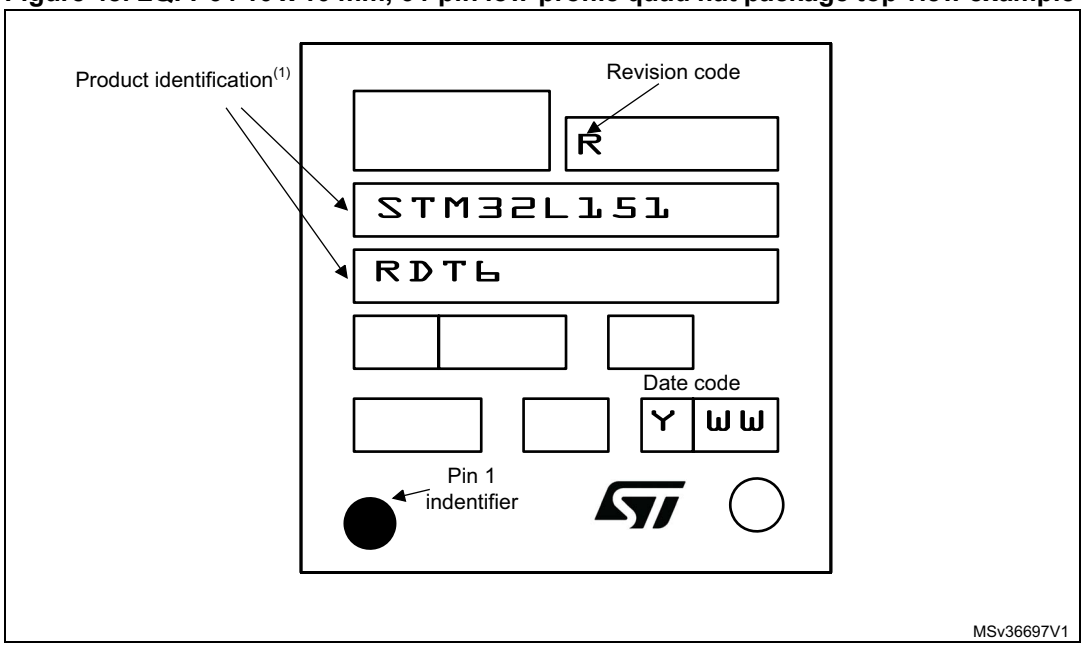



1. Dimensions are in millimeters.

### Marking of engineering samples

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

**Figure 48. LQFP64 10 x 10 mm, 64-pin low-profile quad flat package top view example**




1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity

Figure 55. Thermal resistance suffix 6

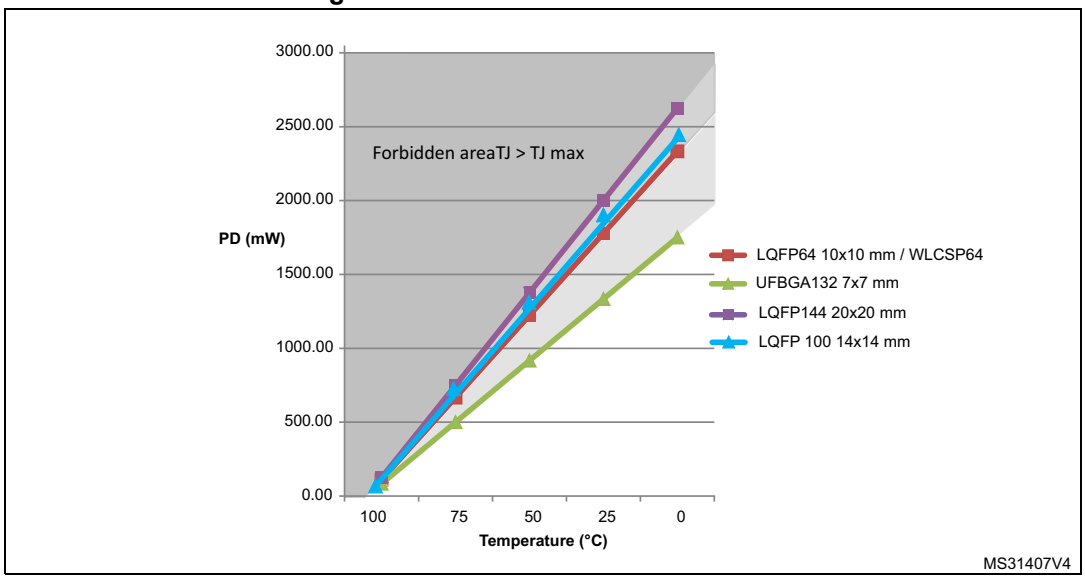
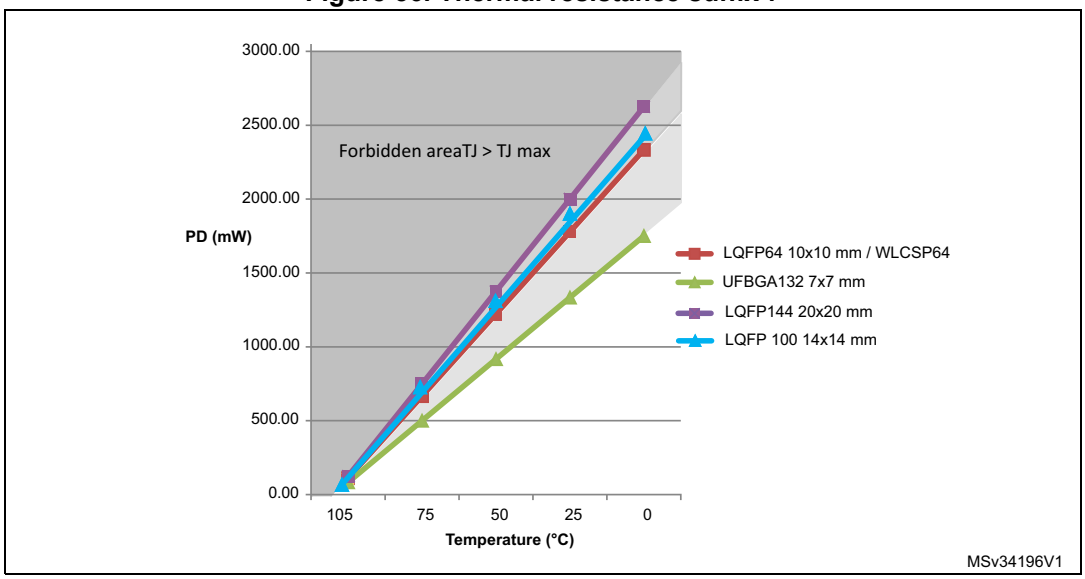



Figure 56. Thermal resistance suffix 7




### 7.6.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

# 9 Revision History

**Table 82. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 03-Oct-2011 | 1 | Initial release. |
| 03-Feb-2012 | 2 | Status of the document changed (datasheet instead of preliminary data).<br>Updated low power features on page 1.<br>Removed references to devices with 256 KB of Flash memory. GPIOF replaced with GIOPH.<br>Added SDIO in *Table 4: Ultra-low-power STM32L15xxD device features and peripheral counts on page 12* and in *Table 19: ction input/output on page 86* (FSMC/SDIO instead of FSMC).<br>*Table 4: Ultra-low-power STM32L15xxD device features and peripheral counts*: replaced STM32L15xWx with STM32L15xQx.<br>*Figure 1: Ultra-low-power STM32L162xC block diagram*: updated legend.<br>Modified *Section 3.4: Clock management on page 20*.<br>*Table 4: STM32L15xQD STM32L162QD UFBGA132 ballout*: replaced STM32L15xWC/D with STM32L15xQD.<br>*Figure 3*, *Figure 3*, *Figure 4*: updated titles.<br>*Table 14: STM32L15xxD pin definitions*: updated title, updated pins PF0, PF1, PH2, PF12, PF13, PF14, PF15, PG0, PG1, PG12, PG15, PD0, and PD1.<br>*Table 19: ction input/output*: Modified ction for PA13 and PA14; removed EVENT OUT for PH2.<br>*Figure 5: Memory map*: removed the text “APB memory space”.<br>Modified *Figure 8: Power supply scheme on page 46*.<br>Modified *Table 2: Functionalities depending on the operating power supply range on page 15*.<br>*Table 18: Current consumption in Run mode, code with data processing running from RAM*: added footnote *3*.<br>*Table 19: Current consumption in Sleep mode*: updated condition for $f_{HSE}$; added footnote *3*.<br>*Table 23: Typical and maximum current consumptions in Standby mode*: modified max values.<br>*Table 64: USB DC electrical characteristics*: removed two footnotes.<br>Modified *Table 38: Flash memory and data EEPROM characteristics on page 83*.<br>*Table 73: Thermal characteristics*: updated “TBDs” with values.<br>Modified tables in *Section 6.3.4: Supply current characteristics on page 54*. |