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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, I²S, POR, PWM, WDT
Number of I/O	51
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	12K x 8
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 21x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l151rdt6tr

2.2.3 Common system strategy.

To offer flexibility and optimize performance, the STM8L15xxx, STM32L15xxx and STM32L162xx family uses a common architecture:

- Same power supply range from 1.65 V to 3.6 V
- Architecture optimized to reach ultra-low consumption both in low-power modes and Run mode
- Fast startup strategy from low-power modes
- Flexible system clock
- Ultrasafe reset: same reset strategy including power-on reset, power-down reset, brownout reset and programmable voltage detector

2.2.4 Features

ST ultra-low-power continuum also lies in feature compatibility:

- More than 15 packages with pin count from 20 to 144 pins and size down to 3 x 3 mm
- Memory density ranging from 2 to 512 Kbytes

- **Stop** mode without RTC

  Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks are stopped, the PLL, MSI RC, HSI and LSI RC, LSE and HSE crystal oscillators are disabled. The voltage regulator is in the low-power mode. The device can be woken up from Stop mode by any of the EXTI line, in 8 µs. The EXTI line source can be one of the 16 external lines. It can be the PVD output, the Comparator 1 event or Comparator 2 event (if internal reference voltage is on). It can also be wakened by the USB wakeup.

- **Standby** mode with RTC

  Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI RC and HSE crystal oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC_CSR).

  The device exits Standby mode in 60 µs when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.

- **Standby** mode without RTC

  Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC_CSR).

  The device exits Standby mode in 60 µs when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped automatically by entering Stop or Standby mode.

Table 3. Functionalities depending on the operating power supply range

	Functionalities depending on the operating power supply range			
Operating power supply range	**DAC and ADC operation**	**USB**	**Dynamic voltage scaling range**	**I/O operation**
V_{DD}= V_{DDA} = 1.65 to 1.71 V	Not functional	Not functional	Range 2 or Range 3	Degraded speed performance
V_{DD}=V_{DDA}= 1.71 to 1.8 V(1)	Not functional	Not functional	Range 1, Range 2 or Range 3	Degraded speed performance
V_{DD}=V_{DDA}= 1.8 to 2.0 V(1)	Conversion time up to 500 Ksps	Not functional	Range 1, Range 2 or Range 3	Degraded speed performance

3.5 Low-power real-time clock and backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Dedicated registers contain the sub-second, second, minute, hour (12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day of the month are made automatically. The RTC provides two programmable alarms and programmable periodic interrupts with wakeup from Stop and Standby modes.

The programmable wakeup time ranges from 120 µs to 36 hours.

The RTC can be calibrated with an external 512 Hz output, and a digital compensation circuit helps reduce drift due to crystal deviation.

The RTC can also be automatically corrected with a 50/60Hz stable powerline.

The RTC calendar can be updated on the fly down to sub second precision, which enables network system synchronization.

A time stamp can record an external event occurrence, and generates an interrupt.

There are thirty-two 32-bit backup registers provided to store 128 bytes of user application data. They are cleared in case of tamper detection.

Three pins can be used to detect tamper events. A change on one of these pins can reset backup register and generate an interrupt. To prevent false tamper event, like ESD event, these three tamper inputs can be digitally filtered.

3.6 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions, and can be individually remapped using dedicated AFIO registers. All GPIOs are high current capable. The alternate function configuration of I/Os can be locked if needed following a specific sequence in order to avoid spurious writing to the I/O registers. The I/O controller is connected to the AHB with a toggling speed of up to 16 MHz.

External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 24 edge detector lines used to generate interrupt/event requests. Each line can be individually configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 115 GPIOs can be connected to the 16 external interrupt lines. The 8 other lines are connected to RTC, PVD, USB, comparator events or capacitive sensing acquisition.

The DMA can be used with the main peripherals: SPI, I^2C, USART, SDIO, general-purpose timers, DAC and ADC.

3.10 LCD (liquid crystal display)

The LCD drives up to 8 common terminals and 44 segment terminals to drive up to 320 pixels.

- Internal step-up converter to guarantee functionality and contrast control irrespective of V_{DD}. This converter can be deactivated, in which case the V_{LCD} pin is used to provide the voltage to the LCD
- Supports static, 1/2, 1/3, 1/4 and 1/8 duty
- Supports static, 1/2, 1/3 and 1/4 bias
- Phase inversion to reduce power consumption and EMI
- Up to 8 pixels can be programmed to blink
- Unneeded segments and common pins can be used as general I/O pins
- LCD RAM can be updated at any time owing to a double-buffer
- The LCD controller can operate in Stop mode

3.11 ADC (analog-to-digital converter)

A 12-bit analog-to-digital converters is embedded into STM32L151xD and STM32L152xD devices with up to 40 external channels, performing conversions in single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs with up to 28 external channels in a group.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all scanned channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start triggers, to allow the application to synchronize A/D conversions and timers. An injection mode allows high priority conversions to be done by interrupting a scan mode which runs in as a background task.

The ADC includes a specific low-power mode. The converter is able to operate at maximum speed even if the CPU is operating at a very low frequency and has an auto-shutdown function. The ADC's runtime and analog front-end current consumption are thus minimized whatever the MCU operating mode.

3.11.1 Temperature sensor

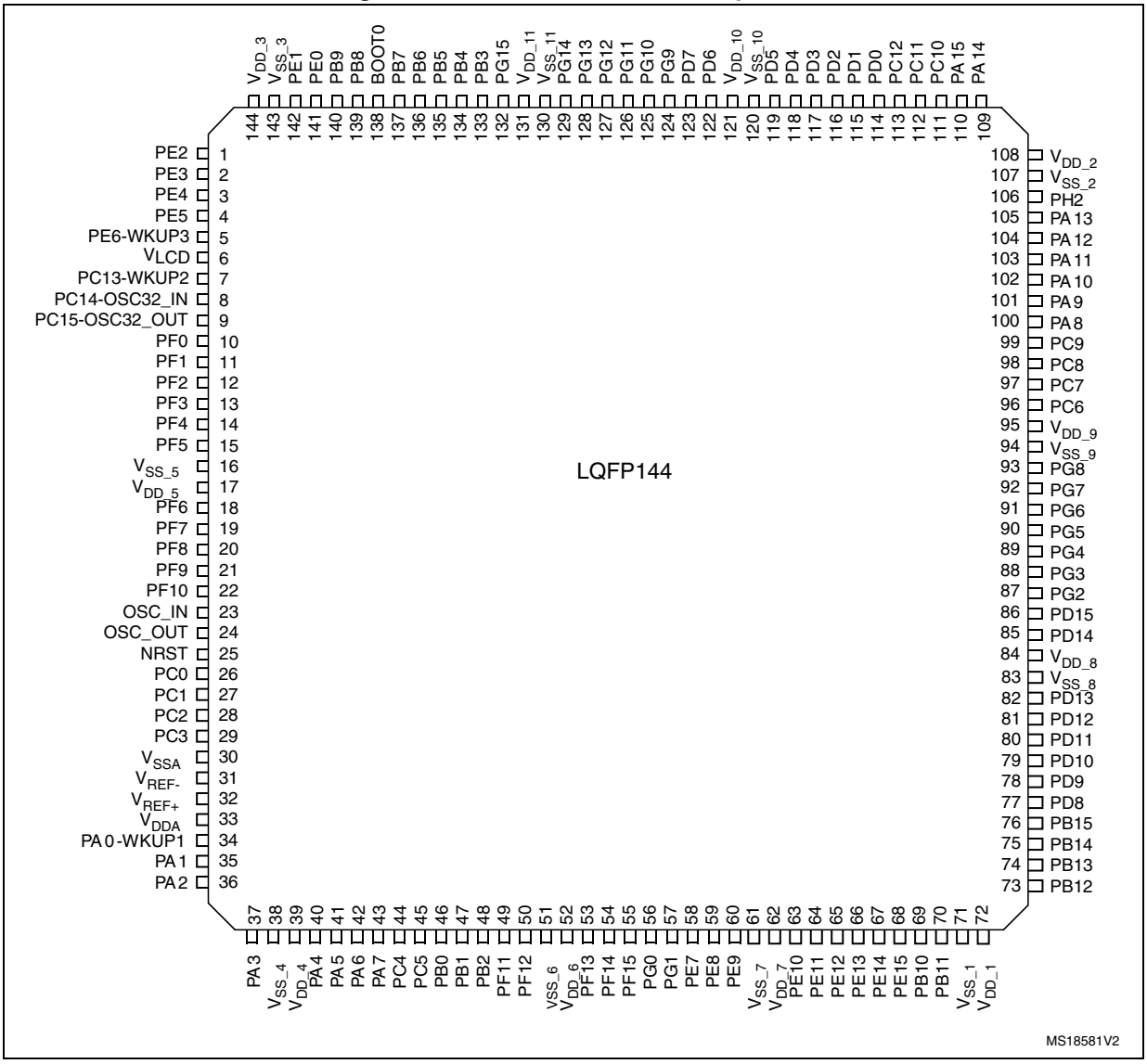
The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies

4 Pin descriptions

Figure 3. STM32L15xZD LQFP144 pinout



1. This figure shows the package top view.

Table 8. STM32L151xD and STM32L152xD pin definitions (continued)

Pins					Pin name	Pin Type(1)	I / O structure	Main function(2) (after reset)	Pin functions	
LQFP144	UFBGA132	LQFP100	LQFP64	WLCSP64					Alternate functions	Additional functions
61	-	-	-	-	V_{SS_7}	S	-	V_{SS_7}	-	-
62	-	-	-	-	V_{DD_7}	S	-	V_{DD_7}	-	-
63	L8	41	-	-	PE10	I/O	TC	PE10	TIM2_CH2/FSMC_D7	ADC_IN25/ COMP1_INP
64	M9	42	-	-	PE11	I/O	FT	PE11	TIM2_CH3/FSMC_D8	-
65	L9	43	-	-	PE12	I/O	FT	PE12	TIM2_CH4/SPI1_NSS /FSMC_D9	-
66	M10	44	-	-	PE13	I/O	FT	PE13	SPI1_SCK/FSMC_D10	-
67	M11	45	-	-	PE14	I/O	FT	PE14	SPI1_MISO/FSMC_D11	-
68	M12	46	-	-	PE15	I/O	FT	PE15	SPI1_MOSI/FSMC_D12	-
69	L10	47	29	G3	PB10	I/O	FT	PB10	TIM2_CH3/I2C2_SCL/ USART3_TX/ LCD_SEG10	-
70	L11	48	30	F3	PB11	I/O	FT	PB11	TIM2_CH4/ I2C2_SDA/ USART3_RX/ LCD_SEG11	-
71	F12	49	31	H2	V_{SS_1}	S	-	V_{SS_1}	-	-
72	G12	50	32	H1	V_{DD_1}	S	-	V_{DD_1}	-	-
73	L12	51	33	G2	PB12	I/O	FT	PB12	TIM10_CH1/I2C2_SMBA/ SPI2_NSS/ I2S2_WS/ USART3_CK/ LCD_SEG12	ADC_IN18/ COMP1_INP
74	K12	52	34	G1	PB13	I/O	FT	PB13	TIM9_CH1/SPI2_SCK/ I2S2_CK/ USART3_CTS/ LCD_SEG13	ADC_IN19/ COMP1_INP
75	K11	53	35	F2	PB14	I/O	FT	PB14	TIM9_CH2/SPI2_MISO/ USART3_RTS/ LCD_SEG14	ADC_IN20/ COMP1_INP
76	K10	54	36	F1	PB15	I/O	FT	PB15	TIM11_CH1/SPI2_MOSI/ I2S2_SD/ LCD_SEG15	ADC_IN21/ COMP1_INP/ RTC_REFIN
77	K9	55	-	-	PD8	I/O	FT	PD8	USART3_TX/LCD_SEG28/ FSMC_D13	-
78	K8	56	-	-	PD9	I/O	FT	PD9	USART3_RX/LCD_SEG29/ FSMC_D14	-

Alternate functions

Table 9. Alternate function input/output

Port name	Digital alternate function number									..			..		
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFIO6	AFIO7	AFIO8		AFIO11	AFIO12		AFIO14	AFIO15
	Alternate function														
	SYSTEM	TIM2	TIM3/4/5	TIM9/ 10/11	I2C1/2	SPI1/2	SPI3	USART1/2/3	UART4/5		LCD	FSMC/ SDIO		CPRI	SYSTEM
BOOT0	BOOT0	-	-	-	-	-	-	-	-		-	-		-	EVENT OUT
NRST	NRST	-	-	-	-	-	-	-	-		-	-		-	-
PA0-WKUP1	-	TIM2_CH1_ETR	TIM5_CH1	-	-	-	-	USART2_CTS	-		-	-		TIMx_IC1	EVENT OUT
PA1	-	TIM2_CH2	TIM5_CH2	-	-	-	-	USART2_RTS	-		SEG0	-		TIMx_IC2	EVENT OUT
PA2	-	TIM2_CH3	TIM5_CH3	TIM9_CH1	-	-	-	USART2_TX	-		SEG1	-		TIMx_IC3	EVENT OUT
PA3	-	TIM2_CH4	TIM5_CH4	TIM9_CH2	-	-	-	USART2_RX	-		SEG2	-		TIMx_IC4	EVENT OUT
PA4	-	-	-	-	-	SPI1_NSS	SPI3_NSS I2S3_WS	USART2_CK	-		-	-		TIMx_IC1	EVENT OUT
PA5	-	TIM2_CH1_ETR	-	-	-	SPI1_SCK	-	-	-		-	-		TIMx_IC2	EVENT OUT
PA6	-	-	TIM3_CH1	TIM10_ CH1	-	SPI1_MISO	-	-	-		SEG3	-		TIMx_IC3	EVENT OUT
PA7	-	-	TIM3_CH2	TIM11_ CH1	-	SPI1_MOSI	-	-	-		SEG4	-		TIMx_IC4	EVENT OUT
PA8	MCO	-	-	-	-	-	-	USART1_CK	-		COM0	-		TIMx_IC1	EVENT OUT
PA9	-	-	-	-	-	-	-	USART1_TX	-		COM1	-		TIMx_IC2	EVENT OUT
PA10	-	-	-	-	-	-	-	USART1_RX	-		COM2	-		TIMx_IC3	EVENT OUT
PA11	-	-	-	-	-	SPI1_MISO		USART1_CTS	-		-	-		TIMx_IC4	EVENT OUT

6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 10: Voltage characteristics*, *Table 11: Current characteristics*, and *Table 12: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 10. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA} and V_{DD})(1)	–0.3	4.0	V
V_{IN}(2)	Input voltage on five-volt tolerant pin	V_{SS} –0.3	V_{DD}+4.0	
	Input voltage on any other pin	V_{SS} –0.3	4.0	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all different ground pins(3)	-	50	
V_{REF+} –V_{DDA}	Allowed voltage difference for $V_{REF+} > V_{DDA}$	-	0.4	V
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.12*		

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 11* for maximum allowed injected current values.
3. Include V_{REF-} pin.

Table 11. Current characteristics

Symbol	Ratings	Max.	Unit
$I_{VDD(\Sigma)}$	Total current into sum of all V_{DD_x} power lines (source)(1)	100	mA
$I_{VSS(\Sigma)}$(2)	Total current out of sum of all V_{SS_x} ground lines (sink)(1)	100	
$I_{VDD(PIN)}$	Maximum current into each V_{DD_x} power pin (source)(1)	70	
$I_{VSS(PIN)}$	Maximum current out of each VSS_x ground pin (sink)(1)	-70	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current sourced by any I/O and control pin	- 25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all IOs and control pins(2)	60	
	Total output current sourced by sum of all IOs and control pins(2)	-60	
$I_{INJ(PIN)}$ (3)	Injected current on five-volt tolerant I/O(4), RST and B pins	-5/+0	
	Injected current on any other pin (5)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(6)	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Negative injection disturbs the analog performance of the device. See note in *Section 6.3.19*.

Table 18. Current consumption in Run mode, code with data processing running from RAM

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max	Unit
I_{DD} (Run from RAM)	Supply current in Run mode code executed from RAM	$f_{HSE} = f_{HCLK}$ up to 16 MHz, included $f_{HSE} = f_{HCLK}/2$ above 16MHz (PLL ON)(1)	Range3, V_{CORE}=1.2 V VOS[1:0]=11	1	230	470	µA
				2	415	780	
				4	800	1200	
			Range2, V_{CORE}=1.5 V VOS[1:0]=10	4	0.935	1.5	mA
				8	1.9	3	
				16	3.75	5	
			Range1, V_{CORE}=1.8 V VOS[1:0]=01	8	2.25	3.5	
				16	4.45	5.55	
				32	9.05	10.9	
		HSI clock source (16 MHz)	Range2, V_{CORE}=1.5 V VOS[1:0]=10	16	3.75	4.8	
			Range1, V_{CORE}=1.8 V VOS[1:0]=01	32	8.95	11.7	
		MSI clock, 65 kHZ	Range3, V_{CORE}=1.2 V VOS[1:0]=11	0.065	43.5	100	µA
		MSI clock, 524 kHZ		0.524	135	215	
		MSI clock, 4.2 MHZ		4.2	835	1100	

1. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 25. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
$t_{WUSLEEP}$	Wakeup from Sleep mode	f_{HCLK} = 32 MHz	0.4	-	µs
$t_{WUSLEEP\_LP}$	Wakeup from Low-power sleep mode, f_{HCLK} = 262 kHz	f_{HCLK} = 262 kHz Flash enabled	46	-	
		f_{HCLK} = 262 kHz Flash switched OFF	46	-	
t_{WUSTOP}	Wakeup from Stop mode, regulator in Run mode ULP bit = 1 and FWU bit = 1	$f_{HCLK} = f_{MSI}$ = 4.2 MHz	8.2	-	
	Wakeup from Stop mode, regulator in low-power mode ULP bit = 1 and FWU bit = 1	$f_{HCLK} = f_{MSI}$ = 4.2 MHz Voltage range 1 and 2	7.7	8.9	
		$f_{HCLK} = f_{MSI}$ = 4.2 MHz Voltage range 3	8.2	13.1	
		$f_{HCLK} = f_{MSI}$ = 2.1 MHz	10.2	13.4	
		$f_{HCLK} = f_{MSI}$ = 1.05 MHz	16	20	
		$f_{HCLK} = f_{MSI}$ = 524 kHz	31	37	
		$f_{HCLK} = f_{MSI}$ = 262 kHz	57	66	
		$f_{HCLK} = f_{MSI}$ = 131 kHz	112	123	
		f_{HCLK} = MSI = 65 kHz	221	236	
$t_{WUSTDBY}$	Wakeup from Standby mode ULP bit = 1 and FWU bit = 1	f_{HCLK} = MSI = 2.1 MHz	58	104	
	Wakeup from Standby mode FWU bit = 0	f_{HCLK} = MSI = 2.1 MHz	2.6	3.25	ms

1. Guaranteed by characterization, unless otherwise specified

6.3.6 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.The external clock signal has to respect the I/O characteristics in *Section 6.3.13*. However, the recommended clock input waveform is shown in *Figure 14*.

Table 26. High-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	CSS is on or PLL is used	1	8	32	MHz
		CSS is off, PLL not used	0	8	32	MHz

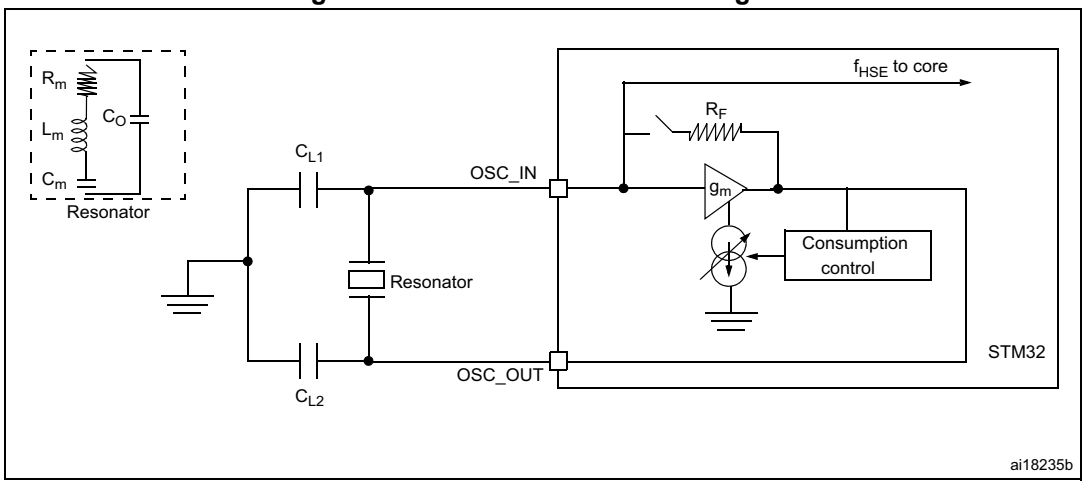
Table 28. HSE oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	1		24	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
C	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_S = 30 Ω	-	20	-	pF
I_{HSE}	HSE driving current	V_{DD}= 3.3 V, V_{IN} = V_{SS} with 30 pF load	-	-	3	mA
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF f_{OSC} = 16 MHz	-	-	2.5 (startup) 0.7 (stabilized)	mA
		C = 10 pF f_{OSC} = 16 MHz	-	-	2.5 (startup) 0.46 (stabilized)	
g_m	Oscillator transconductance	Startup	3.5	-	-	mA /V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	1	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by characterization results.
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 16*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}. Refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website *www.st.com*.

Figure 16. HSE oscillator circuit diagram



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 29*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

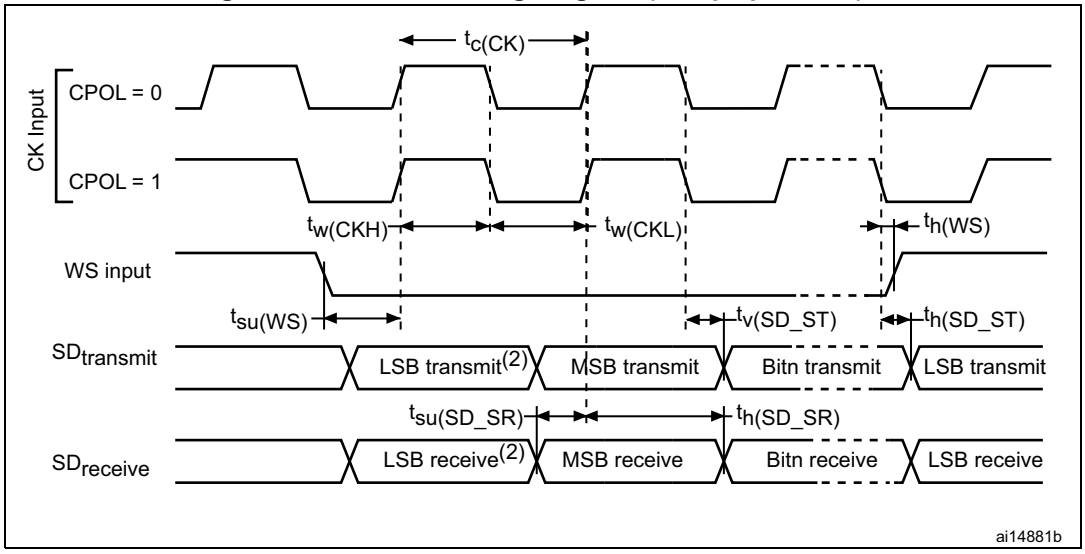
Table 29. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE}	Low speed external oscillator frequency	-	-	32.768	-	kHz
R_F	Feedback resistor	-	-	1.2	-	MΩ
$C^{(2)}$	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_S = 30 kΩ	-	8	-	pF
I_{LSE}	LSE driving current	V_{DD} = 3.3 V, V_{IN} = V_{SS}	-	-	1.1	µA
$I_{DD\ (LSE)}$	LSE oscillator current consumption	V_{DD} = 1.8 V	-	450	-	nA
		V_{DD} = 3.0 V	-	600	-	
		V_{DD} = 3.6V	-	750	-	
g_m	Oscillator transconductance	-	3	-	-	µA/V
$t_{SU(LSE)}$(4)	Startup time	V_{DD} is stabilized	-	1	-	s

1. Guaranteed by characterization results.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. The oscillator selection can be optimized in terms of supply current using an high quality resonator with small R_S value for example MSIV-TIN32.768kHz. Refer to crystal manufacturer for more details.

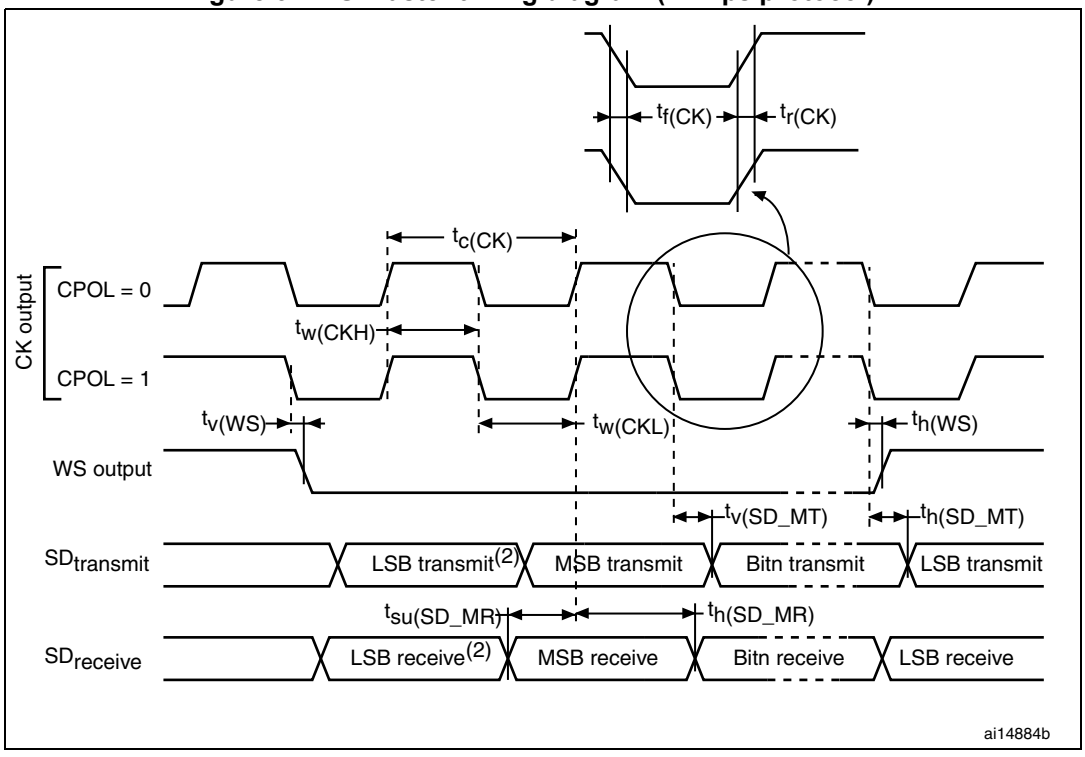
*ODD bit value, digital contribution leads to a min of (I2SDIV/(2*I2SDIV+ODD) and a max of (I2SDIV+ODD)/(2*I2SDIV+ODD). Fs max is supported for each mode/condition.*

Figure 33. I²S slave timing diagram (Philips protocol)(1)



1. Measurement points are done at CMOS levels: $0.3 \times V_{DD}$ and $0.7 \times V_{DD}$.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 34. I²S master timing diagram (Philips protocol)(1)



1. Guaranteed by characterization results.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Table 64. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_S (5)	Sampling time	Direct channels 2.4 V ≤V_{DDA} ≤3.6 V	0.25	-	-	µs
		Multiplexed channels 2.4 V ≤V_{DDA} ≤3.6 V	0.56	-	-	
		Direct channels 1.8 V ≤V_{DDA} ≤2.4 V	0.56	-	-	
		Multiplexed channels 1.8 V ≤V_{DDA} ≤2.4 V	1	-	-	
		-	4	-	384	$1/f_{ADC}$
t_{CONV}	Total conversion time (including sampling time)	f_{ADC} = 16 MHz	1	-	24.75	µs
		-	4 to 384 (sampling phase) +12 (successive approximation)			$1/f_{ADC}$
C_{ADC}	Internal sample and hold capacitor	Direct channels	-	16	-	pF
		Multiplexed channels	-		-	
f_{TRIG}	External trigger frequency Regular sequencer	12-bit conversions	-	-	Tconv+1	$1/f_{ADC}$
		6/8/10-bit conversions	-	-	Tconv	$1/f_{ADC}$
f_{TRIG}	External trigger frequency Injected sequencer	12-bit conversions	-	-	Tconv+2	$1/f_{ADC}$
		6/8/10-bit conversions	-	-	Tconv+1	$1/f_{ADC}$
R_{AIN} (6)	Signal source impedance		-	-	50	kΩ
t_{lat}	Injection trigger conversion latency	f_{ADC} = 16 MHz	219	-	281	ns
		-	3.5	-	4.5	$1/f_{ADC}$
t_{latr}	Regular trigger conversion latency	f_{ADC} = 16 MHz	156	-	219	ns
		-	2.5	-	3.5	$1/f_{ADC}$
t_{STAB}	Power-up time	-	-	-	3.5	µs

1. The Vref+ input can be grounded if neither the ADC nor the DAC are used (this allows to shut down an external voltage reference).
2. The current consumption through VREF is composed of two parameters:

   - one constant (max 300 µA)

   - one variable (max 400 µA), only during sampling time + 2 first conversion pulses

   So, peak consumption is 300+400 = 700 µA and average consumption is 300 + [(4 sampling + 2) /16] x 400 = 450 µA at 1Msps
3. V_{REF+} can be internally connected to V_{DDA} and V_{REF-} can be internally connected to V_{SSA}, depending on the package. Refer to *Section 4: Pin descriptions* for further details.
4. V_{SSA} or V_{REF-} must be tied to ground.
5. Minimum sampling time is reached for an external input impedance limited to a value as defined in *Table 66: Maximum source impedance RAIN max*.
6. External impedance has another high value limitation when using short sampling time as defined in *Table 66: Maximum source impedance RAIN max*.

Figure 36. ADC accuracy characteristics

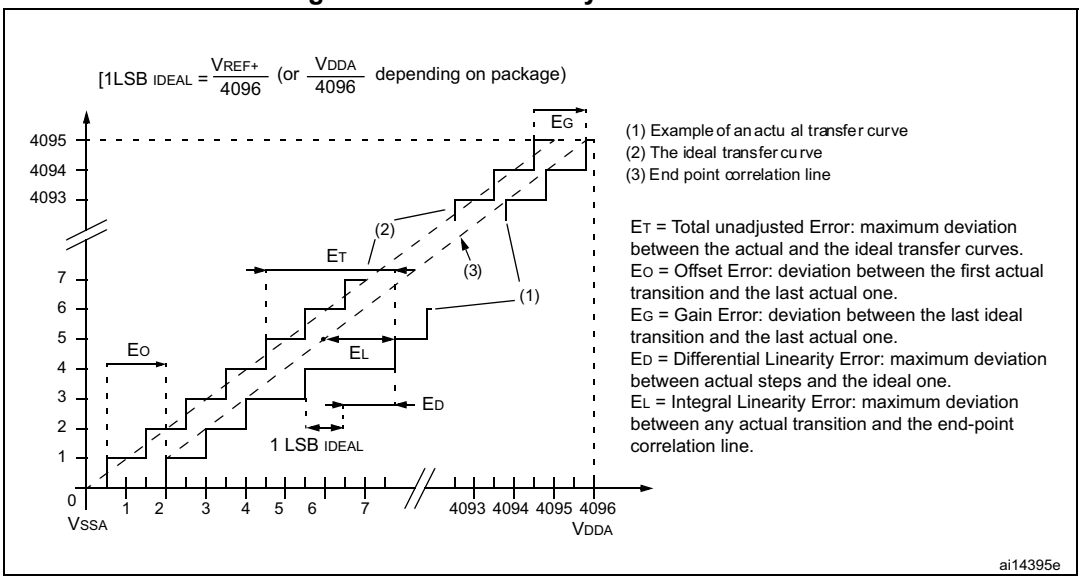
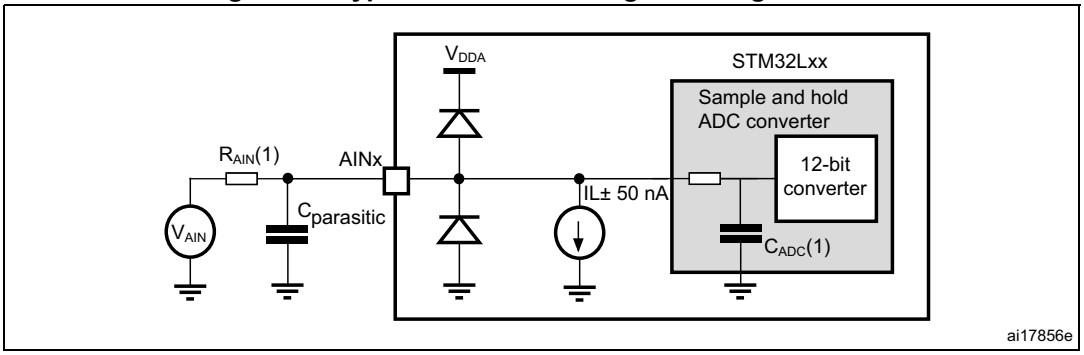


Figure 37. Typical connection diagram using the ADC



1. Refer to *Table 66: Maximum source impedance RAIN max* for the value of R_{AIN} and *Table 64: ADC characteristics* for the value of C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

6.3.20 DAC electrical specifications

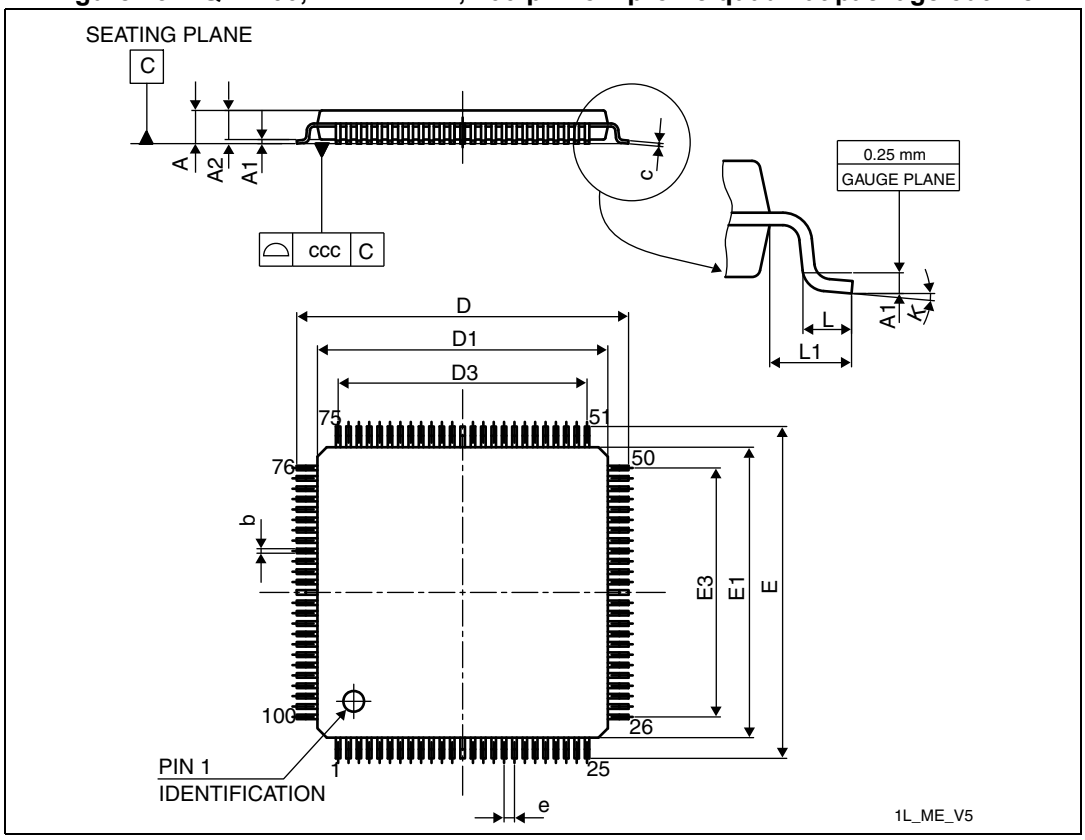
Data guaranteed by design, unless otherwise specified.

Table 67. DAC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.8	-	3.6	V
V_{REF+}	Reference supply voltage	V_{REF+} must always be below V_{DDA}	1.8	-	3.6	
V_{REF-}	Lower reference voltage	-	V_{SSA}			
$I_{DDVREF+}$(1)	Current consumption on V_{REF+} supply V_{REF+} = 3.3 V	No load, middle code (0x800)	-	130	220	µA
		No load, worst code (0x000)	-	220	350	
I_{DDA}(1)	Current consumption on V_{DDA} supply V_{DDA} = 3.3 V	No load, middle code (0x800)	-	210	320	
		No load, worst code (0xF1C)	-	320	520	
R_L(2)	Resistive load	DAC output buffer ON	5	-	-	kΩ
C_L(2)	Capacitive load		-	-	50	pF
R_O	Output impedance	DAC output buffer OFF	12	16	20	kΩ
V_{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON	0.2	-	V_{DDA} – 0.2	V
		DAC output buffer OFF	0.5	-	V_{REF+} – 1LSB	mV
DNL(1)	Differential non linearity(3)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON	-	1.5	3	LSB
		No R_L, $C_L \leq 50$ pF DAC output buffer OFF	-	1.5	3	
INL(1)	Integral non linearity(4)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON	-	2	4	
		No R_L, $C_L \leq 50$ pF DAC output buffer OFF	-	2	4	
Offset(1)	Offset error at code 0x800 (5)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON	-	±10	±25	
		No R_L, $C_L \leq 50$ pF DAC output buffer OFF	-	±5	±8	
Offset1(1)	Offset error at code 0x001(6)	No R_L, $C_L \leq 50$ pF DAC output buffer OFF	-	±1.5	±5	

7.2 LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package information

Figure 43. LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 75. LQPF100, 14 x 14 mm, 100-pin low-profile quad flat package mechanical data

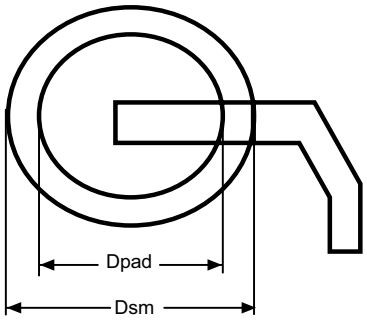
Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591

Table 77. UFBGA132, 7 x 7 mm, 132-ball ultra thin, fine-pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 50. UFBGA132, 7 x 7 mm, 132-ball ultra thin, fine-pitch ball grid array package recommended footprint



Pitch	0.5 mm
D pad	0.27 mm
Dsm	0.35 mm typ (depends on the soldermask registration tolerance)
Solder paste	0.27 mm aperture diameter

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