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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, I²S, POR, PWM, WDT
Number of I/O	51
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	12K x 8
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 21x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l151rdt7

List of figures

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32L151xD and STM32L152xD ultra-low-power ARM® Cortex®-M3 based microcontroller product line.

The STM32L151xD and STM32L152xD microcontrollers feature 384 Kbytes of Flash memory.

The ultra-low-power STM32L151xD and STM32L152xD family includes devices in 5 different package types: from 64 pins to 144 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the ultra-low-power STM32L151xD and STM32L152xD microcontroller family suitable for a wide range of applications:

- Medical and handheld equipment
- Application control and user interface
- PC peripherals, gaming, GPS and sport equipment
- Alarm systems, wired and wireless sensors, video intercom
- Utility metering

This STM32L151xD and STM32L152xD datasheet should be read in conjunction with the STM32L1xxxx reference manual (RM0038). The application note “Getting started with STM32L1xxxx hardware development” (AN3216) gives a hardware implementation overview. Both documents are available from the STMicroelectronics website *www.st.com*.

For information on the ARM® Cortex®-M3 core please refer to the ARM® Cortex®-M3 technical reference manual, available from the www.arm.com website. *Figure 1* shows the general block diagram of the device family.

2 Description

The ultra-low-power STM32L151xD and STM32L152xD devices incorporate the connectivity power of the universal serial bus (USB) with the high-performance ARM® Cortex®-M3 32-bit RISC core operating at a frequency of 32 MHz (33.3 DMIPS), a memory protection unit (MPU), high-speed embedded memories (Flash memory up to 384 Kbytes and RAM up to 48 Kbytes), a flexible static memory controller (FSMC) interface (for devices with packages of 100 pins and more) and an extensive range of enhanced I/Os and peripherals connected to two APB buses.

The STM32L151xD and STM32L152xD devices offer three operational amplifiers, one 12-bit ADC, two DACs, two ultra-low-power comparators, one general-purpose 32-bit timer, six general-purpose 16-bit timers and two basic timers, which can be used as time bases.

Moreover, the STM32L151xD and STM32L152xD devices contain standard and advanced communication interfaces: up to two I2Cs, three SPIs, two I2S, one SDIO, three USARTs, two UARTs, and an USB. The STM32L151xD and STM32L152xD devices offer up to 34 capacitive sensing channels to simply add a touch sensing functionality to any application.

They also include a real-time clock and a set of backup registers that remain powered in Standby mode.

Finally, the integrated LCD controller (except STM32L151xD devices) has a built-in LCD voltage generator that allows to drive up to 8 multiplexed LCDs with the contrast independent of the supply voltage.

The ultra-low-power STM32L151xD and STM32L152xD devices operate from a 1.8 to 3.6 V power supply (down to 1.65 V at power down) with BOR and from a 1.65 to 3.6 V power supply without BOR option. They are available in the -40 to +85 °C and -40 to +105 °C temperature ranges. A comprehensive set of power-saving modes allows the design of low-power applications.

Table 3. Functionalities depending on the operating power supply range (continued)

	Functionalities depending on the operating power supply range			
Operating power supply range	**DAC and ADC operation**	**USB**	**Dynamic voltage scaling range**	**I/O operation**
V_{DD}=V_{DDA} = 2.0 to 2.4 V	Conversion time up to 500 Ksps	Functional(2)	Range 1, Range 2 or Range 3	Full speed operation
V_{DD}=V_{DDA} = 2.4 to 3.6 V	Conversion time up to 1 Msps	Functional(2)	Range 1, Range 2 or Range 3	Full speed operation

1. CPU frequency changes from initial to final must respect "F_{CPU} initial < 4*F_{CPU} final" to limit V_{CORE} drop due to current consumption peak when frequency increases. It must also respect 5 µs delay between two changes. For example to switch from 4.2 MHz to 32 MHz, the user can switch from 4.2 MHz to 16 MHz, wait 5 µs, then switch from 16 MHz to 32 MHz.
2. Should be USB compliant from I/O voltage standpoint, the minimum V_{DD} is 3.0 V.

Table 4. CPU frequency range depending on dynamic voltage scaling

CPU frequency range	Dynamic voltage scaling range
16 MHz to 32 MHz (1ws) 32 kHz to 16 MHz (0ws)	Range 1
8 MHz to 16 MHz (1ws) 32 kHz to 8 MHz (0ws)	Range 2
2.1MHz to 4.2 MHz (1ws) 32 kHz to 2.1 MHz (0ws)	Range 3

3.4 Clock management

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- **Clock prescaler**: to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Safe clock switching**: clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management**: to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source**: three different clock sources can be used to drive the master clock SYSCLK:
  - 1-24 MHz high-speed external crystal (HSE), that can supply a PLL
  - 16 MHz high-speed internal RC oscillator (HSI), trimmable by software, that can supply a PLL
  - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 7 frequencies (65 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.1 MHz, 4.2 MHz). When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be trimmed by software down to a ±0.5% accuracy.
- **Auxiliary clock source**: two ultra-low-power clock sources that can be used to drive the LCD controller and the real-time clock:
  - 32.768 kHz low-speed external crystal (LSE)
  - 37 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock can be measured using the high-speed internal RC oscillator for greater precision.
- **RTC and LCD clock sources:** the LSI, LSE or HSE sources can be chosen to clock the RTC and the LCD, whatever the system clock.
- **USB clock source:** the embedded PLL has a dedicated 48 MHz clock output to supply the USB interface.
- **Startup clock:** after reset, the microcontroller restarts by default with an internal 2 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** this feature can be enabled by software. If a HSE clock failure occurs, the master clock is automatically switched to HSI and a software interrupt is generated if enabled.
- **Clock-out capability (MCO: microcontroller clock output):** it outputs one of the internal clocks for external use by the application.

Several prescalers allow the configuration of the AHB frequency, each APB (APB1 and APB2) domains. The maximum frequency of the AHB and the APB domains is 32 MHz. See *Figure 2* for details on the clock tree.

3.7 Memories

The STM32L151xD and STM32L152xD devices have the following features:

- 48 Kbytes of embedded RAM accessed (read/write) at CPU clock speed with 0 wait states. With the enhanced bus matrix, operating the RAM does not lead to any performance penalty during accesses to the system bus (AHB and APB buses).
- The non-volatile memory is divided into three arrays:
  - 384 Kbytes of embedded Flash program memory
  - 12 Kbytes of data EEPROM
  - Options bytes

  Flash program and data EEPROM are divided into two banks, this enables writing in one bank while running code or reading data in the other bank.

  The options bytes are used to write-protect or read-out protect the memory (with 4 Kbytes granularity) and/or readout-protect the whole memory with the following options:
  - Level 0: no readout protection
  - Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
  - Level 2: chip readout protection, debug features (ARM Cortex-M3 JTAG and serial wire) and boot in RAM selection disabled (JTAG fuse)

  The whole non-volatile memory embeds the error correction code (ECC) feature.

3.8 FSMC (flexible static memory controller)

The FSMC supports the following modes: SRAM, PSRAM, NOR/OneNAND Flash.

Functionality overview:

- Up to 26 bit address bus
- Up to 16-bit data bus
- Write FIFO
- Burst mode
- Code execution from external memory
- Four chip select signals
- Up to 32 MHz external access

3.9 DMA (direct memory access)

The flexible 12-channel, general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with software trigger support for each channel. Configuration is done by software and transfer sizes between source and destination are independent.

from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode. See *Table 69: Temperature sensor calibration values*.

3.11.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and Comparators. V_{REFINT} is internally connected to the ADC_IN17 input channel. It enables accurate monitoring of the V_{DD} value (when no external voltage, VREF+, is available for ADC). The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode. See *Table 15: Embedded internal reference voltage calibration values*.

3.12 DAC (digital-to-analog converter)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in non-inverting configuration.

This dual digital Interface supports the following features:

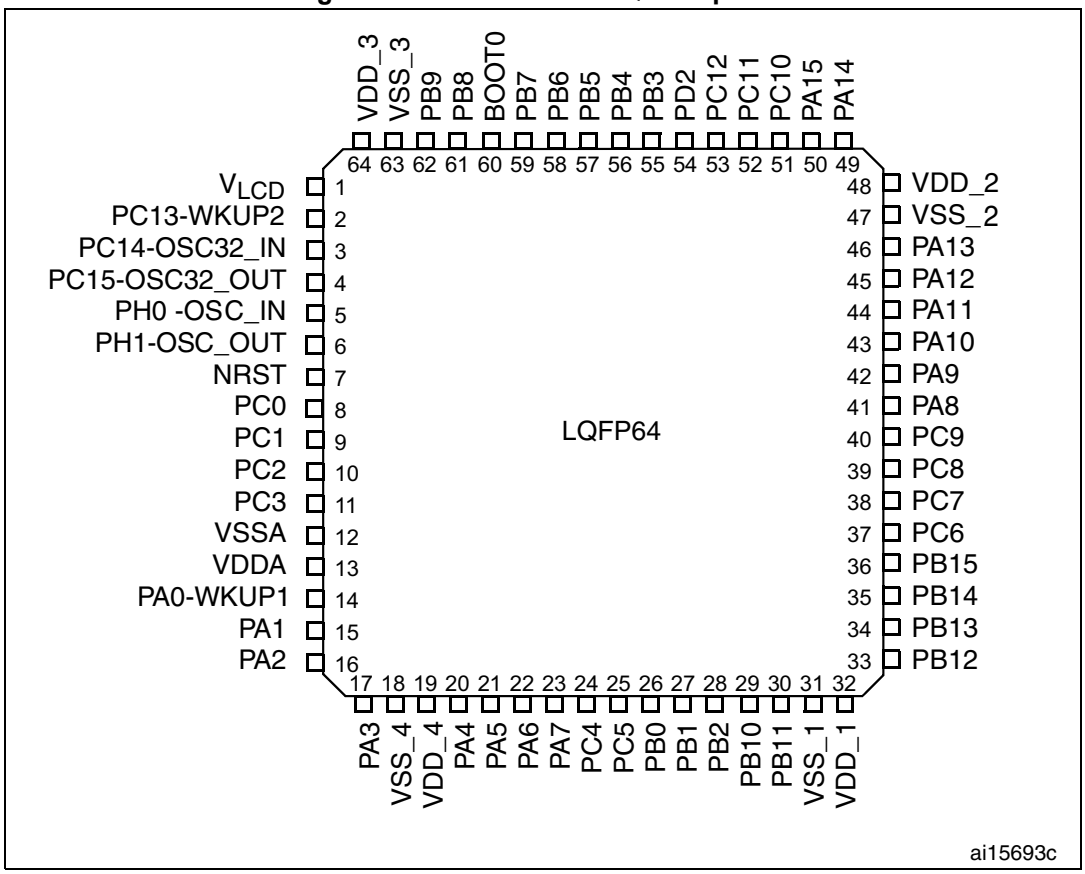
- Two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channels, independent or simultaneous conversions
- DMA capability for each channel (including the underrun interrupt)
- External triggers for conversion
- Input reference voltage V_{REF+}

Eight DAC trigger inputs are used in the STM32L151xD and STM32L152xD devices. The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

3.13 Operational amplifier

The STM32L151xD and STM32L152xD devices embed three operational amplifiers with external or internal follower routing capability (or even amplifier and filter capability with external components). When one operational amplifier is selected, one external ADC channel is used to enable output measurement.

Figure 6. STM32L15xRD LQFP64 pinout



1. This figure shows the package top view.

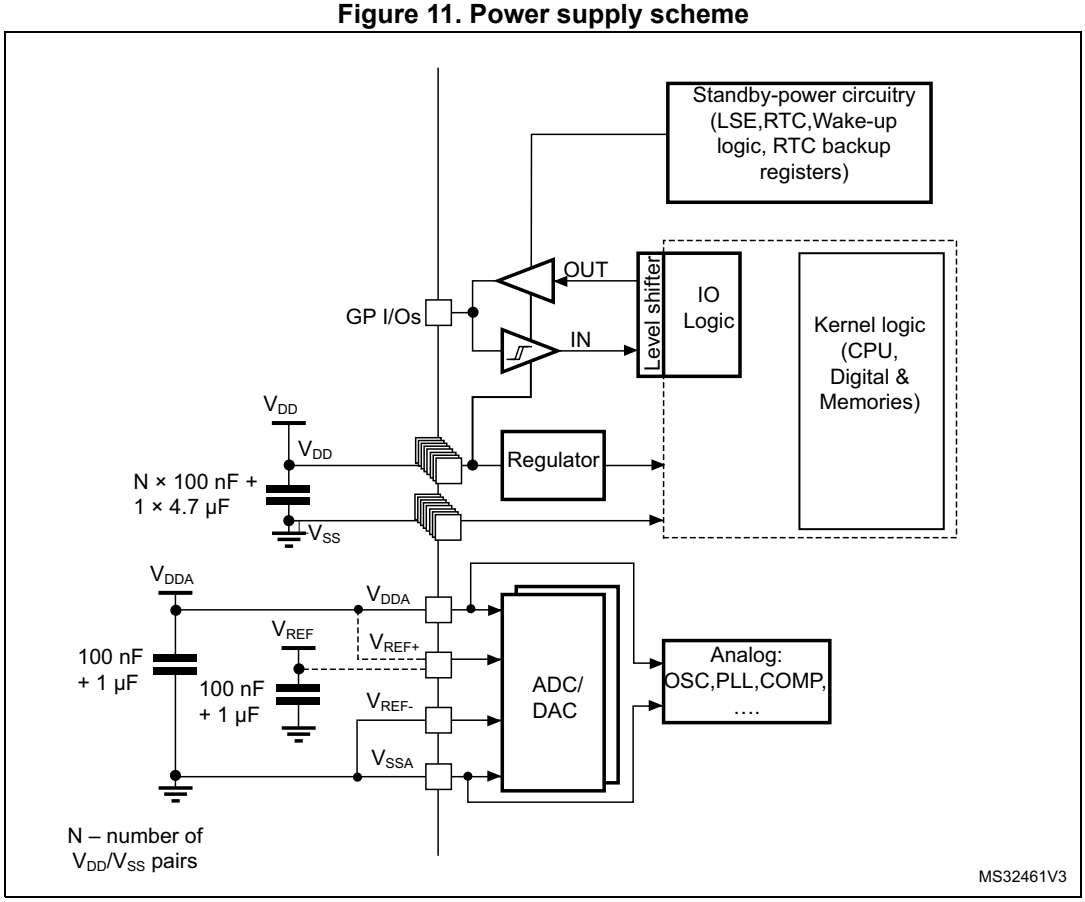
Alternate functions

Table 9. Alternate function input/output

Port name	Digital alternate function number									..			..		
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFIO6	AFIO7	AFIO8		AFIO11	AFIO12		AFIO14	AFIO15
	Alternate function														
	SYSTEM	TIM2	TIM3/4/5	TIM9/ 10/11	I2C1/2	SPI1/2	SPI3	USART1/2/3	UART4/5		LCD	FSMC/ SDIO		CPRI	SYSTEM
BOOT0	BOOT0	-	-	-	-	-	-	-	-		-	-		-	EVENT OUT
NRST	NRST	-	-	-	-	-	-	-	-		-	-		-	-
PA0-WKUP1	-	TIM2_CH1_ETR	TIM5_CH1	-	-	-	-	USART2_CTS	-		-	-		TIMx_IC1	EVENT OUT
PA1	-	TIM2_CH2	TIM5_CH2	-	-	-	-	USART2_RTS	-		SEG0	-		TIMx_IC2	EVENT OUT
PA2	-	TIM2_CH3	TIM5_CH3	TIM9_CH1	-	-	-	USART2_TX	-		SEG1	-		TIMx_IC3	EVENT OUT
PA3	-	TIM2_CH4	TIM5_CH4	TIM9_CH2	-	-	-	USART2_RX	-		SEG2	-		TIMx_IC4	EVENT OUT
PA4	-	-	-	-	-	SPI1_NSS	SPI3_NSS I2S3_WS	USART2_CK	-		-	-		TIMx_IC1	EVENT OUT
PA5	-	TIM2_CH1_ETR	-	-	-	SPI1_SCK	-	-	-		-	-		TIMx_IC2	EVENT OUT
PA6	-	-	TIM3_CH1	TIM10_ CH1	-	SPI1_MISO	-	-	-		SEG3	-		TIMx_IC3	EVENT OUT
PA7	-	-	TIM3_CH2	TIM11_ CH1	-	SPI1_MOSI	-	-	-		SEG4	-		TIMx_IC4	EVENT OUT
PA8	MCO	-	-	-	-	-	-	USART1_CK	-		COM0	-		TIMx_IC1	EVENT OUT
PA9	-	-	-	-	-	-	-	USART1_TX	-		COM1	-		TIMx_IC2	EVENT OUT
PA10	-	-	-	-	-	-	-	USART1_RX	-		COM2	-		TIMx_IC3	EVENT OUT
PA11	-	-	-	-	-	SPI1_MISO		USART1_CTS	-		-	-		TIMx_IC4	EVENT OUT

6.1.6 Power supply scheme

Figure 11. Power supply scheme



6.3.3 Embedded internal reference voltage

The parameters given in *Table 16* are based on characterization results, unless otherwise specified.

Table 15. Embedded internal reference voltage calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 30 °C ±5 °C V_{DDA}= 3 V ±10 mV	0x1FF8 00F8 - 0x1FF8 00F9

Table 16. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{REFINT\ out}$ (1)	Internal reference voltage	– 40 °C < T_J < +110 °C	1.202	1.224	1.242	V
I_{REFINT}	Internal reference current consumption	-	-	1.4	2.3	µA
$T_{VREFINT}$	Internal reference startup time	-	-	2	3	ms
V_{VREF_MEAS}	V_{DDA} and V_{REF+} voltage during V_{REFINT} factory measure	-	2.99	3	3.01	V
A_{VREF_MEAS}	Accuracy of factory-measured V_{REF} value(2)	Including uncertainties due to ADC and V_{DDA}/V_{REF+} values	-	-	±5	mV
T_{Coeff}(3)	Temperature coefficient	–40 °C < T_J < +110 °C	-	25	100	ppm/°C
A_{Coeff}(3)	Long-term stability	1000 hours, T= 25 °C	-	-	1000	ppm
$V_{DDCoeff}$(3)	Voltage coefficient	3.0 V < V_{DDA} < 3.6 V	-	-	2000	ppm/V
$T_{S\_vrefint}$(3)	ADC sampling time when reading the internal reference voltage	-	4	-	-	µs
T_{ADC_BUF}(3) (4)	Startup time of reference voltage buffer for ADC	-	-	-	10	µs
I_{BUF_ADC}(3)	Consumption of reference voltage buffer for ADC	-	-	13.5	25	µA
I_{VREF_OUT}(3)	VREF_OUT output current (5)	-	-	-	1	µA
C_{VREF_OUT}(3)	VREF_OUT output load	-	-	-	50	pF
I_{LPBUF}(3)	Consumption of reference voltage buffer for VREF_OUT and COMP	-	-	730	1200	nA
V_{REFINT_DIV1}(3)	1/4 reference voltage	-	24	25	26	% V_{REFINT}
V_{REFINT_DIV2}(3)	1/2 reference voltage	-	49	50	51	
V_{REFINT_DIV3}(3)	3/4 reference voltage	-	74	75	76	

1. Guaranteed by test in production.
2. The internal V_{REF} value is individually measured in production and stored in dedicated EEPROM bytes.
3. Guaranteed by characterization results.
4. Shortest sampling time can be determined in the application by multiple iterations.

Table 44. Synchronous non-multiplexed PSRAM write timings(1) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{d(CLKL-NWEH)}$	FSMC_CLK low to FSMC_NWE high	5	-	ns
$t_{d(CLKL-DATA)}$	FSMC_D[15:0] valid data after FSMC_CLK low	-	7	ns
$t_{d(CLKL-NBLH)}$	FSMC_CLK low to FSMC_NBL high	3	-	ns
$t_{su(NWAITV-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	6	-	ns
$t_{h(CLKH-NWAITV)}$	FSMC_NWAIT valid after FSMC_CLK high	0	-	ns

1. C_L = 30 pF.

USB characteristics

The USB interface is USB-IF certified (full speed).

Table 58. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

1. Guaranteed by design.

Table 59. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min.(1)	Max.(1)	Unit
Input levels					
V_{DD}	USB operating voltage	-	3.0	3.6	V
V_{DI}(2)	Differential input sensitivity	I(USB_DP, USB_DM)	0.2	-	V
V_{CM}(2)	Differential common mode range	Includes V_{DI} range	0.8	2.5	
V_{SE}(2)	Single ended receiver threshold	-	1.3	2.0	
Output levels					
V_{OL}(3)	Static output level low	R_L of 1.5 kΩ to 3.6 V(4)	-	0.3	V
V_{OH}(3)	Static output level high	R_L of 15 kΩ to V_{SS}(4)	2.8	3.6	

1. All the voltages are measured from the local ground potential.
2. Guaranteed by characterization results.
3. Guaranteed by test in production.
4. R_L is the load connected on the USB drivers.

Figure 32. USB timings: definition of data signal rise and fall time

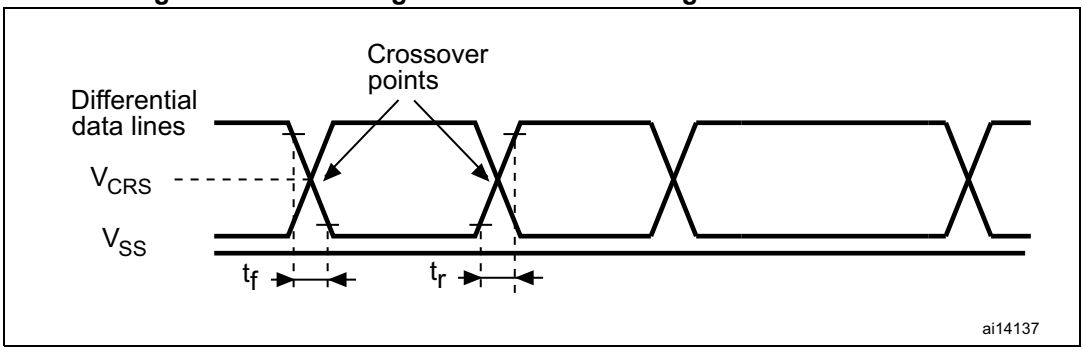


Table 60. USB: full speed electrical characteristics

Driver characteristics(1)					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_r	Rise time(2)	C_L = 50 pF	4	20	ns
t_f	Fall Time(2)	C_L = 50 pF	4	20	ns

6.3.22 Temperature sensor characteristics

Table 69. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C ±5 °C V_{DDA}= 3 V ±10 mV	0x1FF8 00FA - 0x1FF8 00FB
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C ±5 °C V_{DDA}= 3 V ±10 mV	0x1FF8 00FE - 0x1FF8 00FF

Table 70. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	1.48	1.61	1.75	mV/°C
V_{110}	Voltage at 110°C ±5°C(2)	612	626.8	641.5	mV
$I_{DDA(TEMP)}$(3)	Current consumption	-	3.4	6	µA
t_{START}(3)	Startup time	-	-	10	µs
T_{S_temp}(3)	ADC sampling time when reading the temperature	4	-	-	

1. Guaranteed by characterization results.
2. Measured at V_{DD} = 3 V ±10 mV. V110 ADC conversion result is stored in the TS_CAL2 byte.
3. Guaranteed by design.

6.3.23 Comparator

Table 71. Comparator 1 characteristics

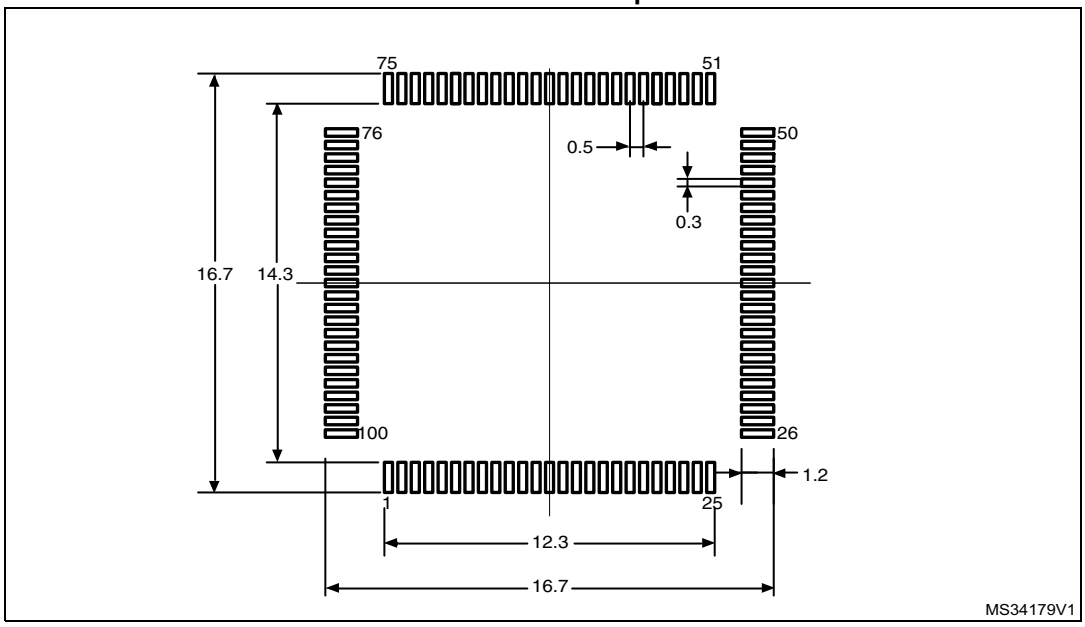
Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	-	1.65		3.6	V
R_{400K}	R_{400K} value	-	-	400	-	kΩ
R_{10K}	R_{10K} value	-	-	10	-	
V_{IN}	Comparator 1 input voltage range	-	0.6	-	V_{DDA}	V
t_{START}	Comparator startup time	-	-	7	10	µs
td	Propagation delay(2)	-	-	3	10	
Voffset	Comparator offset	-	-	±3	±10	mV
$d_{Voffset}/dt$	Comparator offset variation in worst voltage stress conditions	V_{DDA} = 3.6 V V_{IN+} = 0 V V_{IN-} = V_{REFINT} T_A = 25 °C	0	1.5	10	mV/1000 h
I_{COMP1}	Current consumption(3)	-	-	160	260	nA

Table 75. LQPF100, 14 x 14 mm, 100-pin low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 44. LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package recommended footprint

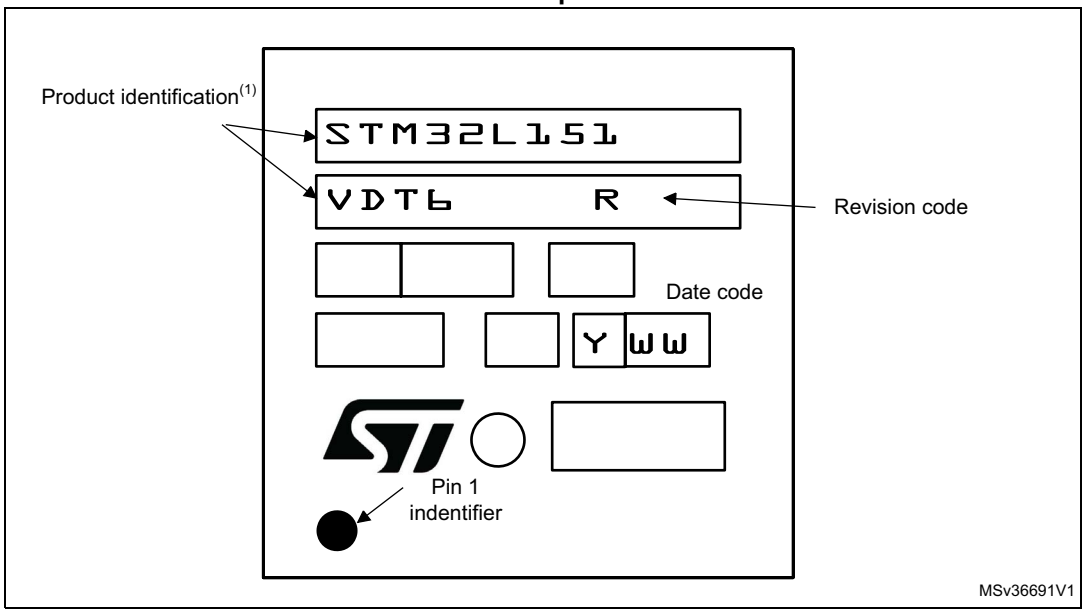


1. Dimensions are in millimeters.

Marking of engineering samples

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 45. LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity

Table 82. Document revision history (continued)

Date	Revision	Changes
18-Apr-2012	3	Added WLCSP64 package. *Section 3: Functional overview*: changed '128 kHz' to '131 kHz' in section "Low power run mode". *Section 3.17.1: General-purpose timers (TIM2, TIM3, TIM4, TIM5, TIM9, TIM10 and TIM11)*: changed 'six' to 'seven' synchronizable general-purpose timers. *Table 14: STM32L15xxD pin definitions on page 52*: updated name of reference manual in footnote *5.* I2C updated: footnote *3.* from *Table 58* Note about I2C clock updated: footnote *2.* from *Table 58* modified. Note [non-robust] updated: footnote *2.* from *Table 68* modified. GPIOs high current capability updated: *Section 3.6: GPIOs (general-purpose inputs/outputs)* 'except for analog inputs' was removed.
15-Jun-2012	4	Changed maximum number of touch sensing channels to 34, and updated *Table 4: Ultra-low-power STM32L15xxD device features and peripheral counts*. Updated *Section 3.10: ADC (analog-to-digital converter)* to add *Section 3.10.1: Temperature sensor* and *Section 3.10.2: Internal voltage reference (VREFINT)*. Removed caution note below *Figure 8: Power supply scheme*. Added note below *Table 4: STM32L15xQD STM32L162QD UFBGA132 ballout*. Modified *Table 8: STM32L15xRDSTM32L162RD WLCSP64 ballout* to match top view. Changed FSMC_LBAR into FSMC_NADV, and I2C1_SMBAI into I2C1_SMBA in *Table 14: STM32L15xxD pin definitions*. Modified PB10/11/12 for AFIO4 ction, and replaced LBAR by NADV for AFIO12 in *Table 19: ction input/output*. Updated *Table 22: Typical and maximum current consumptions in Stop mode* and added *Note 6*. Updated *Table 23: Typical and maximum current consumptions in Standby mode*. Updated t_{WUSTOP} in *Table :* . Updated *Table 27: Peripheral current consumption*. Updated *Table 60: SPI characteristics*, added *Note 1* and *Note 3*, and applied *Note 2* to $t_{r(SCK)}$, $t_{f(SCK)}$, $t_{w(SCKH)}$, $t_{w(SCKL)}$, $t_{su(MI)}$, $t_{su(SI)}$, $t_{h(MI)}$, and $t_{h(SI)}$. Updated I_{DD} maximum value in *Table 38: Flash memory and data EEPROM characteristics*.

Table 82. Document revision history (continued)

Date	Revision	Changes
25-Oct-2012	5	Updated Features Updated *Figure 1: Ultra-low-power STM32L162xC block diagram* Added *Table 4: Functionalities depending on the working mode (from Run/active down to standby)*, and *Table 3: ange depending on dynamic voltage scaling* Updated *Figure 3: STM32L162VC LQFP100 pinout* Updated *Table 14: STM32L15xxD pin definitions* Added *Note 2* in *Table 15: Embedded reset and power control block characteristics* Replaced TBD values in *Table 30: Low-speed external user clock characteristics*, *Table 38: Flash memory and data EEPROM characteristics* and *Table 55: I/O AC characteristics* Added *Table 61: I2S characteristics*, *Figure 29: I2S slave timing diagram (Philips protocol)(1)* and *Figure 30: I2S master timing diagram (Philips protocol)(1)* Added *Table 62: SDIO characteristics* Added *Figure 31: SDIO timings* Updated *Section 6.3.9: FSMC characteristics* Updated *Table 72: Temperature sensor characteristics* Added *Figure 40: Thermal resistance*
01-Feb-2013	6	Removed AHB1/AHB2 and corrected typo on APB1/APB2 in *Figure 1: Ultra-low-power STM32L162xC block diagram* Updated “OP amp” line in *Table 4: Functionalities depending on the working mode (from Run/active down to standby)* Added IWDG and WWDG rows in *Table 4: Functionalities depending on the working mode (from Run/active down to standby)* Added OneNAND support in *Section 3.8: FSMC (flexible static memory controller)* The comment "HSE = 16 MHz(2) (PLL ON for fHCLK above 16 MHz)" replaced by "fHSE = fHCLK up to 16 MHz included, fHSE = fHCLK/2 above 16 MHz (PLL ON)(2)” in table *Table 19: Current consumption in Sleep mode* Updated Stop mode current to 1.5 µA in *Ultra low power platform* Replaced BGA132 by UFBGA132 in *Table 4: Ultra-low-power STM32L15xxD device features and peripheral counts* Replaced BGA132 by UFBGA132 in *Figure 4: STM32L15xQD STM32L162QD UFBGA132 ballout* Updated entire *Section 7: Package characteristics*