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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	109
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	12K x 8
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 40x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	132-UFBGA
Supplier Device Package	132-UFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l152qdh6

- **Stop** mode without RTC

  Stop mode achieves the lowest power consumption while retaining the RAM and register contents. All clocks are stopped, the PLL, MSI RC, HSI and LSI RC, LSE and HSE crystal oscillators are disabled. The voltage regulator is in the low-power mode. The device can be woken up from Stop mode by any of the EXTI line, in 8 µs. The EXTI line source can be one of the 16 external lines. It can be the PVD output, the Comparator 1 event or Comparator 2 event (if internal reference voltage is on). It can also be wakened by the USB wakeup.

- **Standby** mode with RTC

  Standby mode is used to achieve the lowest power consumption and real time clock. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI RC and HSE crystal oscillators are also switched off. The LSE or LSI is still running. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC_CSR).

  The device exits Standby mode in 60 µs when an external reset (NRST pin), an IWDG reset, a rising edge on one of the three WKUP pins, RTC alarm (Alarm A or Alarm B), RTC tamper event, RTC timestamp event or RTC Wakeup event occurs.

- **Standby** mode without RTC

  Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire V_{CORE} domain is powered off. The PLL, MSI RC, HSI and LSI RC, HSE and LSE crystal oscillators are also switched off. After entering Standby mode, the RAM and register contents are lost except for registers in the Standby circuitry (wakeup logic, IWDG, RTC, LSI, LSE Crystal 32K osc, RCC_CSR).

  The device exits Standby mode in 60 µs when an external reset (NRST pin) or a rising edge on one of the three WKUP pin occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped automatically by entering Stop or Standby mode.

Table 3. Functionalities depending on the operating power supply range

	Functionalities depending on the operating power supply range			
Operating power supply range	**DAC and ADC operation**	**USB**	**Dynamic voltage scaling range**	**I/O operation**
V_{DD}= V_{DDA} = 1.65 to 1.71 V	Not functional	Not functional	Range 2 or Range 3	Degraded speed performance
V_{DD}=V_{DDA}= 1.71 to 1.8 V(1)	Not functional	Not functional	Range 1, Range 2 or Range 3	Degraded speed performance
V_{DD}=V_{DDA}= 1.8 to 2.0 V(1)	Conversion time up to 500 Ksps	Not functional	Range 1, Range 2 or Range 3	Degraded speed performance

The DMA can be used with the main peripherals: SPI, I^2C, USART, SDIO, general-purpose timers, DAC and ADC.

3.10 LCD (liquid crystal display)

The LCD drives up to 8 common terminals and 44 segment terminals to drive up to 320 pixels.

- Internal step-up converter to guarantee functionality and contrast control irrespective of V_{DD}. This converter can be deactivated, in which case the V_{LCD} pin is used to provide the voltage to the LCD
- Supports static, 1/2, 1/3, 1/4 and 1/8 duty
- Supports static, 1/2, 1/3 and 1/4 bias
- Phase inversion to reduce power consumption and EMI
- Up to 8 pixels can be programmed to blink
- Unneeded segments and common pins can be used as general I/O pins
- LCD RAM can be updated at any time owing to a double-buffer
- The LCD controller can operate in Stop mode

3.11 ADC (analog-to-digital converter)

A 12-bit analog-to-digital converters is embedded into STM32L151xD and STM32L152xD devices with up to 40 external channels, performing conversions in single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs with up to 28 external channels in a group.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all scanned channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start triggers, to allow the application to synchronize A/D conversions and timers. An injection mode allows high priority conversions to be done by interrupting a scan mode which runs in as a background task.

The ADC includes a specific low-power mode. The converter is able to operate at maximum speed even if the CPU is operating at a very low frequency and has an auto-shutdown function. The ADC's runtime and analog front-end current consumption are thus minimized whatever the MCU operating mode.

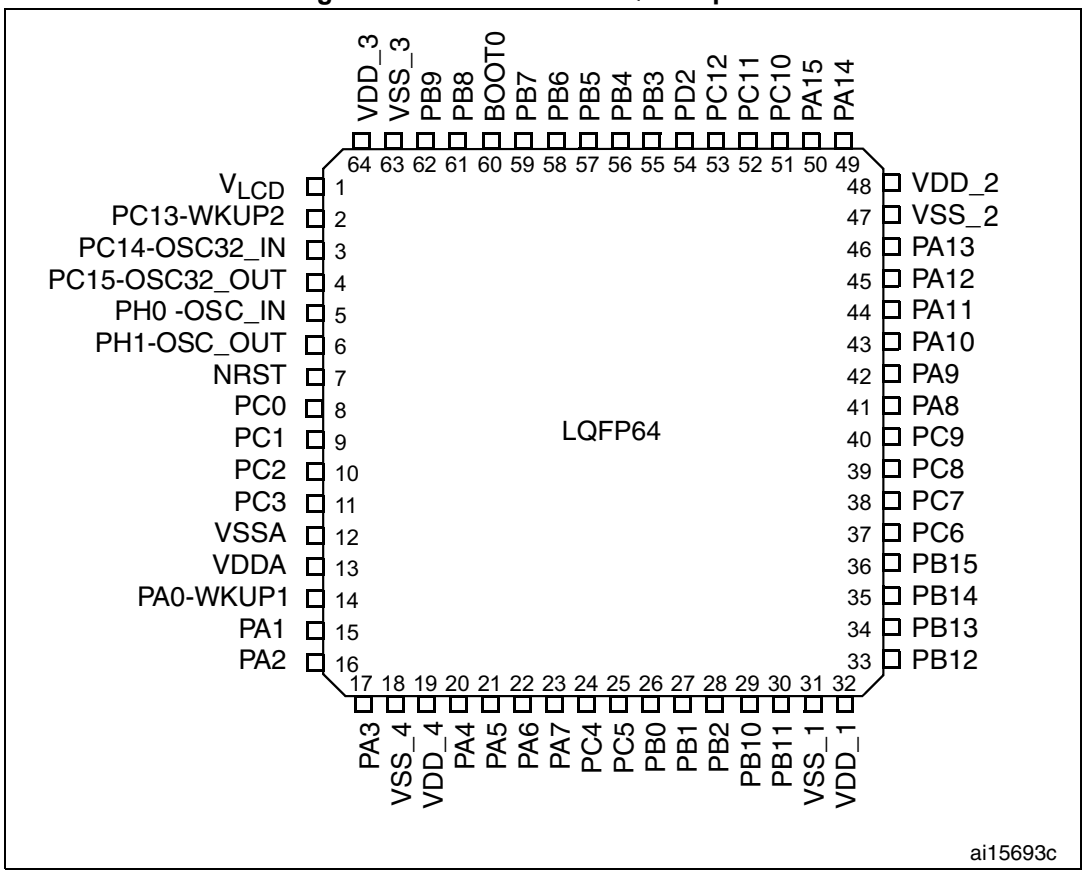
3.11.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

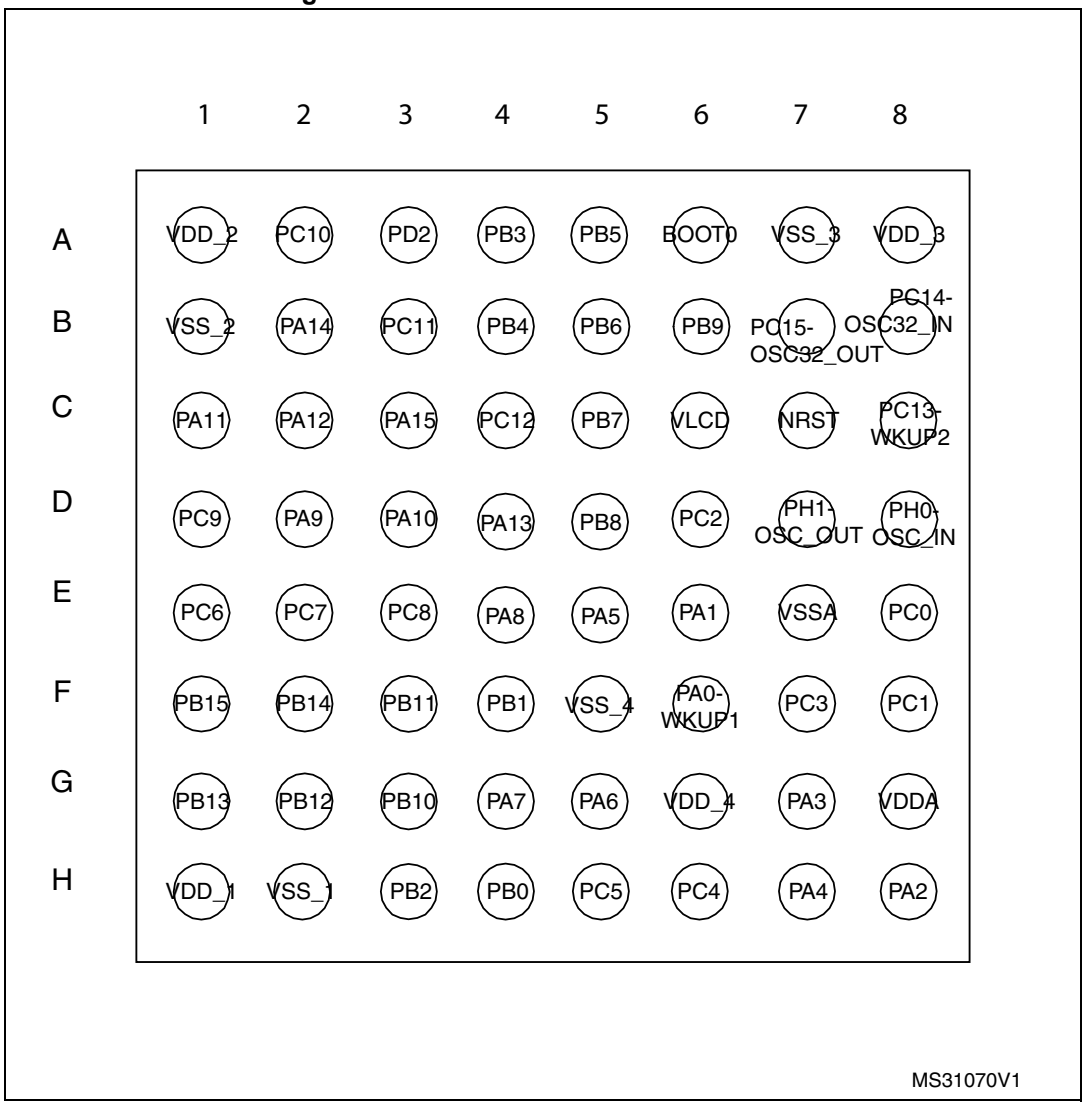
The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies

Figure 6. STM32L15xRD LQFP64 pinout



1. This figure shows the package top view.

Figure 7. STM32L15xRD WLCSP64 ballout



1. This figure shows the package top view.

Table 7. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	FT	5 V tolerant I/O
	TC	Standard 3.3 V I/O
	B	Dedicated BOOT0 pin
	RST	Bidirectional reset pin with embedded weak pull-up resistor

Table 9. Alternate function input/output (continued)

Port name	Digital alternate function number									..			..		
	AFIO0	AFIO1	AFIO2	AFIO3	AFIO4	AFIO5	AFIO6	AFIO7	AFIO8		AFIO11	AFIO12		AFIO14	AFIO15
	Alternate function														
	SYSTEM	TIM2	TIM3/4/5	TIM9/ 10/11	I2C1/2	SPI1/2	SPI3	USART1/2/3	UART4/5		LCD	FSMC/ SDIO		CPRI	SYSTEM
PB11	-	TIM2_CH4	-	-	I2C2_SDA	-	-	USART3_RX	-		SEG11	-		-	EVENT OUT
PB12	-	-	-	TIM10_CH1	I2C2_SMBA	SPI2_NSS I2S2_WS	-	USART3_CK	-		SEG12	-		-	EVENT OUT
PB13	-	-	-	TIM9_CH1	-	SPI2_SCK I2S2_CK	-	USART3_CTS	-		SEG13	-		-	EVENT OUT
PB14	-	-	-	TIM9_CH2	-	SPI2_MISO	-	USART3_RTS	-		SEG14	-		-	EVENT OUT
PB15	-	-	-	TIM11_CH1	-	SPI2_MOSI I2S2_SD	-	-	-		SEG15	-		-	EVENT OUT
PC0	-	-	-	-	-		-	-	-		SEG18	-		TIMx_IC1	EVENT OUT
PC1	-	-	-	-	-	-	-	-	-		SEG19	-		TIMx_IC2	EVENT OUT
PC2	-	-	-	-	-	-	-	-	-		SEG20	-		TIMx_IC3	EVENT OUT
PC3	-	-	-	-	-	-	-	-	-		SEG21	-		TIMx_IC4	EVENT OUT
PC4	-	-	-	-	-	-	-	-	-		SEG22	-		TIMx_IC1	EVENT OUT
PC5	-	-	-	-	-	-	-	-	-		SEG23	-		TIMx_IC2	EVENT OUT
PC6	-	-	TIM3_CH1	-	-	I2S2_MCK	-	-	-		SEG24	SDIO_D6		TIMx_IC3	EVENT OUT
PC7	-	-	TIM3_CH2	-	-	-	I2S3_MCK	-	-		SEG25	SDIO_D7		TIMx_IC4	EVENT OUT
PC8	-	-	TIM3_CH3	-	-	-	-	-	-		SEG26	SDIO_D0		TIMx_IC1	EVENT OUT
PC9	-	-	TIM3_CH4	-	-	-	-	-	-		SEG27	SDIO_D1		TIMx_IC2	EVENT OUT

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.6 V (for the 1.65 V ≤V_{DD} ≤3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 9*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 10*.

Figure 9. Pin loading conditions

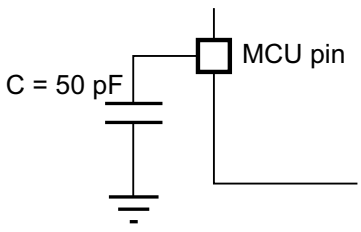


Figure 10. Pin input voltage

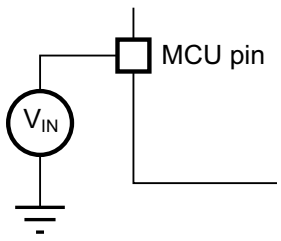


Table 19. Current consumption in Sleep mode

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max (1)	Unit
$I_{DD(SLEEP)}$	Supply current in Sleep mode, code executed from RAM, Flash switched OFF	f_{HSE} = f_{HCLK} up to 16 MHz, included f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)(2)	Range3, Vcore=1.2 V VOS[1:0]=11	1	58	220	µA
				2	96	300	
				4	170	380	
			Range2, Vcore=1.5 V VOS[1:0]=10	4	210	500	
				8	400	700	
				16	810	1100	
			Range1, Vcore=1.8 V VOS[1:0]=01	8	485	800	
				16	955	1250	
				32	2100	2700	
		HSI clock source (16 MHz)	Range2, Vcore=1.5 V VOS[1:0]=10	16	835	1100	
			Range1, Vcore=1.8 V VOS[1:0]=01	32	2100	2700	
		MSI clock, 65 kHZ	Range3, Vcore=1.2 V VOS[1:0]=11	0.065	18.5	72	
		MSI clock, 524 kHZ		0.524	37	92	
		MSI clock, 4.2 MHZ		4.2	180	273	
	Supply current in Sleep mode, Flash switched ON	f_{HSE} = f_{HCLK} up to 16 MHz, included f_{HSE} = f_{HCLK}/2 above 16MHz (PLL ON)(2)	Range3, Vcore=1.2 V VOS[1:0]=11	1	75	250	
				2	115	300	
				4	200	380	
			Range2, Vcore=1.5 V VOS[1:0]=10	4	230	500	
				8	430	700	
				16	840	1120	
			Range1, Vcore=1.8 V VOS[1:0]=01	8	500	800	
				16	980	1300	
				32	2100	2700	
		HSI clock source (16 MHz)	Range2, Vcore=1.5 V VOS[1:0]=10	16	860	1160	
			Range1, Vcore=1.8 V VOS[1:0]=01	32	2150	2800	
		MSI clock, 65 kHZ	Range3, Vcore=1.2 V VOS[1:0]=11	0.065	33,5	90	
		MSI clock, 524 kHZ		0.524	53	110	
		MSI clock, 4.2 MHZ		4.2	200	290	

1. Guaranteed by characterization results, unless otherwise specified.

2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register)

Table 20. Current consumption in Low-power run mode

Symbol	Parameter	Conditions			Typ	Max(1)	Unit
$I_{DD\ (LP\ Run)}$	Supply current in Low-power run mode	All peripherals OFF, code executed from RAM, Flash switched OFF, V_{DD} from 1.65 V to 3.6 V	MSI clock, 65 kHz f_{HCLK} = 32 kHz	T_A = -40 °C to 25 °C	11	14	µA
				T_A = 85 °C	26	32	
				T_A = 105 °C	53	72	
			MSI clock, 65 kHz f_{HCLK} = 65 kHz	T_A =-40 °C to 25 °C	18	21	
				T_A = 85 °C	33	40	
				T_A = 105 °C	60	78	
			MSI clock, 131 kHz f_{HCLK} = 131 kHz	T_A = -40 °C to 25 °C	36	41	
				T_A = 55 °C	39	44	
				T_A = 85 °C	50	58	
				T_A = 105 °C	78	95	
		All peripherals OFF, code executed from Flash, V_{DD} from 1.65 V to 3.6 V	MSI clock, 65 kHz f_{HCLK} = 32 kHz	T_A = -40 °C to 25 °C	36	40.5	
				T_A = 85 °C	53	60	
				T_A = 105 °C	81	100	
			MSI clock, 65 kHz f_{HCLK} = 65 kHz	T_A = -40 °C to 25 °C	44	49	
				T_A = 85 °C	61	67	
				T_A = 105 °C	89	107	
			MSI clock, 131 kHz f_{HCLK} = 131 kHz	T_A = -40 °C to 25 °C	64	71	
				T_A = 55 °C	68	73	
				T_A = 85 °C	80	88	
				T_A = 105 °C	101	110	
I_{DD} max (LP Run)	Max allowed current in Low-power run mode	V_{DD} from 1.65 V to 3.6 V	-	-	-	200	

1. Guaranteed by characterization results, unless otherwise specified.

Table 26. High-speed external user clock characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{HSEH}	OSC_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time		12	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitance		-	2.6	-	pF

1. Guaranteed by design.

Figure 14. High-speed external clock source AC timing diagram

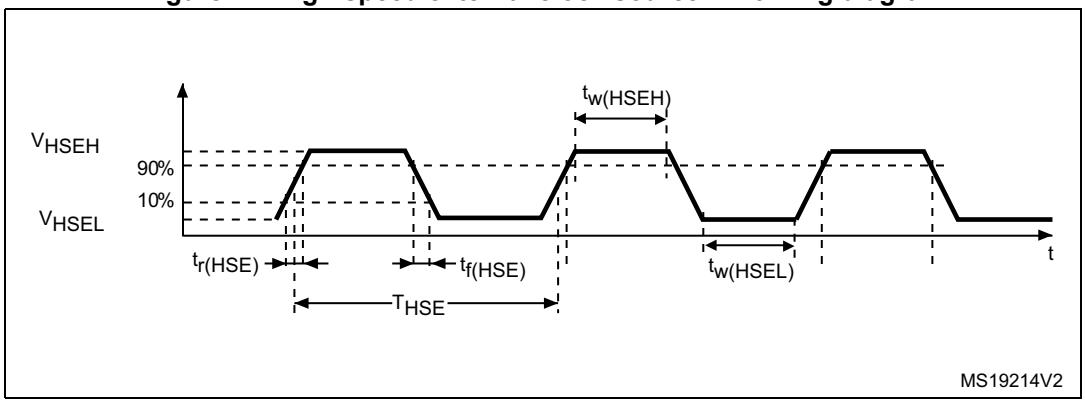


Table 28. HSE oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	1		24	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
C	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_S = 30 Ω	-	20	-	pF
I_{HSE}	HSE driving current	V_{DD}= 3.3 V, V_{IN} = V_{SS} with 30 pF load	-	-	3	mA
$I_{DD(HSE)}$	HSE oscillator power consumption	C = 20 pF f_{OSC} = 16 MHz	-	-	2.5 (startup) 0.7 (stabilized)	mA
		C = 10 pF f_{OSC} = 16 MHz	-	-	2.5 (startup) 0.46 (stabilized)	
g_m	Oscillator transconductance	Startup	3.5	-	-	mA /V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	1	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by characterization results.
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 16*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}. Refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website *www.st.com*.

6.3.7 Internal clock source characteristics

The parameters given in *Table 30* are derived from tests performed under the conditions summarized in *Table 13*.

High-speed internal (HSI) RC oscillator

Table 30. HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	V_{DD} = 3.0 V	-	16	-	MHz
$TRIM^{(1)(2)}$	HSI user-trimmed resolution	Trimming code is not a multiple of 16	-	±0.4	0.7	%
		Trimming code is a multiple of 16	-	-	±1.5	%
$ACC_{HSI}^{(2)}$	Accuracy of the factory-calibrated HSI oscillator	V_{DDA} = 3.0 V, T_A = 25 °C	$-1^{(3)}$	-	$1^{(3)}$	%
		V_{DDA} = 3.0 V, T_A = 0 to 55 °C	-1.5	-	1.5	%
		V_{DDA} = 3.0 V, T_A = -10 to 70 °C	-2	-	2	%
		V_{DDA} = 3.0 V, T_A = -10 to 85 °C	-2.5	-	2	%
		V_{DDA} = 3.0 V, T_A = -10 to 105 °C	-4	-	2	%
		V_{DDA} = 1.65 V to 3.6 V T_A = -40 to 105 °C	-4	-	3	%
$t_{SU(HSI)}^{(2)}$	HSI oscillator startup time	-	-	3.7	6	µs
$I_{DD(HSI)}^{(2)}$	HSI oscillator power consumption	-	-	100	140	µA

1. The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0).
2. Guaranteed by characterization results.
3. Guaranteed by test in production.

Low-speed internal (LSI) RC oscillator

Table 31. LSI oscillator characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$f_{LSI}^{(1)}$	LSI frequency	26	38	56	kHz
$D_{LSI}^{(2)}$	LSI oscillator frequency drift 0°C ≤T_A ≤105°C	-10	-	4	%
$t_{su(LSI)}^{(3)}$	LSI oscillator startup time	-	-	200	µs
$I_{DD(LSI)}^{(3)}$	LSI oscillator power consumption	-	400	510	nA

1. Guaranteed by test in production.
2. This is a deviation for an individual part, once the initial frequency has been measured.
3. Guaranteed by design.

Table 38. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$2*T_{HCLK}$ -3	$2*T_{HCLK}$ +2	ns
$t_{v(NWE\_NE)}$	FSMC_NEx low to FSMC_NWE low	0.5	1	ns
$t_{w(NWE)}$	FSMC_NWE low time	T_{HCLK} - 2	T_{HCLK} + 3	ns
$t_{h(NE\_NWE)}$	FSMC_NWE high to FSMC_NE high hold time	T_{HCLK} - 2.5	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	0	ns
$t_{h(A\_NWE)}$	Address hold time after FSMC_NWE high	T_{HCLK} - 2.5	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0	ns
$t_{h(BL\_NWE)}$	FSMC_BL hold time after FSMC_NWE high	T_{HCLK} - 4	-	ns
$t_{v(Data\_NE)}$	FSMC_NEx low to Data valid	-	T_{HCLK}	ns
$t_{h(Data\_NWE)}$	Data hold time after FSMC_NWE high	T_{HCLK} - 2.5	-	ns

1. C_L = 30 pF.

Figure 20. Asynchronous multiplexed PSRAM/NOR read waveforms

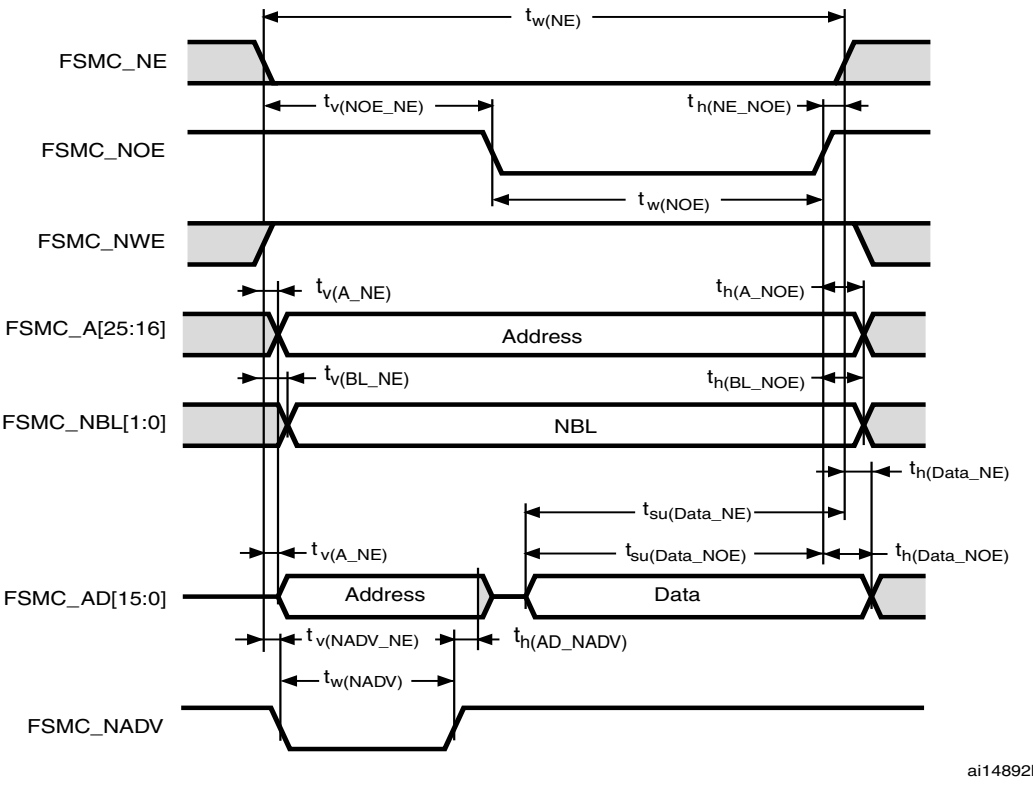


Figure 24. Synchronous non-multiplexed NOR/PSRAM read timings

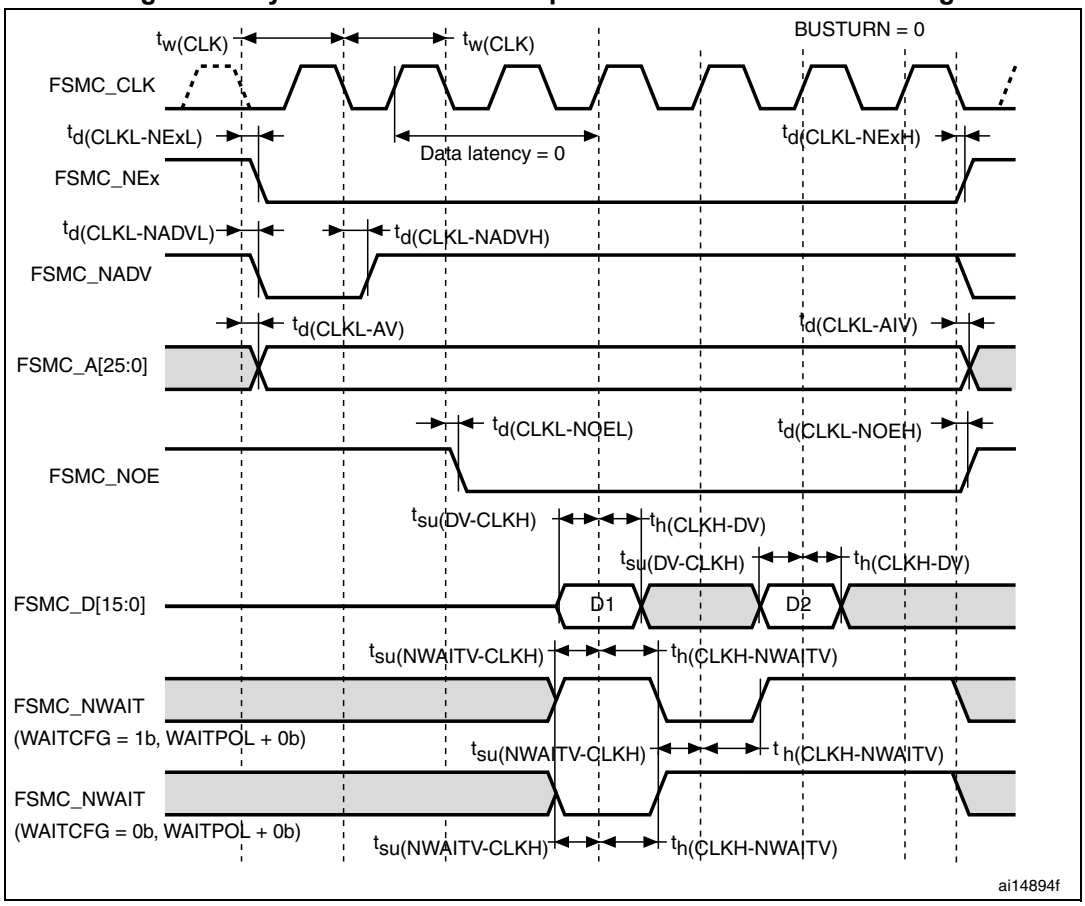
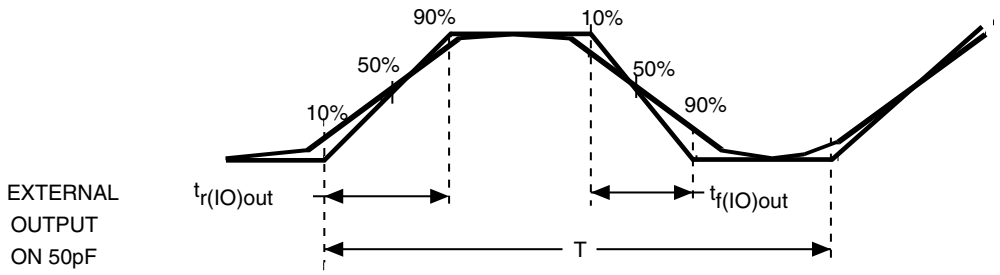


Table 43. Synchronous non-multiplexed NOR/PSRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	$2*T_{HCLK}$ - 0.5	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x = 0...2)	-	0	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x = 0...2)	0	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	3	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	3.5	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 16...25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x = 16...25)	0	-	ns
$t_{d(CLKL-NOEL)}$	FSMC_CLK low to FSMC_NOE low	-	T_{HCLK} + 1	ns
$t_{d(CLKL-NOEH)}$	FSMC_CLK low to FSMC_NOE high	2.5	-	ns
$t_{su(DV-CLKH)}$	FSMC_D[15:0] valid data before FSMC_CLK high	4	-	ns
$t_{h(CLKH-DV)}$	FSMC_D[15:0] valid data after FSMC_CLK high	4	-	ns

Figure 26. I/O AC characteristics definition



Maximum frequency is achieved if $(t_r + t_f) \leq 2/3)T$ and if the duty cycle is (45-55%)
when loaded by 50pF

ai14131c

6.3.15 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 53*)

Unless otherwise specified, the parameters given in *Table 53* are derived from tests performed under the conditions summarized in *Table 13*.

Table 53. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST input low level voltage	-	-	-	0.3 V_{DD}	V
$V_{IH(NRST)}$(1)	NRST input high level voltage	-	0.7 V_{DD}	-	-	
$V_{OL(NRST)}$(1)	NRST output low level voltage	I_{OL} = 2 mA 2.7 V < V_{DD} < 3.6 V	-	-	0.4	
		I_{OL} = 1.5 mA 1.65 V < V_{DD} < 2.7 V	-	-		
$V_{hys(NRST)}$(1)	NRST Schmitt trigger voltage hysteresis	-	-	10%V_{DD}(2)	-	mV
R_{PU}	Weak pull-up equivalent resistor(3)	V_{IN} = V_{SS}	30	45	60	kΩ
$V_{F(NRST)}$(1)	NRST input filtered pulse	-	-	-	50	ns
$V_{NF(NRST)}$(3)	NRST input not filtered pulse	-	350	-	-	ns

1. Guaranteed by design.
2. With a minimum of 200 mV.
3. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is around 10%.

Figure 29. SPI timing diagram - slave mode and CPHA = 0

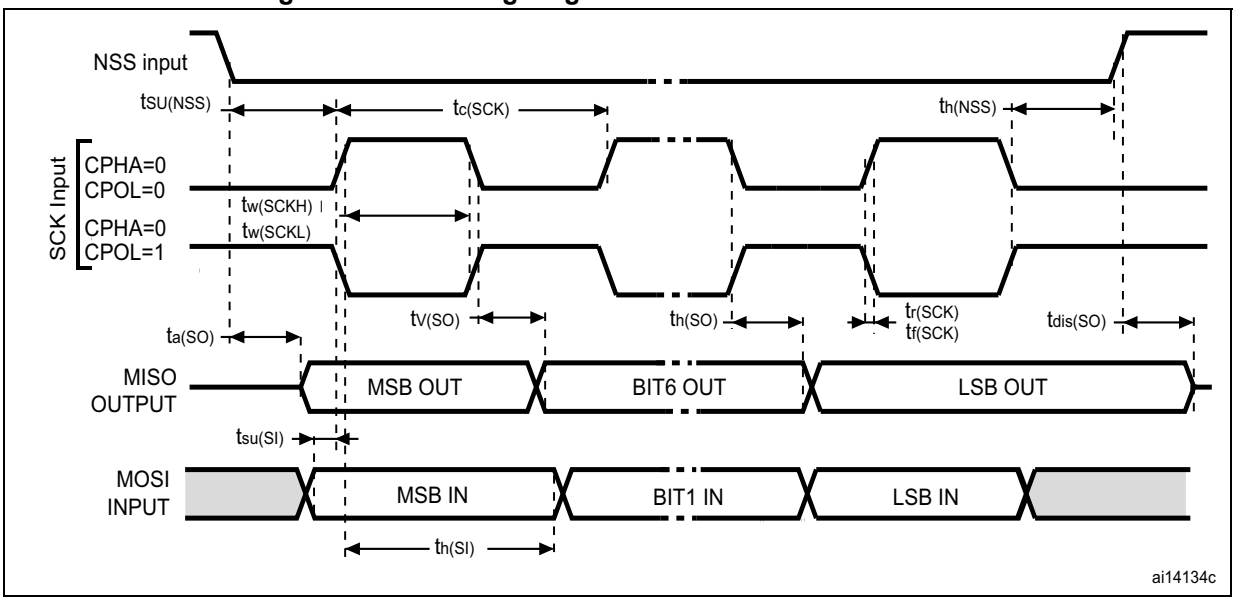
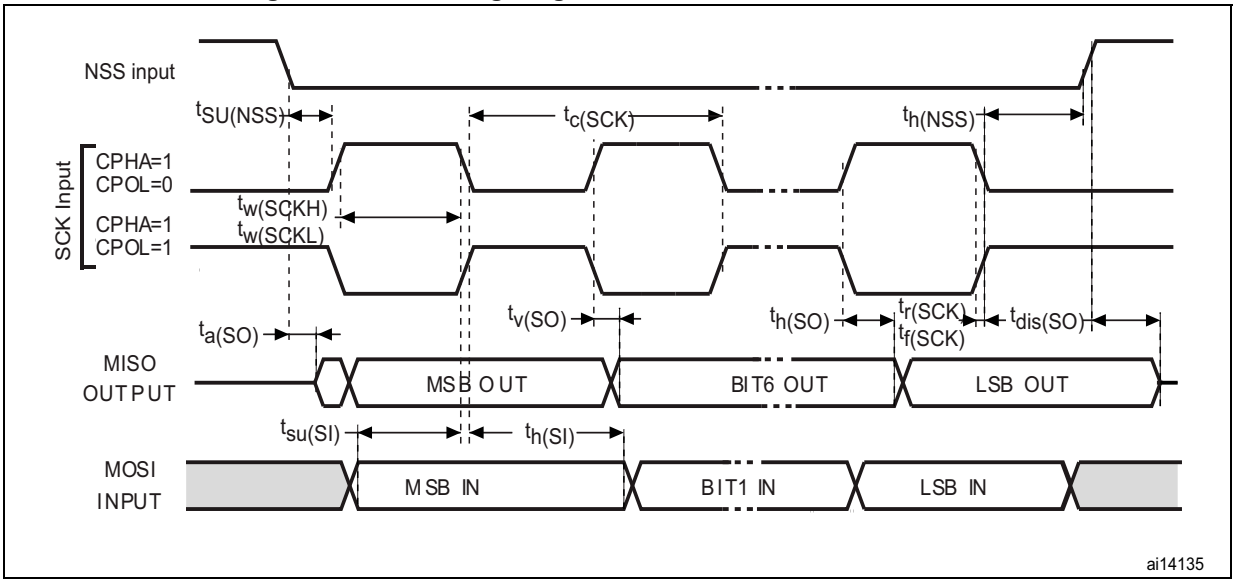


Figure 30. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

6.3.18 SDIO characteristics

Table 62. SDIO characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{PP}	Clock frequency in data transfer mode	CL ≤30 pF	0	24	MHz
$t_{W(CKL)}$	Clock low time, f_{PP} = 24 MHz	CL ≤30 pF	20(2)	-	ns
$t_{W(CKH)}$	Clock high time, f_{PP} = 24 MHz	CL ≤30 pF	18(2)	-	
t_r	Clock rise time, f_{PP} = 24 MHz	CL ≤30 pF	-	5	
t_f	Clock fall time, f_{PP} = 24 MHz	CL ≤30 pF	-	5	
CMD, D inputs (referenced to CK) in SD default mode					
-			From 2.8 to 3.6 V	-	-
t_{ISU}	Input setup time, f_{PP} = 24 MHz	CL ≤30 pF	2	-	ns
t_{IH}	Input hold time, f_{PP} = 24 MHz	CL ≤30 pF	1.6	-	
CMD, D outputs (referenced to CK) in SD default mode					
t_{OVD}	Output valid default time, f_{PP} = 24 MHz	CL ≤30 pF	0	14	ns
t_{OHD}	Output hold default time, f_{PP} = 24 MHz	CL ≤30 pF	0	-	

1. Guaranteed by characterization results.
2. Values measured with a threshold level equal to $V_{DD}/2$.

Figure 35. SDIO timings

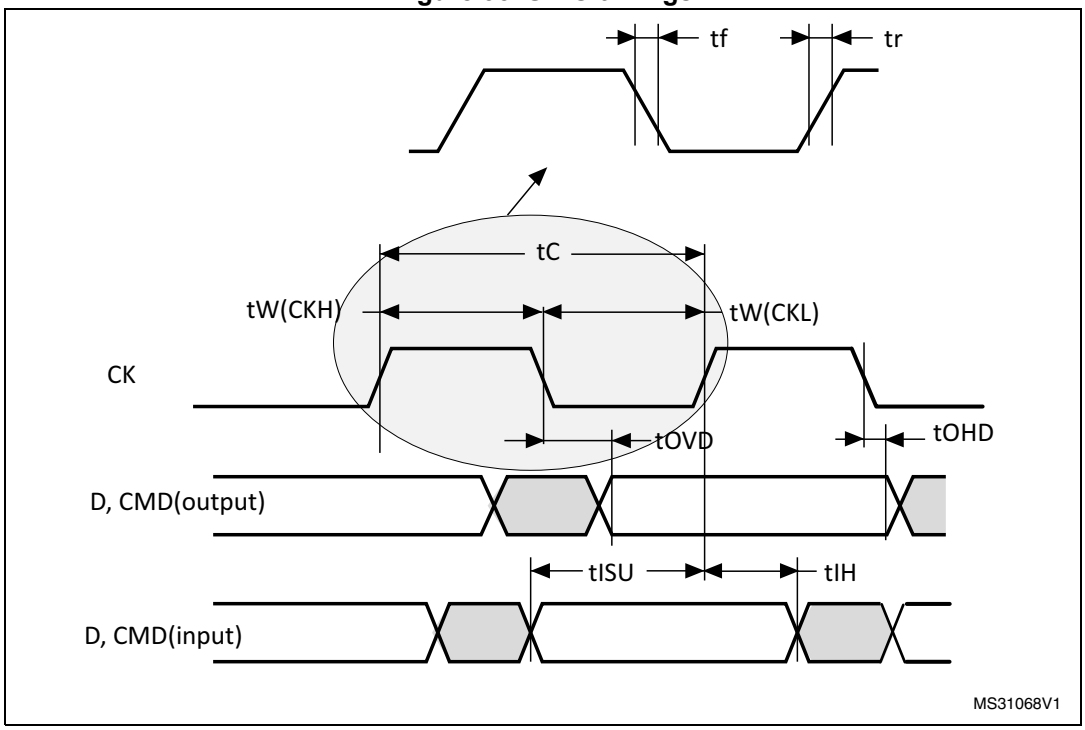


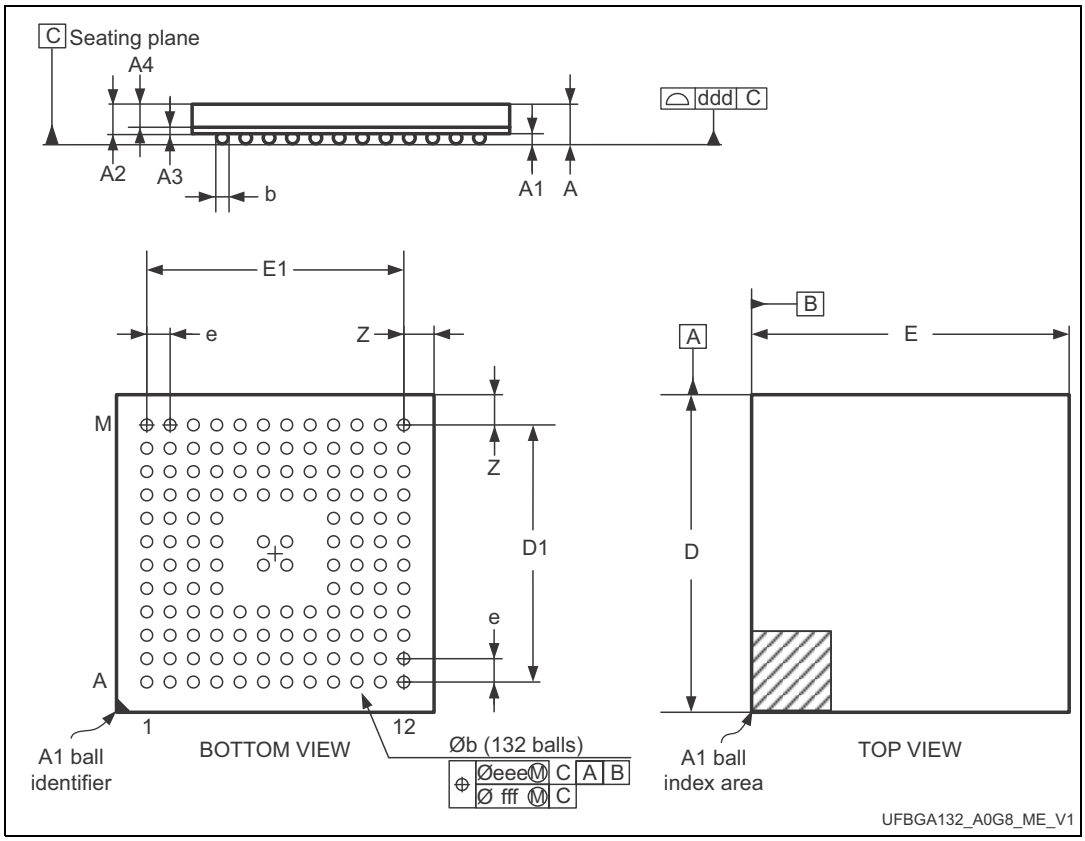
Table 65. ADC accuracy(1)(2)

Symbol	Parameter	Test conditions	Min(3)	Typ	Max(3)	Unit
ET	Total unadjusted error	2.4 V ≤V_{DDA} ≤ 3.6 V 2.4 V ≤V_{REF+} ≤ 3.6 V f_{ADC} = 8 MHz, R_{AIN} = 50 Ω T_A = -40 to 105 °C	-	2	4	LSB
EO	Offset error		-	1	2	
EG	Gain error		-	1.5	3.5	
ED	Differential linearity error		-	1	2	
EL	Integral linearity error		-	1.7	3	
ENOB	Effective number of bits	2.4 V ≤V_{DDA} ≤ 3.6 V V_{DDA} = V_{REF+} f_{ADC} = 16 MHz, R_{AIN} = 50 Ω T_A = -40 to 105 °C F_{input}=10kHz	9.2	10	-	bits
SINAD	Signal-to-noise and distortion ratio		57.5	62	-	dB
SNR	Signal-to-noise ratio		57.5	62	-	
THD	Total harmonic distortion		-	-70	-65	
ENOB	Effective number of bits	1.8 V ≤V_{DDA} ≤ 2.4 V V_{DDA} = V_{REF+} f_{ADC} = 8 MHz or 4 MHz, R_{AIN} = 50 Ω T_A = -40 to 105 °C F_{input}=10kHz	9.2	10	-	bits
SINAD	Signal-to-noise and distortion ratio		57.5	62	-	dB
SNR	Signal-to-noise ratio		57.5	62	-	
THD	Total harmonic distortion		-	-70	-65	
ET	Total unadjusted error	2.4 V ≤V_{DDA} ≤ 3.6 V 1.8 V ≤V_{REF+} ≤ 2.4 V f_{ADC} = 4 MHz, R_{AIN} = 50 Ω T_A = -40 to 105 °C	-	4	6.5	LSB
EO	Offset error		-	2	4	
EG	Gain error		-	4	6	
ED	Differential linearity error		-	1	2	
EL	Integral linearity error		-	1.5	3	
ET	Total unadjusted error	1.8 V ≤V_{DDA} ≤ 2.4 V 1.8 V ≤V_{REF+} ≤ 2.4 V f_{ADC} = 4 MHz, R_{AIN} = 50 Ω T_A = -40 to 105 °C	-	2	3	LSB
EO	Offset error		-	1	1.5	
EG	Gain error		-	1.5	2	
ED	Differential linearity error		-	1	2	
EL	Integral linearity error		-	1	1.5	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC accuracy vs. negative injection current: Injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.13* does not affect the ADC accuracy.
3. Guaranteed by characterization results.

7.4 UFBGA132, 7 x 7 mm, 132-ball ultra thin, fine-pitch ball grid array package information

Figure 49. UFBGA132, 7 x 7 mm, 132-ball ultra thin, fine-pitch ball grid array package outline



1. Drawing is not to scale.

Table 77. UFBGA132, 7 x 7 mm, 132-ball ultra thin, fine-pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	0.270	0.320	0.370	0.0106	0.0126	0.0146
b	0.170	0.280	0.330	0.0067	0.0110	0.0130
D	6.950	7.000	7.050	0.2736	0.2756	0.2776
E	6.950	7.000	7.050	0.2736	0.2756	0.2776
e	-	0.500	-	-	0.0197	-
F	0.700	0.750	0.800	0.0276	0.0295	0.0315

9 Revision History

Table 82. Document revision history

Date	Revision	Changes
03-Oct-2011	1	Initial release.
03-Feb-2012	2	Status of the document changed (datasheet instead of preliminary data). Updated low power features on page 1. Removed references to devices with 256 KB of Flash memory. GPIOF replaced with GIOPH. Added SDIO in *Table 4: Ultra-low-power STM32L15xxD device features and peripheral counts on page 12* and in *Table 19: ction input/output on page 86* (FSMC/SDIO instead of FSMC). *Table 4: Ultra-low-power STM32L15xxD device features and peripheral counts*: replaced STM32L15xWx with STM32L15xQx. *Figure 1: Ultra-low-power STM32L162xC block diagram*: updated legend. Modified *Section 3.4: Clock management on page 20*. *Table 4: STM32L15xQD STM32L162QD UFBGA132 ballout*: replaced STM32L15xWC/D with STM32L15xQD. *Figure 3*, *Figure 3*, *Figure 4*: updated titles. *Table 14: STM32L15xxD pin definitions*: updated title, updated pins PF0, PF1, PH2, PF12, PF13, PF14, PF15, PG0, PG1, PG12, PG15, PD0, and PD1. *Table 19: ction input/output*: Modified ction for PA13 and PA14; removed EVENT OUT for PH2. *Figure 5: Memory map*: removed the text “APB memory space”. Modified *Figure 8: Power supply scheme on page 46*. Modified *Table 2: Functionalities depending on the operating power supply range on page 15*. *Table 18: Current consumption in Run mode, code with data processing running from RAM*: added footnote *3*. *Table 19: Current consumption in Sleep mode*: updated condition for f_{HSE}; added footnote *3*. *Table 23: Typical and maximum current consumptions in Standby mode*: modified max values. *Table 64: USB DC electrical characteristics*: removed two footnotes. Modified *Table 38: Flash memory and data EEPROM characteristics on page 83*. *Table 73: Thermal characteristics*: updated “TBDs” with values. Modified tables in *Section 6.3.4: Supply current characteristics on page 54*.

Table 82. Document revision history (continued)

Date	Revision	Changes
07-Apr-2014	7	Updated current consumption in *Section : Features*. Updated *Section 2.2: Ultra-low-power device continuum*. Updated *Table 3: Functionalities depending on the operating power supply range*.. Added V_{DD}= 1.71 to 1.8 V operating power supply range in *Table 5: Functionalities depending on the working mode (from Run/active down to standby)*. Updated *Section 3.10: LCD (liquid crystal display)* to remove V_{LCD} rail decoupling. Updated *Section 3.16: Touch sensing*. Updated *Figure 5: Pin loading conditions*. Updated *Figure 6: Pin input voltage*. Updated *Figure 11: Power supply scheme*. Updated *Table 10: Voltage characteristics* (added row). Updated *Table 11: Current characteristics*. Updated *Table 13: General operating conditions*. Removed figures “Power supply and reference decoupling (V_{REF+} not connected to V_{DDA}) and “Power supply and reference decoupling (V_{REF+} connected to V_{DDA}). Updated *Table 15: Embedded internal reference voltage calibration values* and moved inside *Section 6.3.3: Embedded internal reference voltage*. Updated *Section 6.3.4: Supply current characteristics*. Updated *Table 17: Current consumption in Run mode, code with data processing running from Flash*, *Table 18: Current consumption in Run mode, code with data processing running from RAM*, *Table 19: Current consumption in Sleep mode*, *Table 20: Current consumption in Low-power run mode*, *Table 21: Current consumption in Low-power sleep mode*, *Table 22: Typical and maximum current consumptions in Stop mode*, and *Table 23: Typical and maximum current consumptions in Standby mode*. Added *Section 6.3.5: Wakeup time from low-power mode*. Updated *Section 6.3.6: External clock source characteristics*. Moved *Figure 14: High-speed external clock source AC timing diagram* after *Table 26: High-speed external user clock characteristics*. Updated *Figure 17: Typical application with a 32.768 kHz crystal*. Updated *Table 28: HSE oscillator characteristics*. Updated *Section 6.3.12: Electrical sensitivity characteristics* (title). Updated *Section 6.3.13: I/O current injection characteristics*. Updated *Table 49: I/O current injection susceptibility* and added footnote. Updated conditions in *Table 51: Output voltage characteristics*. Updated *Section 6.3.15: NRST pin characteristics*.Updated *Figure 27: Recommended NRST pin protection*. Updated *Table 53: NRST pin characteristics*.