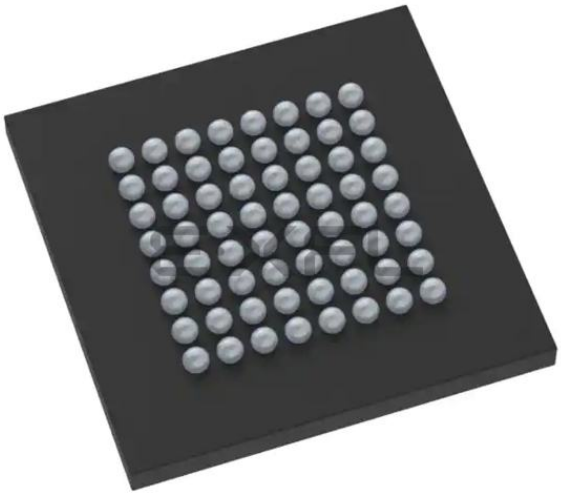

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	12K x 8
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 21x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-UFBGA, WLCSP
Supplier Device Package	64-WLCSP (4.54x4.91)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l152rdy6tr

The memory protection unit (MPU) improves system reliability by defining the memory attributes (such as read/write access permissions) for different memory regions. It provides up to eight different regions and an optional predefined background region.

Owing to its embedded ARM core, the STM32L151xD and STM32L152xD devices are compatible with all ARM tools and software.

Nested vectored interrupt controller (NVIC)

The ultra-low-power STM32L151xD and STM32L152xD devices embed a nested vectored interrupt controller able to handle up to 56 maskable interrupt channels (not including the 16 interrupt lines of ARM® Cortex®-M3) and 16 priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving*, higher-priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.3 Reset and supply management

3.3.1 Power supply schemes

- V_{DD} = 1.65 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 1.65 to 3.6 V: external analog power supplies for ADC, reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 1.8 V when the ADC is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.

3.3.2 Power supply supervisor

The device has an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR) that can be coupled with a brownout reset (BOR) circuitry.

The device exists in two versions:

- The version with BOR activated at power-on operates between 1.8 V and 3.6 V.
- The other version without BOR operates between 1.65 V and 3.6 V.

After the V_{DD} threshold is reached (1.65 V or 1.8 V depending on the BOR which is active or not at power-on), the option byte loading process starts, either to confirm or modify default thresholds, or to disable the BOR permanently: in this case, the V_{DD} min value becomes 1.65 V (whatever the version, BOR active or not, at power-on).

When BOR is active at power-on, it ensures proper operation starting from 1.8 V whatever the power ramp-up phase before it reaches 1.8 V. When BOR is not active at power-up, the

3.4 Clock management

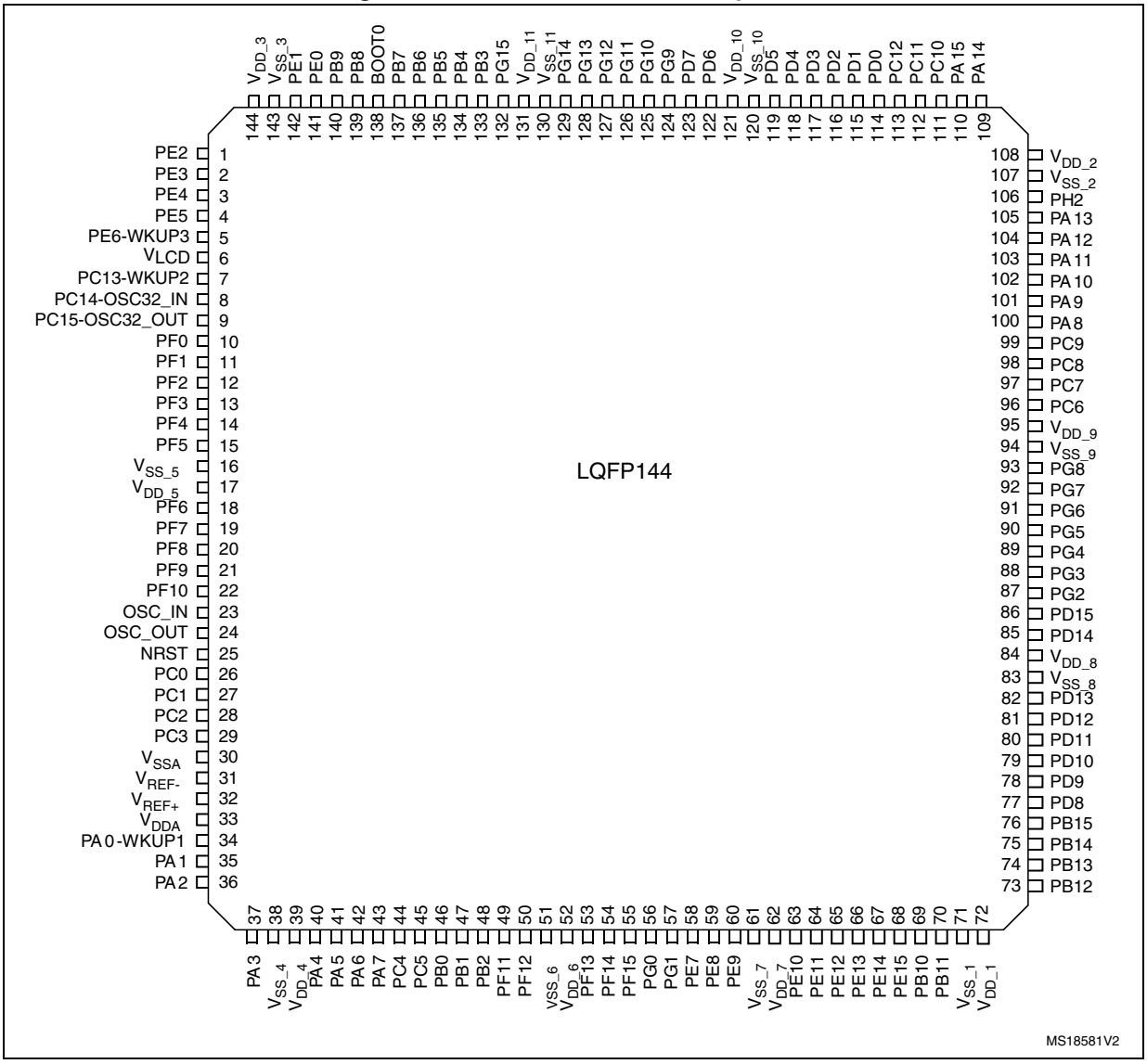
The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. It features:

- **Clock prescaler**: to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Safe clock switching**: clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management**: to reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock source**: three different clock sources can be used to drive the master clock SYSCLK:
  - 1-24 MHz high-speed external crystal (HSE), that can supply a PLL
  - 16 MHz high-speed internal RC oscillator (HSI), trimmable by software, that can supply a PLL
  - Multispeed internal RC oscillator (MSI), trimmable by software, able to generate 7 frequencies (65 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.1 MHz, 4.2 MHz). When a 32.768 kHz clock source is available in the system (LSE), the MSI frequency can be trimmed by software down to a ±0.5% accuracy.
- **Auxiliary clock source**: two ultra-low-power clock sources that can be used to drive the LCD controller and the real-time clock:
  - 32.768 kHz low-speed external crystal (LSE)
  - 37 kHz low-speed internal RC (LSI), also used to drive the independent watchdog. The LSI clock can be measured using the high-speed internal RC oscillator for greater precision.
- **RTC and LCD clock sources:** the LSI, LSE or HSE sources can be chosen to clock the RTC and the LCD, whatever the system clock.
- **USB clock source:** the embedded PLL has a dedicated 48 MHz clock output to supply the USB interface.
- **Startup clock:** after reset, the microcontroller restarts by default with an internal 2 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** this feature can be enabled by software. If a HSE clock failure occurs, the master clock is automatically switched to HSI and a software interrupt is generated if enabled.
- **Clock-out capability (MCO: microcontroller clock output):** it outputs one of the internal clocks for external use by the application.

Several prescalers allow the configuration of the AHB frequency, each APB (APB1 and APB2) domains. The maximum frequency of the AHB and the APB domains is 32 MHz. See *Figure 2* for details on the clock tree.

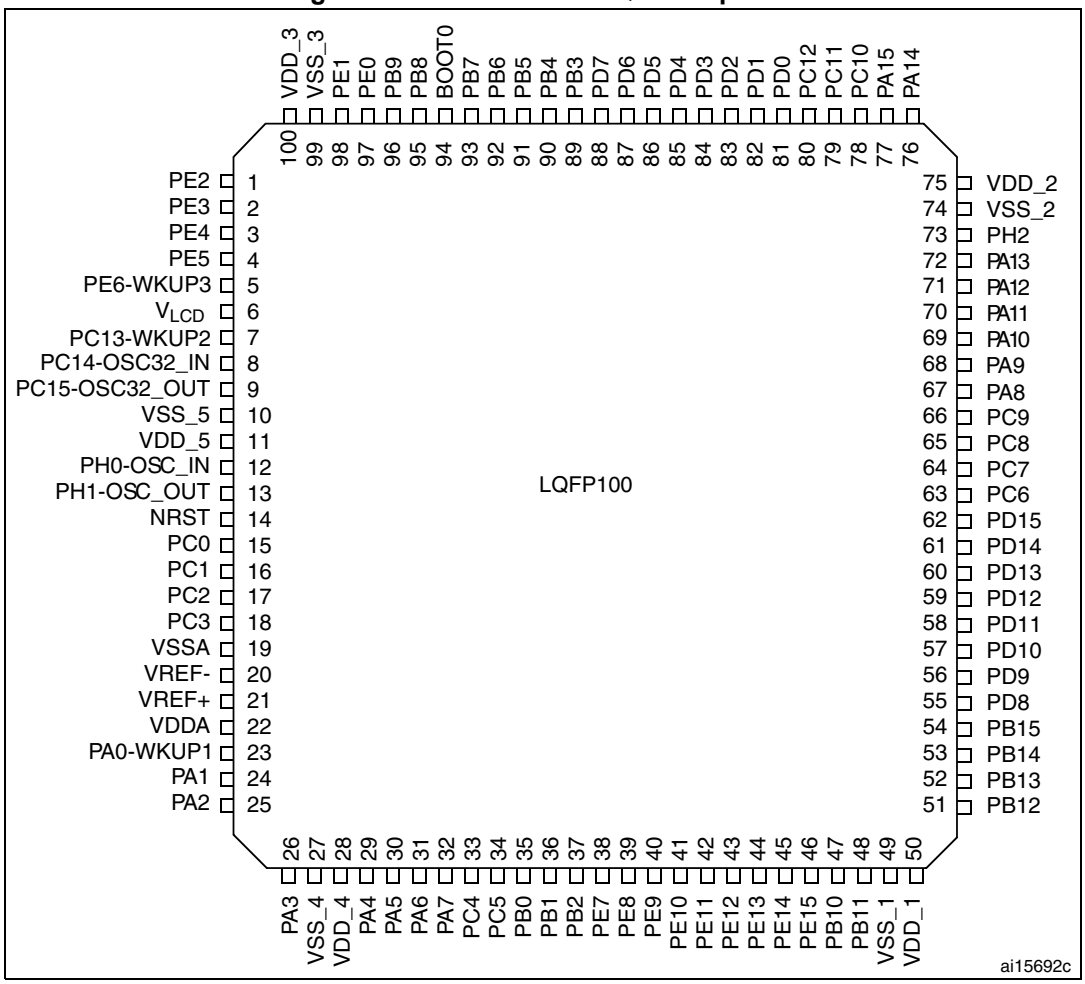
4 Pin descriptions

Figure 3. STM32L15xZD LQFP144 pinout



1. This figure shows the package top view.

Figure 5. STM32L15xVD LQFP100 pinout



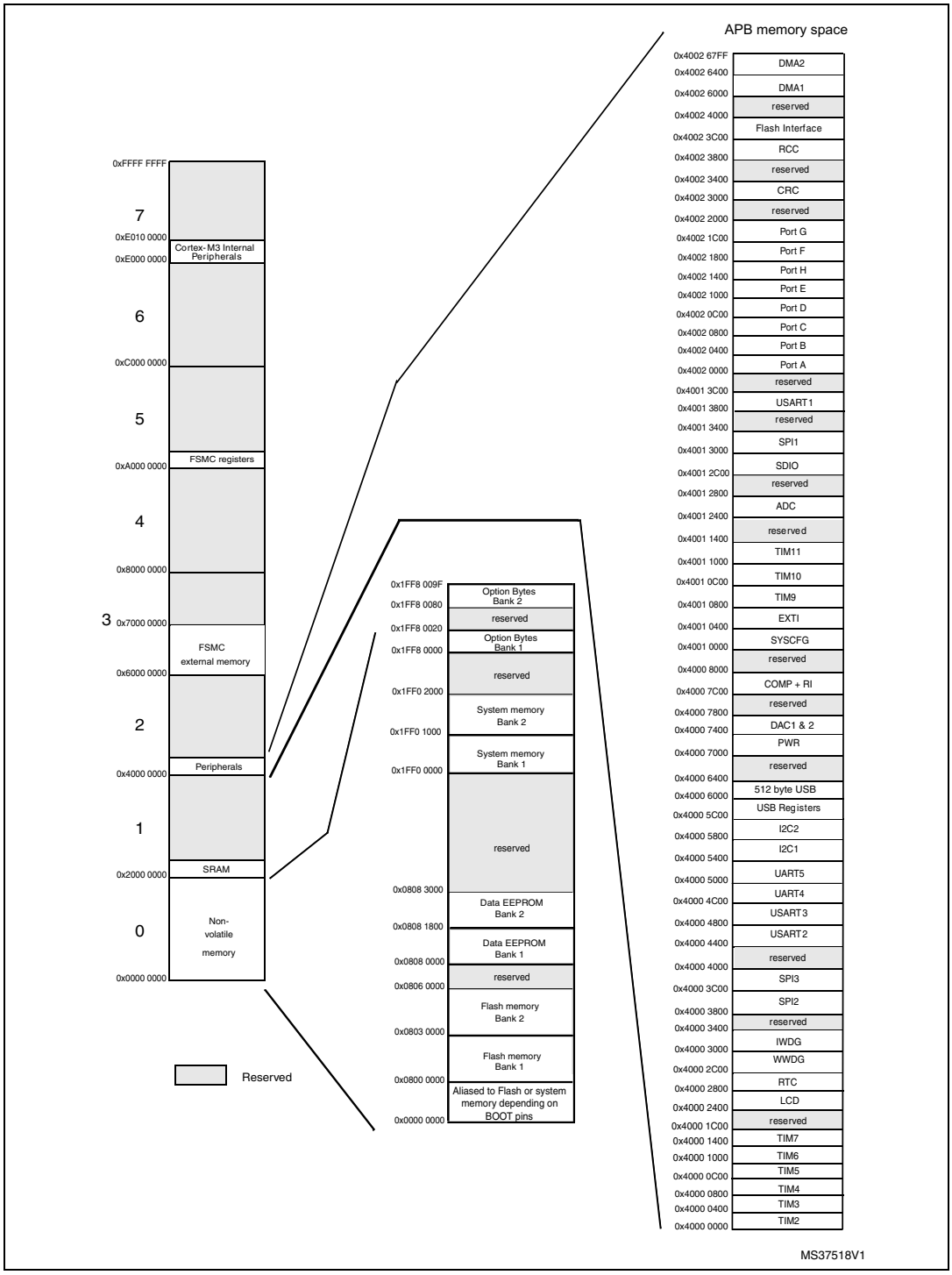
1. This figure shows the package top view.

Table 8. STM32L151xD and STM32L152xD pin definitions (continued)

Pins					Pin name	Pin Type(1)	I / O structure	Main function(2) (after reset)	Pin functions	
LQFP144	UFBGA132	LQFP100	LQFP64	WLCSP64					Alternate functions	Additional functions
115	B9	82	-	-	PD1	I/O	FT	PD1	SPI2_SCK/I2S2_CK /FSMC_D3	-
116	C8	83	54	A3	PD2	I/O	FT	PD2	TIM3_ETR/ UART5_RX/LCD_SEG31/ LCD_SEG43/LCD_COM7/ SDIO_CMD	-
117	B8	84	-	-	PD3	I/O	FT	PD3	SPI2_MISO/USART2_CTS/ FSMC_CLK	-
118	B7	85	-	-	PD4	I/O	FT	PD4	SPI2_MOSI/I2S2_SD/ USART2_RTS/ FSMC_NOE	-
119	A6	86	-	-	PD5	I/O	FT	PD5	USART2_TX/FSMC_NWE	-
120	F7	-	-	-	V_{SS_10}	S	-	V_{SS_10}	-	-
121	G7	-	-	-	V_{DD_10}	S	-	V_{DD_10}	-	-
122	B6	87	-	-	PD6	I/O	FT	PD6	USART2_RX /FSMC_NWAIT	-
123	A5	88	-	-	PD7	I/O	FT	PD7	TIM9_CH2/USART2_CK /FSMC_NE1	-
124	D9	-	-	-	PG9	I/O	FT	PG9	FSMC_NE2	-
125	D8	-	-	-	PG10	I/O	FT	PG10	FSMC_NE3	-
126	-	-	-	-	PG11	I/O	FT	PG11	-	-
127	D7	-	-	-	PG12	I/O	FT	PG12	FSMC_NE4	-
128	C7	-	-	-	PG13	I/O	FT	PG13	FSMC_A24	-
129	C6	-	-	-	PG14	I/O	FT	PG14	FSMC_A25	-
130	-	-	-	-	V_{SS_11}	S	-	V_{SS_11}	-	-
131	-	-	-	-	V_{DD_11}	S	-	V_{DD_11}	-	-
132	-	-	-	-	PG15	I/O	FT	PG15	-	-
133	A8	89	55	A4	PB3	I/O	FT	JTDO	TIM2_CH2/SPI1_SCK/ SPI3_SCK/ I2S3_CK/ LCD_SEG7/JTDO	COMP2_INM
134	A7	90	56	B4	PB4	I/O	FT	NJTRST	TIM3_CH1/SPI1_MISO/ SPI3_MISO/ LCD_SEG8/NJTRST	COMP2_INP

5 Memory mapping

Figure 8. Memory map



4. Positive current injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 10* for maximum allowed input voltage values.
5. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 10: Voltage characteristics* for the maximum allowed input voltage values.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 12. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

6.3 Operating conditions

6.3.1 General operating conditions

Table 13. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	32	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	32	
f_{PCLK2}	Internal APB2 clock frequency	-	0	32	
V_{DD}	Standard operating voltage	BOR detector disabled	1.65	3.6	V
		BOR detector enabled, at power on	1.8	3.6	
		BOR detector disabled, after power on	1.65	3.6	
V_{DDA}(1)	Analog operating voltage (ADC and DAC not used)	Must be the same voltage as V_{DD}(2)	1.65	3.6	V
	Analog operating voltage (ADC or DAC used)		1.8	3.6	
V_{IN}	I/O input voltage	FT pins; 2.0 V ≤V_{DD}	-0.3	5.5(3)	V
		FT pins; V_{DD} < 2.0 V	-0.3	5.25(3)	
		BOOT0 pin	0	5.5	
		Any other pin	-0.3	V_{DD}+0.3	
P_D	Power dissipation at TA = 85 °C for suffix 6 or TA = 105 °C for suffix 7(4)	LQFP144 package	-	500	mW
		LQFP100 package	-	465	
		LQFP64 package	-	435	
		UFBGA132	-	333	
		WLCSP64 package	-	435	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation(5)	–40	85	°C
	Ambient temperature for 7 suffix version	Maximum power dissipation	–40	105	

6.3.3 Embedded internal reference voltage

The parameters given in *Table 16* are based on characterization results, unless otherwise specified.

Table 15. Embedded internal reference voltage calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 30 °C ±5 °C V_{DDA}= 3 V ±10 mV	0x1FF8 00F8 - 0x1FF8 00F9

Table 16. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{REFINT\ out}$ (1)	Internal reference voltage	– 40 °C < T_J < +110 °C	1.202	1.224	1.242	V
I_{REFINT}	Internal reference current consumption	-	-	1.4	2.3	µA
$T_{VREFINT}$	Internal reference startup time	-	-	2	3	ms
V_{VREF_MEAS}	V_{DDA} and V_{REF+} voltage during V_{REFINT} factory measure	-	2.99	3	3.01	V
A_{VREF_MEAS}	Accuracy of factory-measured V_{REF} value(2)	Including uncertainties due to ADC and V_{DDA}/V_{REF+} values	-	-	±5	mV
T_{Coeff}(3)	Temperature coefficient	–40 °C < T_J < +110 °C	-	25	100	ppm/°C
A_{Coeff}(3)	Long-term stability	1000 hours, T= 25 °C	-	-	1000	ppm
$V_{DDCoeff}$(3)	Voltage coefficient	3.0 V < V_{DDA} < 3.6 V	-	-	2000	ppm/V
$T_{S\_vrefint}$(3)	ADC sampling time when reading the internal reference voltage	-	4	-	-	µs
T_{ADC_BUF}(3) (4)	Startup time of reference voltage buffer for ADC	-	-	-	10	µs
I_{BUF_ADC}(3)	Consumption of reference voltage buffer for ADC	-	-	13.5	25	µA
I_{VREF_OUT}(3)	VREF_OUT output current (5)	-	-	-	1	µA
C_{VREF_OUT}(3)	VREF_OUT output load	-	-	-	50	pF
I_{LPBUF}(3)	Consumption of reference voltage buffer for VREF_OUT and COMP	-	-	730	1200	nA
V_{REFINT_DIV1}(3)	1/4 reference voltage	-	24	25	26	% V_{REFINT}
V_{REFINT_DIV2}(3)	1/2 reference voltage	-	49	50	51	
V_{REFINT_DIV3}(3)	3/4 reference voltage	-	74	75	76	

1. Guaranteed by test in production.
2. The internal V_{REF} value is individually measured in production and stored in dedicated EEPROM bytes.
3. Guaranteed by characterization results.
4. Shortest sampling time can be determined in the application by multiple iterations.

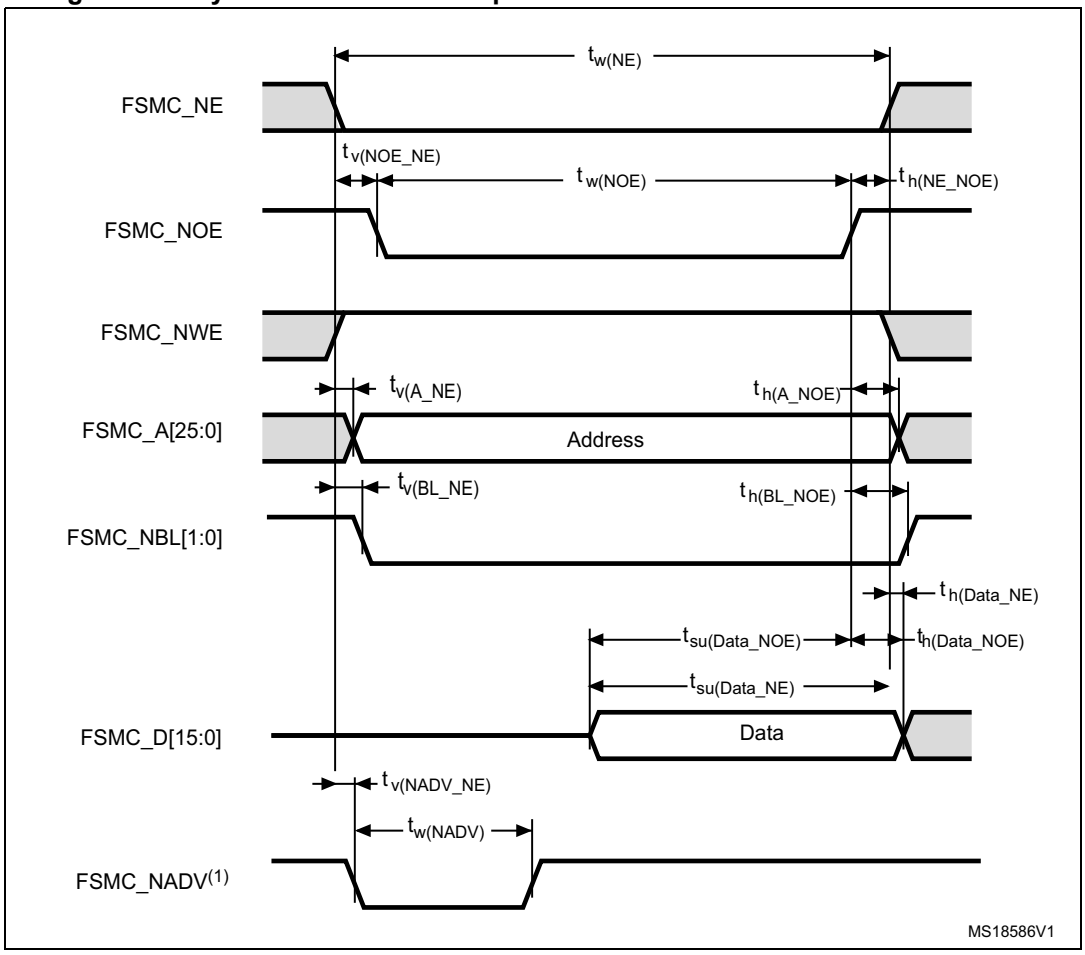
6.3.10 FSMC characteristics

Asynchronous waveforms and timings

Figure 18 through *Figure 21* represent asynchronous waveforms and *Table 37* through *Table 40* provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- AddressSetupTime = 0 (AddressSetupTime = 1, for asynchronous multiplexed modes)
- AddressHoldTime = 1
- DataSetupTime = 1

Figure 18. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms



1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

Table 38. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$2*T_{HCLK}$ -3	$2*T_{HCLK}$ +2	ns
$t_{v(NWE\_NE)}$	FSMC_NEx low to FSMC_NWE low	0.5	1	ns
$t_{w(NWE)}$	FSMC_NWE low time	T_{HCLK} - 2	T_{HCLK} + 3	ns
$t_{h(NE\_NWE)}$	FSMC_NWE high to FSMC_NE high hold time	T_{HCLK} - 2.5	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	0	ns
$t_{h(A\_NWE)}$	Address hold time after FSMC_NWE high	T_{HCLK} - 2.5	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0	ns
$t_{h(BL\_NWE)}$	FSMC_BL hold time after FSMC_NWE high	T_{HCLK} - 4	-	ns
$t_{v(Data\_NE)}$	FSMC_NEx low to Data valid	-	T_{HCLK}	ns
$t_{h(Data\_NWE)}$	Data hold time after FSMC_NWE high	T_{HCLK} - 2.5	-	ns

1. C_L = 30 pF.

Figure 20. Asynchronous multiplexed PSRAM/NOR read waveforms

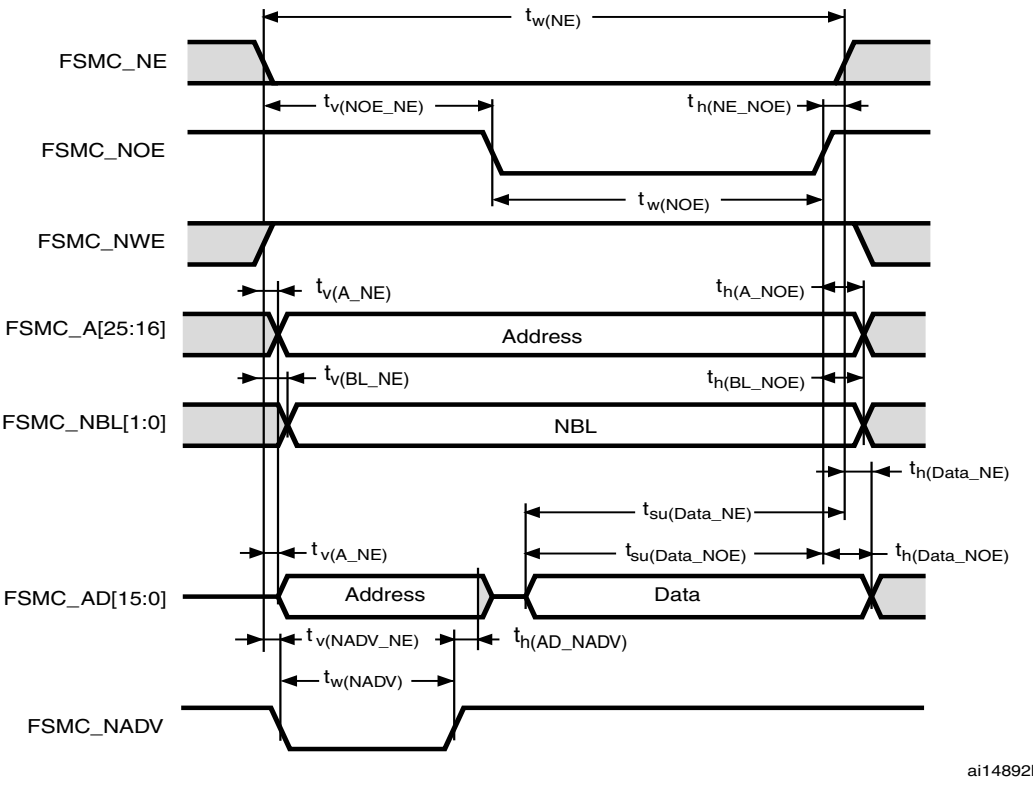


Table 40. Asynchronous multiplexed PSRAM/NOR write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$4*T_{HCLK} - 3$	$4*T_{HCLK} + 2$	ns
$t_{v(NWE\_NE)}$	FSMC_NEx low to FSMC_NWE low	T_{HCLK}	$T_{HCLK} + 1$	ns
$t_{w(NWE)}$	FSMC_NWE low time	$2*T_{HCLK} - 2$	$2*T_{HCLK} + 4$	ns
$t_{h(NE\_NWE)}$	FSMC_NWE high to FSMC_NE high hold time	$T_{HCLK} - 2.5$	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	6	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	1.5	2	ns
$t_{w(NADV)}$	FSMC_NADV low time	$T_{HCLK} - 4$	$T_{HCLK} + 4$	ns
$t_{h(AD\_NADV)}$	FSMC_AD (address) valid hold time after FSMC_NADV high	$T_{HCLK} - 5$	-	ns
$t_{h(A\_NWE)}$	Address hold time after FSMC_NWE high	$T_{HCLK} - 2.5$	-	ns
$t_{h(BL\_NWE)}$	FSMC_BL hold time after FSMC_NWE high	$T_{HCLK} - 3$	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0.5	ns
$t_{v(Data\_NADV)}$	FSMC_NADV high to Data valid	-	$T_{HCLK} + 6$	ns
$t_{h(Data\_NWE)}$	Data hold time after FSMC_NWE high	$T_{HCLK} - 2.5$	-	ns

1. C_L = 30 pF.

6.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 45*. They are based on the EMS levels and classes defined in application note AN1709.

Table 45. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, f_{HCLK} = 32 MHz conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, T_A = +25 °C, f_{HCLK} = 32 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 46. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. frequency range			Unit
				4 MHz voltage range 3	16 MHz voltage range 2	32 MHz voltage range 1	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C, LQFP100 package compliant with IEC 61967-2	0.1 to 30 MHz	3	-6	-5	dBµV
			30 to 130 MHz	18	4	-7	
			130 MHz to 1GHz	15	5	-7	
			SAE EMI Level	2.5	2	1	-

6.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 47. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to JESD22-C101	III	500	V

1. Guaranteed by characterization results.

SPI characteristics

Unless otherwise specified, the parameters given in the following table are derived from tests performed under the conditions summarized in *Table 13*.

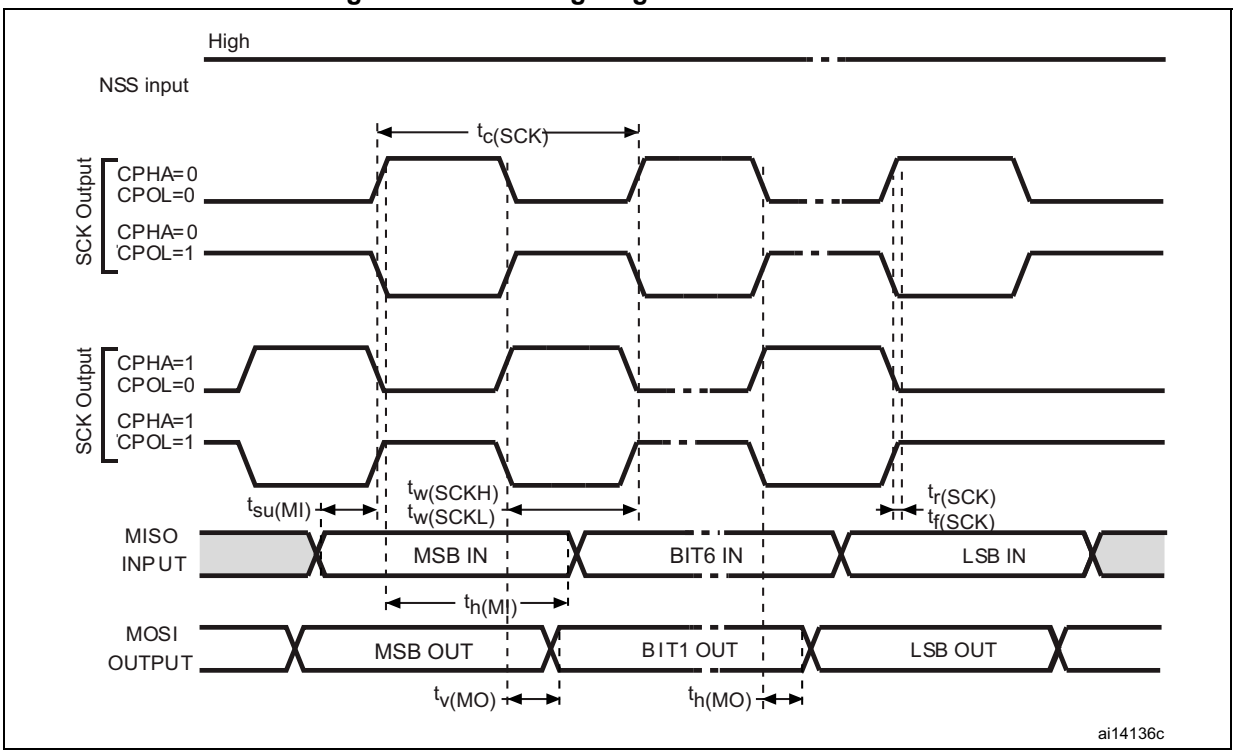
Refer to *Section 6.3.13: I/O current injection characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 57. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Max(2)	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	16	MHz
		Slave mode	-	16	
		Slave transmitter	-	12(3)	
$t_{r(SCK)}$(2) $t_{f(SCK)}$(2)	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	6	ns
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}$	NSS setup time	Slave mode	$4t_{HCLK}$	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	$2t_{HCLK}$	-	
$t_{w(SCKH)}$(2) $t_{w(SCKL)}$(2)	SCK high and low time	Master mode	$t_{SCK}/2-5$	$t_{SCK}/2+3$	
$t_{su(MI)}$(2)	Data input setup time	Master mode	5	-	
$t_{su(SI)}$(2)		Slave mode	6	-	
$t_{h(MI)}$(2)	Data input hold time	Master mode	5	-	
$t_{h(SI)}$(2)		Slave mode	5	-	
$t_{a(SO)}$(4)	Data output access time	Slave mode	0	$3t_{HCLK}$	
$t_{v(SO)}$(2)	Data output valid time	Slave mode	-	33	
$t_{v(MO)}$(2)	Data output valid time	Master mode	-	6.5	
$t_{h(SO)}$(2)	Data output hold time	Slave mode	17	-	
$t_{h(MO)}$(2)		Master mode	0.5	-	

1. The characteristics above are given for voltage range 1.
2. Guaranteed by characterization results.
3. The maximum SPI clock frequency in slave transmitter mode is given for an SPI slave input clock duty cycle (DuCy(SCK)) ranging between 40 to 60%.
4. Min time is for the minimum time to drive the output and max time is for the maximum time to validate the data.

Figure 31. SPI timing diagram - master mode(1)



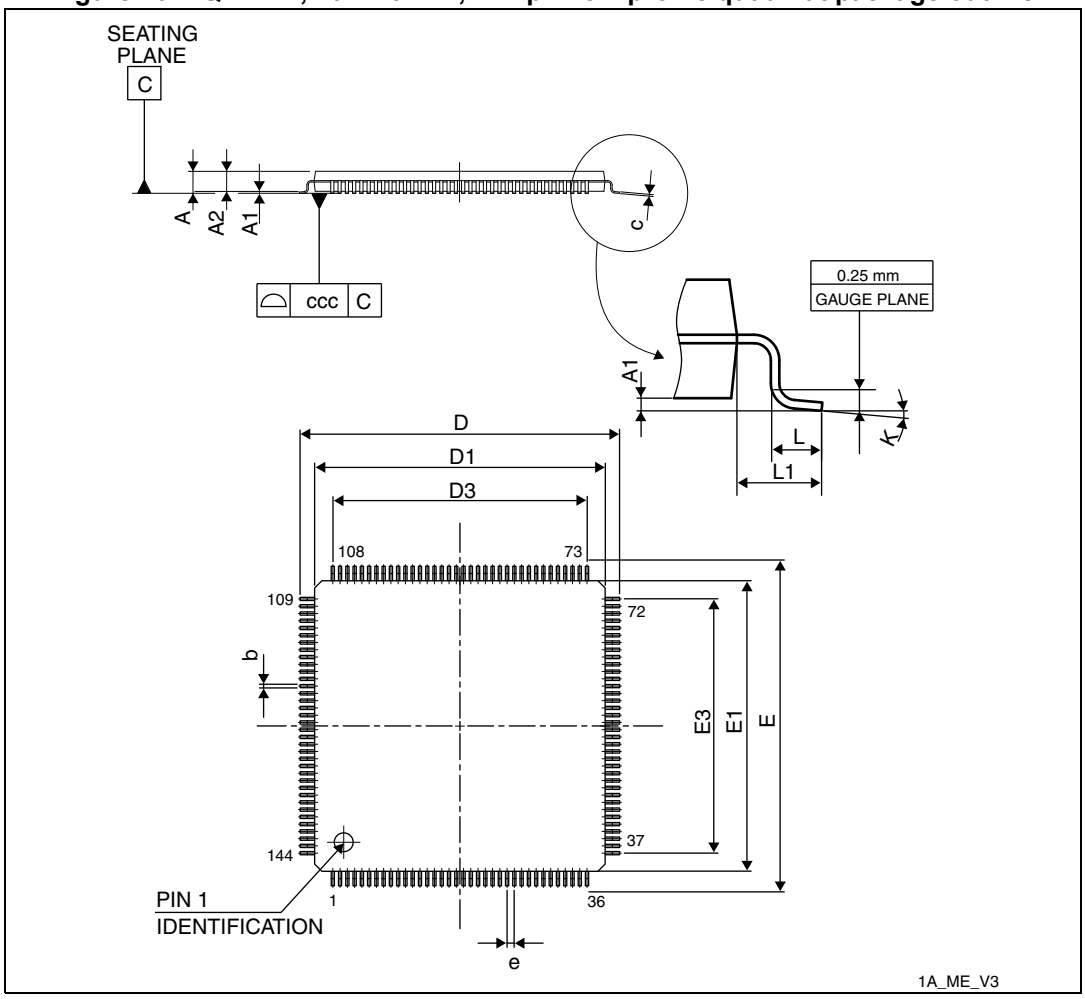
1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

7.1 LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package information

Figure 40. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package outline



1. Drawing is not to scale.

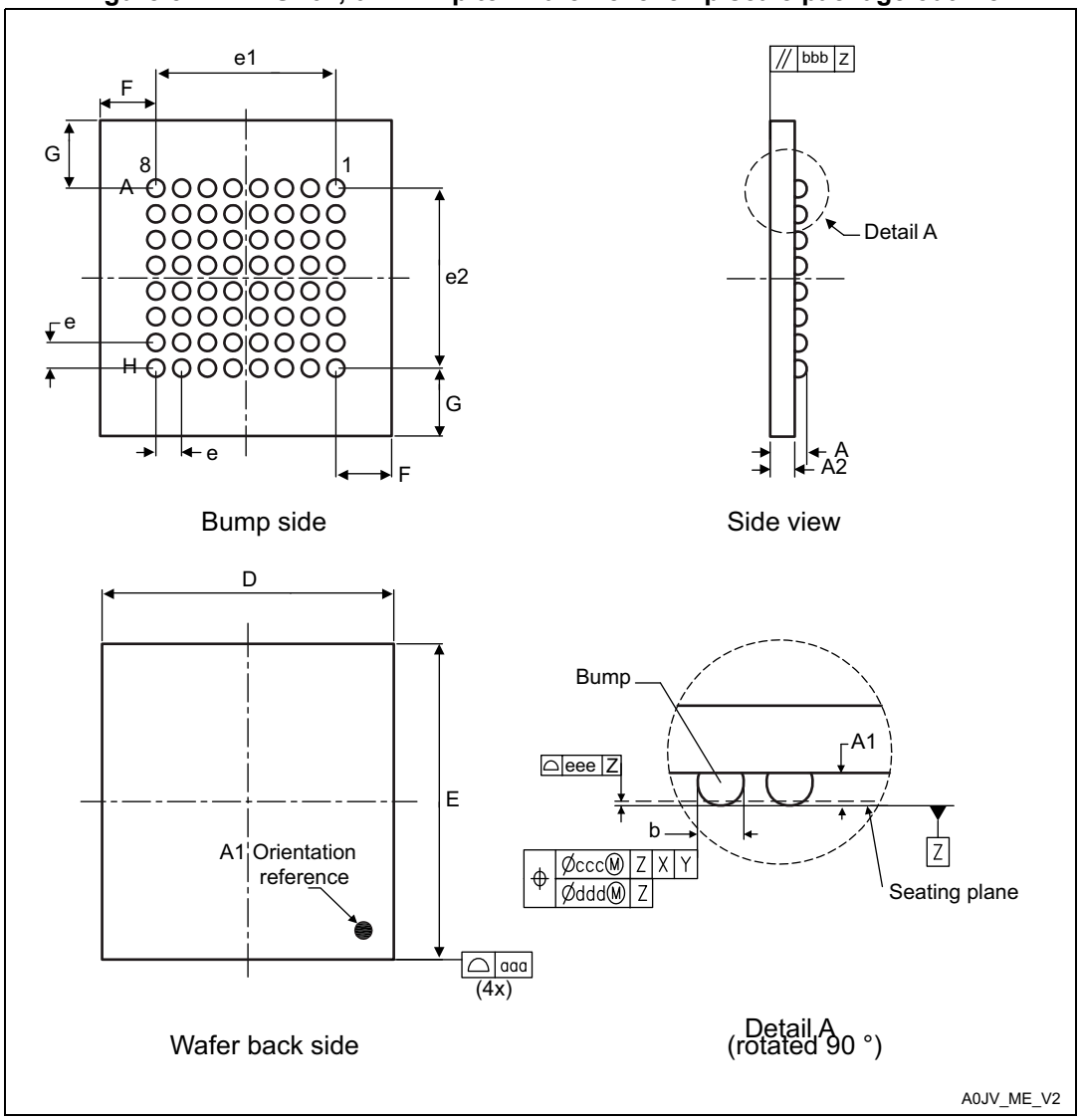
Table 74. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.8740
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	-	17.500	-	-	0.6890	-
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-	-	0.6890	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

7.5 WLCSP64, 0.4 mm pitch wafer level chip scale package information

Figure 52. WLCSP64, 0.4 mm pitch wafer level chip scale package outline



1. Drawing is not to scale.

Table 78. WLCSP64, 0.4 mm pitch wafer level chip scale package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.540	0.570	0.600	0.0205	0.0224	0.0236
A1	-	0.190	-	-	0.0075	-
A2	-	0.380	-	-	0.0150	-

9 Revision History

Table 82. Document revision history

Date	Revision	Changes
03-Oct-2011	1	Initial release.
03-Feb-2012	2	Status of the document changed (datasheet instead of preliminary data). Updated low power features on page 1. Removed references to devices with 256 KB of Flash memory. GPIOF replaced with GIOPH. Added SDIO in *Table 4: Ultra-low-power STM32L15xxD device features and peripheral counts on page 12* and in *Table 19: ction input/output on page 86* (FSMC/SDIO instead of FSMC). *Table 4: Ultra-low-power STM32L15xxD device features and peripheral counts*: replaced STM32L15xWx with STM32L15xQx. *Figure 1: Ultra-low-power STM32L162xC block diagram*: updated legend. Modified *Section 3.4: Clock management on page 20*. *Table 4: STM32L15xQD STM32L162QD UFBGA132 ballout*: replaced STM32L15xWC/D with STM32L15xQD. *Figure 3*, *Figure 3*, *Figure 4*: updated titles. *Table 14: STM32L15xxD pin definitions*: updated title, updated pins PF0, PF1, PH2, PF12, PF13, PF14, PF15, PG0, PG1, PG12, PG15, PD0, and PD1. *Table 19: ction input/output*: Modified ction for PA13 and PA14; removed EVENT OUT for PH2. *Figure 5: Memory map*: removed the text “APB memory space”. Modified *Figure 8: Power supply scheme on page 46*. Modified *Table 2: Functionalities depending on the operating power supply range on page 15*. *Table 18: Current consumption in Run mode, code with data processing running from RAM*: added footnote *3*. *Table 19: Current consumption in Sleep mode*: updated condition for f_{HSE}; added footnote *3*. *Table 23: Typical and maximum current consumptions in Standby mode*: modified max values. *Table 64: USB DC electrical characteristics*: removed two footnotes. Modified *Table 38: Flash memory and data EEPROM characteristics on page 83*. *Table 73: Thermal characteristics*: updated “TBDs” with values. Modified tables in *Section 6.3.4: Supply current characteristics on page 54*.

Table 82. Document revision history (continued)

Date	Revision	Changes
18-Apr-2012	3	Added WLCSP64 package. *Section 3: Functional overview*: changed '128 kHz' to '131 kHz' in section "Low power run mode". *Section 3.17.1: General-purpose timers (TIM2, TIM3, TIM4, TIM5, TIM9, TIM10 and TIM11)*: changed 'six' to 'seven' synchronizable general-purpose timers. *Table 14: STM32L15xxD pin definitions on page 52*: updated name of reference manual in footnote *5.* I2C updated: footnote *3.* from *Table 58* Note about I2C clock updated: footnote *2.* from *Table 58* modified. Note [non-robust] updated: footnote *2.* from *Table 68* modified. GPIOs high current capability updated: *Section 3.6: GPIOs (general-purpose inputs/outputs)* 'except for analog inputs' was removed.
15-Jun-2012	4	Changed maximum number of touch sensing channels to 34, and updated *Table 4: Ultra-low-power STM32L15xxD device features and peripheral counts*. Updated *Section 3.10: ADC (analog-to-digital converter)* to add *Section 3.10.1: Temperature sensor* and *Section 3.10.2: Internal voltage reference (VREFINT)*. Removed caution note below *Figure 8: Power supply scheme*. Added note below *Table 4: STM32L15xQD STM32L162QD UFBGA132 ballout*. Modified *Table 8: STM32L15xRDSTM32L162RD WLCSP64 ballout* to match top view. Changed FSMC_LBAR into FSMC_NADV, and I2C1_SMBAI into I2C1_SMBA in *Table 14: STM32L15xxD pin definitions*. Modified PB10/11/12 for AFIO4 ction, and replaced LBAR by NADV for AFIO12 in *Table 19: ction input/output*. Updated *Table 22: Typical and maximum current consumptions in Stop mode* and added *Note 6*. Updated *Table 23: Typical and maximum current consumptions in Standby mode*. Updated t_{WUSTOP} in *Table :* . Updated *Table 27: Peripheral current consumption*. Updated *Table 60: SPI characteristics*, added *Note 1* and *Note 3*, and applied *Note 2* to $t_{r(SCK)}$, $t_{f(SCK)}$, $t_{w(SCKH)}$, $t_{w(SCKL)}$, $t_{su(MI)}$, $t_{su(SI)}$, $t_{h(MI)}$, and $t_{h(SI)}$. Updated I_{DD} maximum value in *Table 38: Flash memory and data EEPROM characteristics*.