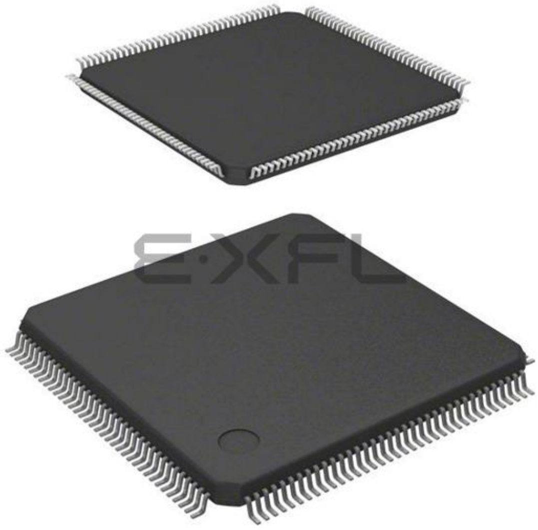

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, Cap Sense, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	115
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	12K x 8
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 40x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l152zdt6

Table 5. Functionalities depending on the working mode (from Run/active down to standby)

Ips	Run/Active	Sleep	Low-power Run	Low-power Sleep	Stop		Standby	
						Wakeup capability		Wakeup capability
CPU	Y	--	Y	--	--	--	--	--
Flash	Y	Y	Y	Y	--	--	--	--
RAM	Y	Y	Y	Y	Y	--	--	--
Backup Registers	Y	Y	Y	Y	Y	--	Y	--
EEPROM	Y	Y	Y	Y	Y	--	--	--
Brown-out rest (BOR)	Y	Y	Y	Y	Y	Y	Y	--
DMA	Y	Y	Y	Y	--	--	--	--
Programmable Voltage Detector (PVD)	Y	Y	Y	Y	Y	Y	Y	--
Power On Reset (POR)	Y	Y	Y	Y	Y	Y	Y	--
Power Down Rest (PDR)	Y	Y	Y	Y	Y	--	Y	--
High Speed Internal (HSI)	Y	Y	--	--	--	--	--	--
High Speed External (HSE)	Y	Y	--	--	--	--	--	--
Low Speed Internal (LSI)	Y	Y	Y	Y	Y	--	Y	--
Low Speed External (LSE)	Y	Y	Y	Y	Y	--	Y	--
Multi-Speed Internal (MSI)	Y	Y	Y	Y	--	--	--	--
Inter-Connect Controller	Y	Y	Y	Y	--	--	--	--
RTC	Y	Y	Y	Y	Y	Y	Y	--
RTC Tamper	Y	Y	Y	Y	Y	Y	Y	Y
Auto WakeUp (AWU)	Y	Y	Y	Y	Y	Y	Y	Y
LCD	Y	Y	Y	Y	Y	--	--	--
USB	Y	Y	--	--	--	Y	--	--
USART	Y	Y	Y	Y	Y	(1)	--	--
SPI	Y	Y	Y	Y	--	--	--	--
I2C	Y	Y	Y	Y	--	(1)	--	--

3.5 Low-power real-time clock and backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Dedicated registers contain the sub-second, second, minute, hour (12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day of the month are made automatically. The RTC provides two programmable alarms and programmable periodic interrupts with wakeup from Stop and Standby modes.

The programmable wakeup time ranges from 120 µs to 36 hours.

The RTC can be calibrated with an external 512 Hz output, and a digital compensation circuit helps reduce drift due to crystal deviation.

The RTC can also be automatically corrected with a 50/60Hz stable powerline.

The RTC calendar can be updated on the fly down to sub second precision, which enables network system synchronization.

A time stamp can record an external event occurrence, and generates an interrupt.

There are thirty-two 32-bit backup registers provided to store 128 bytes of user application data. They are cleared in case of tamper detection.

Three pins can be used to detect tamper events. A change on one of these pins can reset backup register and generate an interrupt. To prevent false tamper event, like ESD event, these three tamper inputs can be digitally filtered.

3.6 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions, and can be individually remapped using dedicated AFIO registers. All GPIOs are high current capable. The alternate function configuration of I/Os can be locked if needed following a specific sequence in order to avoid spurious writing to the I/O registers. The I/O controller is connected to the AHB with a toggling speed of up to 16 MHz.

External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 24 edge detector lines used to generate interrupt/event requests. Each line can be individually configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 115 GPIOs can be connected to the 16 external interrupt lines. The 8 other lines are connected to RTC, PVD, USB, comparator events or capacitive sensing acquisition.

TIM10, TIM11 and TIM9

TIM10 and TIM11 are based on a 16-bit auto-reload upcounter. TIM9 is based on a 16-bit auto-reload up/down counter. They include a 16-bit prescaler. TIM10 and TIM11 feature one independent channel, whereas TIM9 has two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers.

They can also be used as simple time bases and be clocked by the LSE clock source (32.768 kHz) to provide time bases independent from the main CPU clock.

3.17.2 Basic timers (TIM6 and TIM7)

These timers are mainly used for DAC trigger generation. They can also be used as generic 16-bit time bases.

3.17.3 SysTick timer

This timer is dedicated to the OS, but could also be used as a standard downcounter. It is based on a 24-bit downcounter with autoreload capability and a programmable clock source. It features a maskable system interrupt generation when the counter reaches 0.

3.17.4 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 37 kHz internal RC and, as it operates independently of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.

3.17.5 Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.18 Communication interfaces

3.18.1 I²C bus

Up to two I²C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes.

They support dual slave addressing (7-bit only) and both 7- and 10-bit addressing in master mode. A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SM Bus 2.0/PM Bus.

Table 8. STM32L151xD and STM32L152xD pin definitions (continued)

Pins					Pin name	Pin Type[(1)]	I / O structure	Main function[(2)] (after reset)	Pin functions	
LQFP144	UFBGA132	LQFP100	LQFP64	WLCSP64					Alternate functions	Additional functions
14	F3	-	-	-	PF4	I/O	FT	PF4	FSMC_A4	-
15	F4	-	-	-	PF5	I/O	FT	PF5	FSMC_A5	-
16	F2	10	-	-	V_{SS_5}	S	-	V_{SS_5}	-	-
17	G2	11	-	-	V_{DD_5}	S	-	V_{DD_5}	-	-
18	G3	-	-	-	PF6	I/O	FT	PF6	TIM5_CH1/TIM5_ETR	ADC_IN27
19	G4	-	-	-	PF7	I/O	FT	PF7	TIM5_CH2	ADC_IN28/ COMP1_INP
20	H4	-	-	-	PF8	I/O	FT	PF8	TIM5_CH3	ADC_IN29/ COMP1_INP
21	J6	-	-	-	PF9	I/O	FT	PF9	TIM5_CH4	ADC_IN30/ COMP1_INP
22	-	-	-	-	PF10	I/O	FT	PF10	-	ADC_IN31/ COMP1_INP
23	F1	12	5	D8	PH0-OSC_IN[(5)]	I/O	TC	PH0	-	OSC_IN
24	G1	13	6	D7	PH1-OSC_OUT[(5)]	I/O	TC	PH1	-	OSC_OUT
25	H2	14	7	C7	NRST	I/O	RST	NRST	-	-
26	H1	15	8	E8	PC0	I/O	FT	PC0	LCD_SEG18	ADC_IN10/ COMP1_INP
27	J2	16	9	F8	PC1	I/O	FT	PC1	LCD_SEG19	ADC_IN11/ COMP1_INP OPAMP3_VINP
28	-	17	10	D6	PC2	I/O	FT	PC2	LCD_SEG20	ADC_IN12/ COMP1_INP OPAMP3_VINM
-	J3	-	-	-	PC2	I/O	FT	PC2	LCD_SEG20	ADC_IN12/ COMP1_INP
-	K1	-	-	-	OPAMP3_VINM	I	-	OPAMP3_VINM	-	-
29	K2	18	11	F7	PC3	I/O	TC	PC3	LCD_SEG21	ADC_IN13/ COMP1_INP/ OPAMP3_VOUT
30	J1	19	12	E7	V_{SSA}	S	-	V_{SSA}	-	-

Table 8. STM32L151xD and STM32L152xD pin definitions (continued)

Pins					Pin name	Pin Type(1)	I / O structure	Main function(2) (after reset)	Pin functions	
LQFP144	UFBGA132	LQFP100	LQFP64	WLCSP64					Alternate functions	Additional functions
31	-	20	-	-	V_{REF-}	S	-	V_{REF-}	-	-
32	L1	21	-	-	V_{REF+}	S	-	V_{REF+}	-	-
33	M1	22	13	G8	V_{DDA}	S	-	V_{DDA}	-	-
34	L2	23	14	F6	PA0-WKUP1	I/O	FT	PA0	TIM2_CH1_ETR/ TIM5_CH1/ USART2_CTS	WKUP1/ RTC_TAMP2/ ADC_IN0/ COMP1_INP
35	M2	24	15	E6	PA1	I/O	FT	PA1	TIM2_CH2/TIM5_CH2/ USART2_RTS/ LCD_SEG0	ADC_IN1/ COMP1_INP/ OPAMP1_VINP
36	-	25	16	H8	PA2	I/O	FT	PA2	TIM2_CH3/TIM5_CH3/ TIM9_CH1/ USART2_TX/LCD_SEG1	ADC_IN2/ COMP1_INP/ OPAMP1_VINM
-	K3	-	-	-	PA2	I/O	FT	PA2	TIM2_CH3/TIM5_CH3/ TIM9_CH1/ USART2_TX/LCD_SEG1	ADC_IN2/ COMP1_INP
-	M3	-	-	-	OPAMP1_VINM	I	TC	OPAMP1_VINM	-	-
37	L3	26	17	G7	PA3	I/O	TC	PA3	TIM2_CH4/TIM5_CH4/ TIM9_CH2/ USART2_RX/LCD_SEG2	ADC_IN3/ COMP1_INP/ OPAMP1_VOUT
38	-	27	18	F5	V_{SS_4}	S	-	V_{SS_4}	-	-
39	-	28	19	G6	V_{DD_4}	S	-	V_{DD_4}	-	-
40	J4	29	20	H7	PA4	I/O	TC	PA4	SPI1_NSS/SPI3_NSS/ I2S3_WS/USART2_CK	ADC_IN4/ DAC_OUT1/ COMP1_INP
41	K4	30	21	E5	PA5	I/O	TC	PA5	TIM2_CH1_ETR/ SPI1_SCK	ADC_IN5/ DAC_OUT2/ COMP1_INP
42	L4	31	22	G5	PA6	I/O	FT	PA6	TIM3_CH1/TIM10_CH1/ SPI1_MISO/ LCD_SEG3	ADC_IN6/ COMP1_INP/ OPAMP2_VINP
43	-	32	23	G4	PA7	I/O	FT	PA7	TIM3_CH2/TIM11_CH1/ SPI1_MOSI/ LCD_SEG4	ADC_IN7/ COMP1_INP/ OPAMP2_VINM

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.6 V (for the 1.65 V ≤V_{DD} ≤3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 9*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 10*.

Figure 9. Pin loading conditions

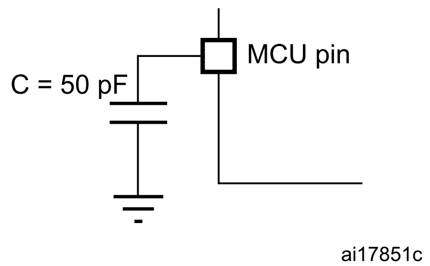


Figure 10. Pin input voltage

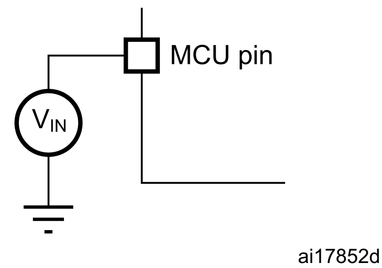


Table 24. Peripheral current consumption[(1)] (continued)

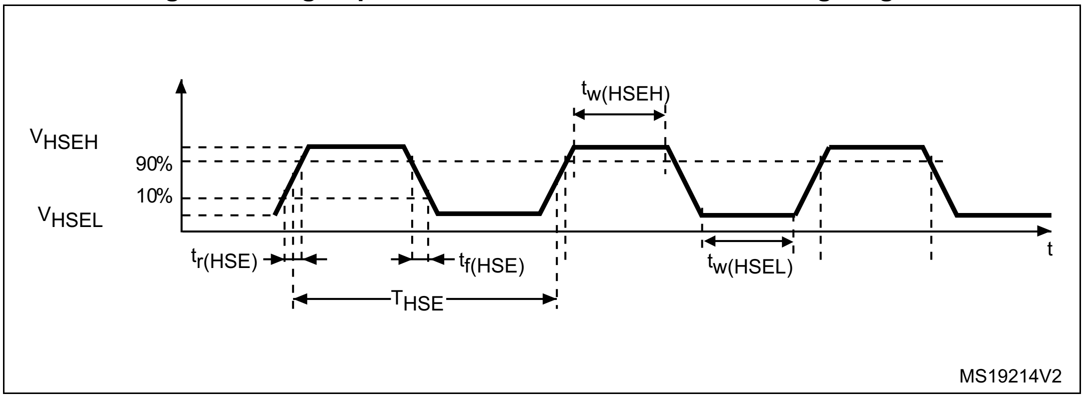
Peripheral		Typical consumption, V_{DD} = 3.0 V, T_A = 25 °C				Unit
		Range 1, V_{CORE}= 1.8 V VOS[1:0] = 01	Range 2, V_{CORE}= 1.5 V VOS[1:0] = 10	Range 3, V_{CORE}= 1.2 V VOS[1:0] = 11	Low-power sleep and run	
APB2	SYSCFG & RI	3.5	2.9	2.4	2.9	µA/MHz (f_{HCLK})
	TIM9	9.0	7.4	5.8	7.4	
	TIM10	7.1	5.8	4.6	5.8	
	TIM11	6.5	5.3	4.3	5.3	
	ADC[(2)]	11.0	9.1	7.2	9.1	
	SDIO	28.4	24.2	19.1	24.2	
	SPI1	5.1	4.2	3.3	4.2	
	USART1	9.4	7.8	6.1	7.8	
AHB	GPIOA	7.3	6.1	4.8	6.1	
	GPIOB	7.5	6.1	4.8	6.1	
	GPIOC	8.2	6.8	5.3	6.8	
	GPIOD	8.7	7.1	5.7	7.1	
	GPIOE	7.6	6.2	4.9	6.2	
	GPIOF	7.7	6.3	5.0	6.3	
	GPIOG	8.4	7.0	5.4	7.0	
	GPIOH	1.8	1.3	1.1	1.3	
	CRC	0.8	0.6	0.4	0.6	
	FLASH	26.3	19.3	18.3	-[(3)]	
	DMA1	19.0	16.0	12.8	16.0	
	DMA2	17.0	14.5	11.5	14.5	
	FSMC	16.0	13.4	10.6	13.4	
All enabled		310	246	217	226.7	

Table 26. High-speed external user clock characteristics[1] (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{HSEH}	OSC_IN input pin high level voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time		12	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitance		-	2.6	-	pF

1. Guaranteed by design.

Figure 14. High-speed external clock source AC timing diagram



4. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Note: *For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator (see Figure 17). C_{L1} and $C_{L2,}$ are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}.*
Load capacitance C_L has the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Caution: To avoid exceeding the maximum value of C_{L1} and C_{L2} (15 pF) it is strongly recommended to use a resonator with a load capacitance $C_L \leq 7$ pF. Never use a resonator with a load capacitance of 12.5 pF.
Example: if the user chooses a resonator with a load capacitance of C_L = 6 pF and C_{stray} = 2 pF, then $C_{L1} = C_{L2}$ = 8 pF.

Figure 17. Typical application with a 32.768 kHz crystal

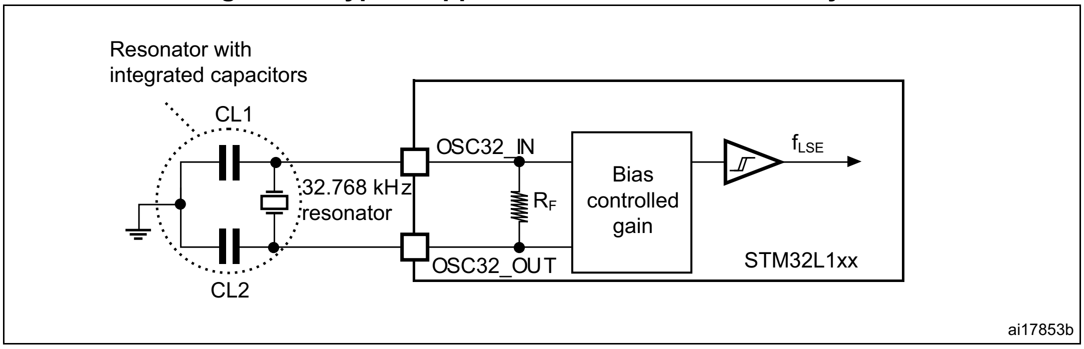


Table 43. Synchronous non-multiplexed NOR/PSRAM read timings[1] (continued)

Symbol	Parameter	Min	Max	Unit
$t_{su(NWAITV-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	6	-	ns
$t_{h(CLKH-NWAITV)}$	FSMC_NWAIT valid after FSMC_CLK high	0	-	ns

1. C_L = 30 pF.

Figure 25. Synchronous non-multiplexed PSRAM write timings

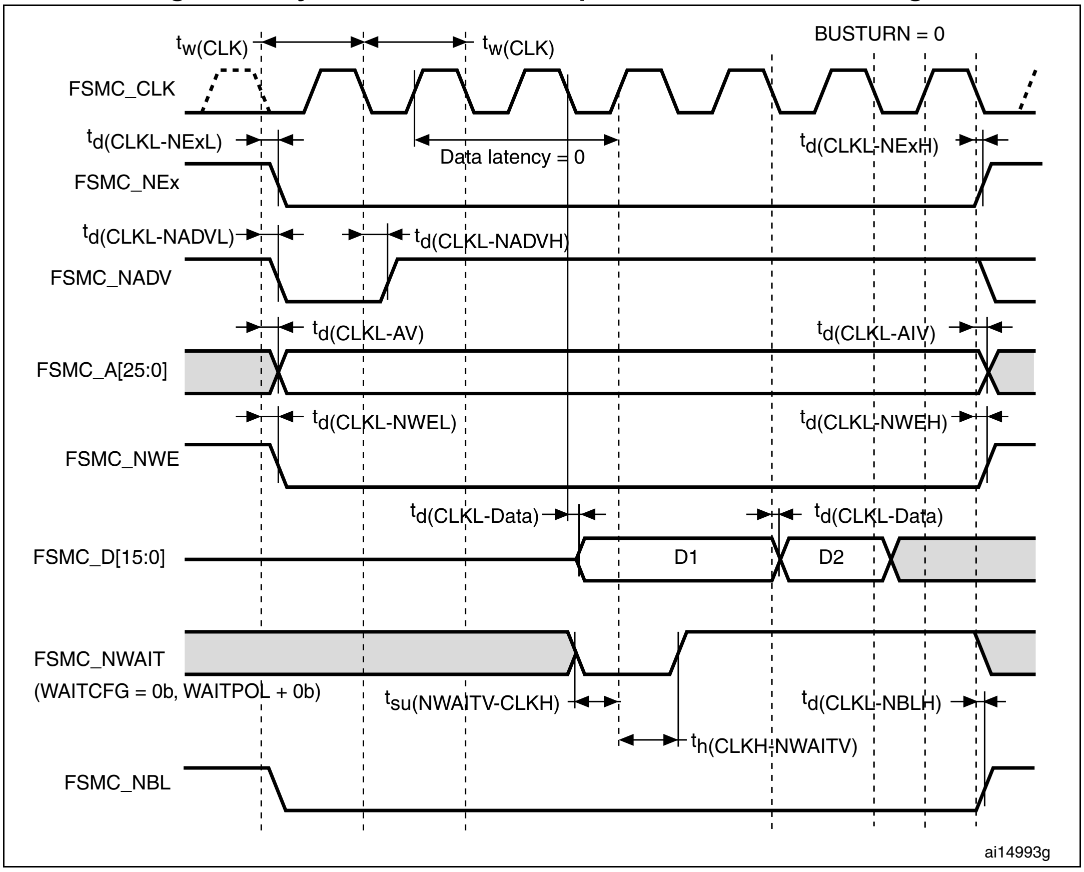
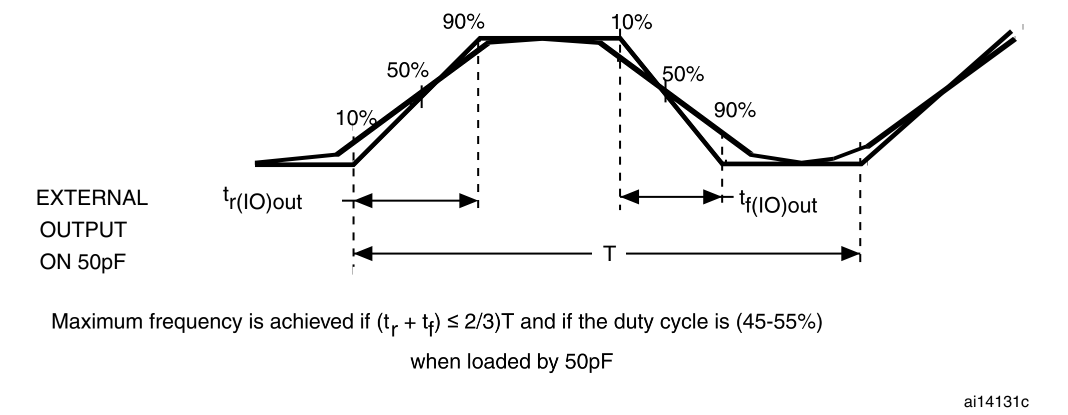


Table 44. Synchronous non-multiplexed PSRAM write timings[1]

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	$2*T_{HCLK}$ -3	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x = 0...2)	-	0	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x = 0...2)	1	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	5	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	7	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 16...25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x = 16...25)	T_{HCLK} + 4	-	ns
$t_{d(CLKL-NWEL)}$	FSMC_CLK low to FSMC_NWE low	-	2	ns

Figure 26. I/O AC characteristics definition



6.3.15 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 53*)

Unless otherwise specified, the parameters given in *Table 53* are derived from tests performed under the conditions summarized in *Table 13*.

Table 53. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST input low level voltage	-	-	-	0.3 V_{DD}	V
$V_{IH(NRST)}$(1)	NRST input high level voltage	-	0.7 V_{DD}	-	-	V
$V_{OL(NRST)}$(1)	NRST output low level voltage	I_{OL} = 2 mA 2.7 V < V_{DD} < 3.6 V	-	-	0.4	V
		I_{OL} = 1.5 mA 1.65 V < V_{DD} < 2.7 V	-	-		
$V_{hys(NRST)}$(1)	NRST Schmitt trigger voltage hysteresis	-	-	10%V_{DD}(2)	-	mV
R_{PU}	Weak pull-up equivalent resistor(3)	V_{IN} = V_{SS}	30	45	60	kΩ
$V_{F(NRST)}$(1)	NRST input filtered pulse	-	-	-	50	ns
$V_{NF(NRST)}$(3)	NRST input not filtered pulse	-	350	-	-	ns

1. Guaranteed by design.
2. With a minimum of 200 mV.
3. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is around 10%.

6.3.18 SDIO characteristics

Table 62. SDIO characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{PP}	Clock frequency in data transfer mode	CL ≤30 pF	0	24	MHz
$t_{W(CKL)}$	Clock low time, f_{PP} = 24 MHz	CL ≤30 pF	20(2)	-	ns
$t_{W(CKH)}$	Clock high time, f_{PP} = 24 MHz	CL ≤30 pF	18(2)	-	
t_r	Clock rise time, f_{PP} = 24 MHz	CL ≤30 pF	-	5	
t_f	Clock fall time, f_{PP} = 24 MHz	CL ≤30 pF	-	5	
CMD, D inputs (referenced to CK) in SD default mode					
-			From 2.8 to 3.6 V	-	-
t_{ISU}	Input setup time, f_{PP} = 24 MHz	CL ≤30 pF	2	-	ns
t_{IH}	Input hold time, f_{PP} = 24 MHz	CL ≤30 pF	1.6	-	
CMD, D outputs (referenced to CK) in SD default mode					
t_{OVD}	Output valid default time, f_{PP} = 24 MHz	CL ≤30 pF	0	14	ns
t_{OHD}	Output hold default time, f_{PP} = 24 MHz	CL ≤30 pF	0	-	

1. Guaranteed by characterization results.
2. Values measured with a threshold level equal to $V_{DD}/2$.

Figure 35. SDIO timings

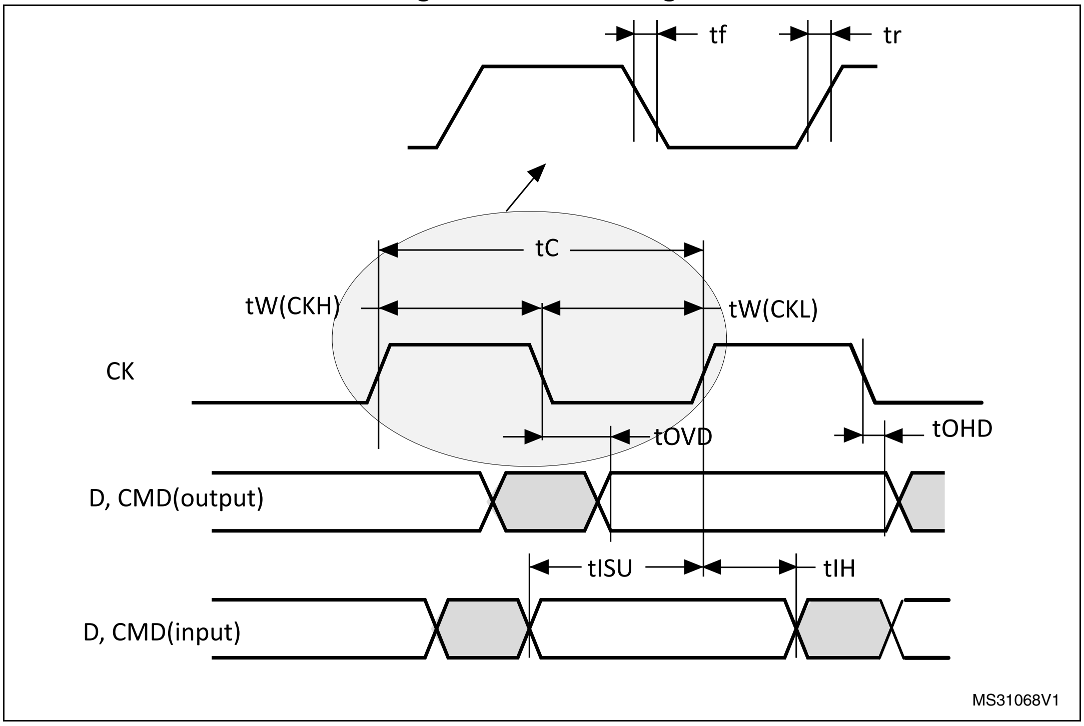


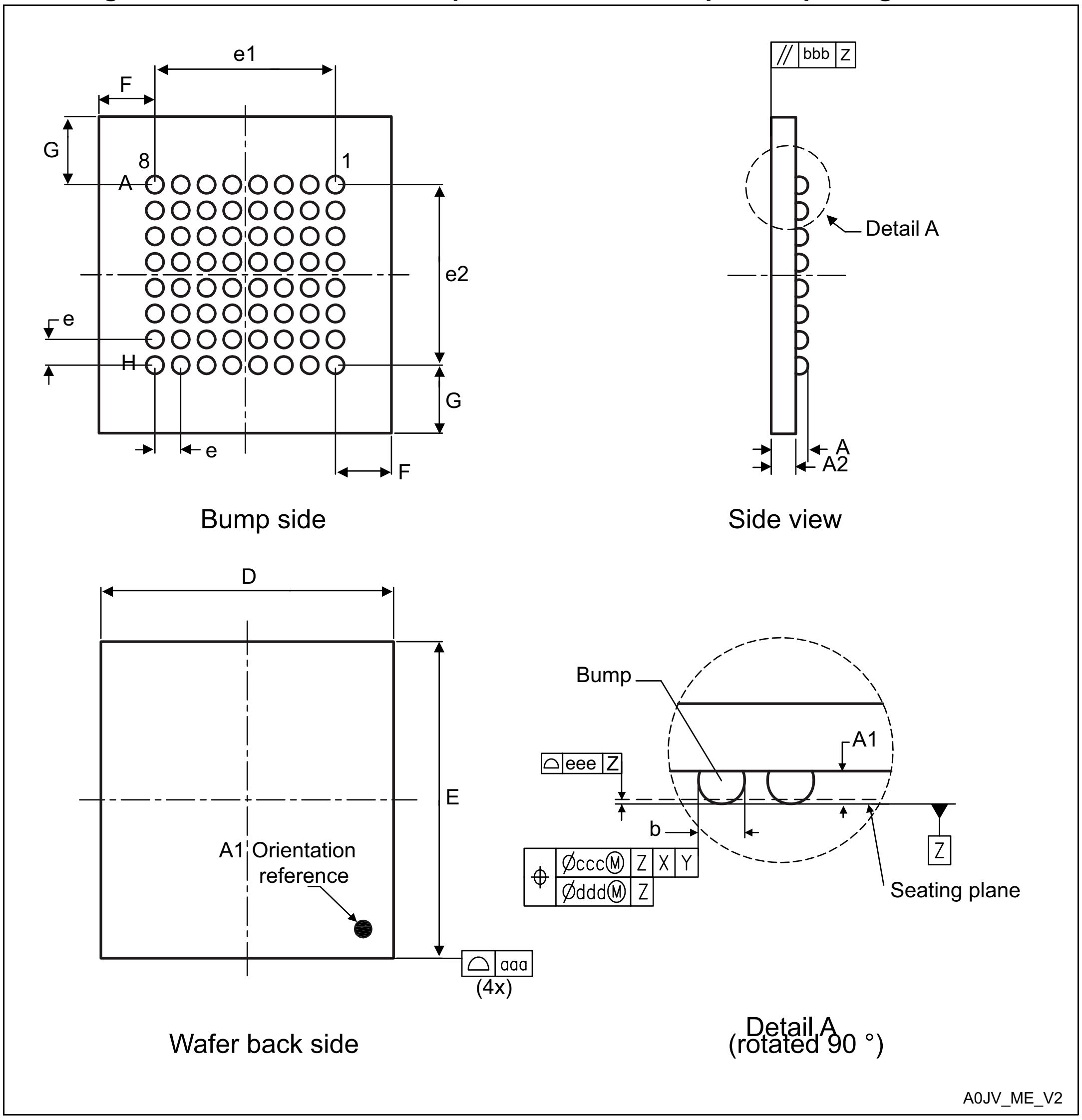
Table 67. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
dOffset/dT(1)	Offset error temperature coefficient (code 0x800)	V_{DDA} = 3.3V V_{REF+} = 3.0V T_A = 0 to 50 °C DAC output buffer OFF	-20	-10	0	μV/°C
		V_{DDA} = 3.3V V_{REF+} = 3.0V T_A = 0 to 50 °C DAC output buffer ON	0	20	50	
Gain(1)	Gain error(7)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON	-	+0.1 / -0.2%	+0.2 / -0.5%	%
		No R_L, $C_L \leq 50$ pF DAC output buffer OFF	-	+0 / -0.2%	+0 / -0.4%	
dGain/dT(1)	Gain error temperature coefficient	V_{DDA} = 3.3V V_{REF+} = 3.0V T_A = 0 to 50 °C DAC output buffer OFF	-10	-2	0	μV/°C
		V_{DDA} = 3.3V V_{REF+} = 3.0V T_A = 0 to 50 °C DAC output buffer ON	-40	-8	0	
TUE(1)	Total unadjusted error	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON	-	12	30	LSB
		No R_L, $C_L \leq 50$ pF DAC output buffer OFF	-	8	12	
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes till DAC_OUT reaches final value ±1LSB	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ	-	7	12	μs
Update rate	Max frequency for a correct DAC_OUT change (95% of final value) with 1 LSB variation in the input code	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ	-	-	1	Msps
t_{WAKEUP}	Wakeup time from off state (setting the ENx bit in the DAC Control register)(8)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ	-	9	15	μs
PSRR+	V_{DDA} supply rejection ratio (static DC measurement)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ	-	-60	-35	dB

1. Data based on characterization results.
2. Connected between DAC_OUT and V_{SSA}.
3. Difference between two consecutive codes - 1 LSB.

7.5 WLCSP64, 0.4 mm pitch wafer level chip scale package information

Figure 52. WLCSP64, 0.4 mm pitch wafer level chip scale package outline



1. Drawing is not to scale.

Table 78. WLCSP64, 0.4 mm pitch wafer level chip scale package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	0.540	0.570	0.600	0.0205	0.0224	0.0236
A1	-	0.190	-	-	0.0075	-
A2	-	0.380	-	-	0.0150	-

Table 78. WLCSP64, 0.4 mm pitch wafer level chip scale package mechanical data (continued)

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
b(2)	0.240	0.270	0.300	0.0094	0.0106	0.0118
D	4.504	4.539	4.574	0.1773	0.1787	0.1801
E	4.876	4.911	4.946	0.1920	0.1933	0.1947
e	-	0.400	-	-	0.0157	-
e1	-	2.800	-	-	0.1102	-
F	-	0.870	-	-	0.0343	-
G	-	1.056	-	-	0.0416	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 53. WLCSP64, 0.4 mm pitch wafer level chip scale package recommended footprint

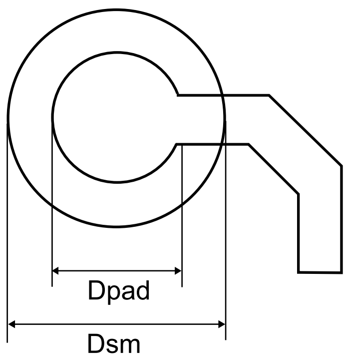


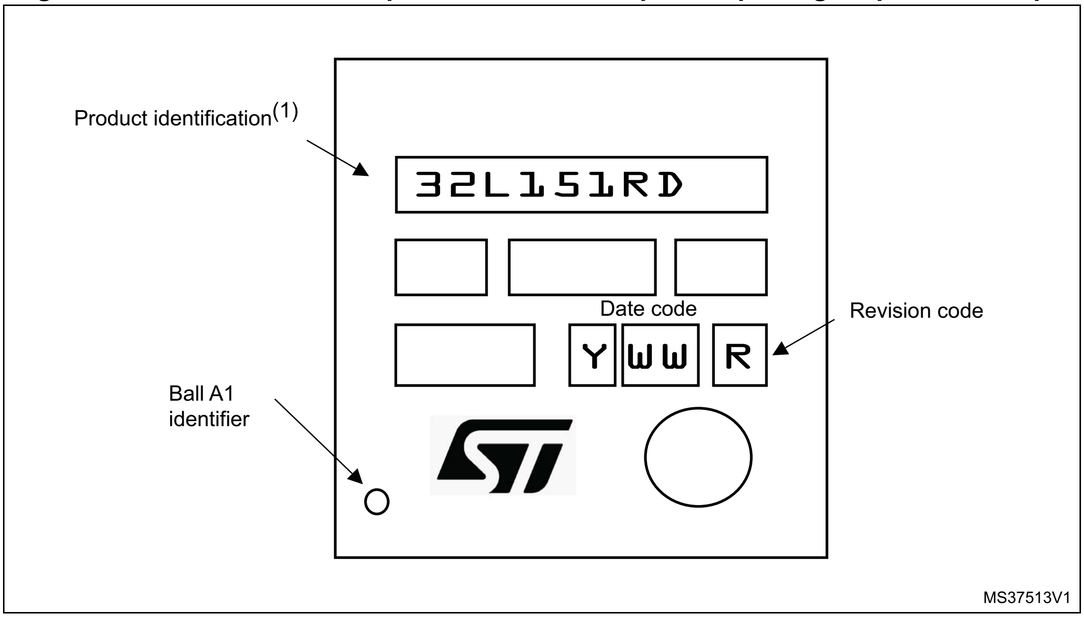
Table 79. WLCSP64, 0.4 mm pitch package recommended PCB design rules

Dimension	Recommended values
Pitch	0.4
Dpad	260 µm max. (circular)
	220 µm recommended
Dsm	300 µm min. (for 260 µm diameter pad)
PCB pad design	Non-solder mask defined via underbump allowed.

Marking of engineering samples

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Figure 54. WLCSP64, 0.4 mm pitch wafer level chip scale package top view example



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity