Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	55MHz
Connectivity	CANbus, Ethernet, I²C, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	62
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 1.95V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-TFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at91sam7xc256-cu

- **Fully Static Operation: Up to 55 MHz at 1.65V and 85· C Worst Case Conditions**
- **Available in 100-lead LQFP Green and 100-ball TFBGA Green Packages**

1. Description

Atmel's AT91SAM7XC512/256/128 is a member of a series of highly integrated Flash microcontrollers based on the 32-bit ARM RISC processor. It features 512/256/128 Kbyte high-speed Flash and 128/64/32 Kbyte SRAM, a large set of peripherals, including an 802.3 Ethernet MAC, a CAN controller, an AES 128 Encryption accelerator and a Triple Data Encryption System. A complete set of system functions minimizes the number of external components.

The embedded Flash memory can be programmed in-system via the JTAG-ICE interface or via a parallel interface on a production programmer prior to mounting. Built-in lock bits and a security bit protect the firmware from accidental overwrite and preserve its confidentiality.

The AT91SAM7XC512/256/128 system controller includes a reset controller capable of managing the power-on sequence of the microcontroller and the complete system. Correct device operation can be monitored by a built-in brownout detector and a watchdog running off an integrated RC oscillator.

By combining the ARM7TDMI processor with on-chip Flash and SRAM, and a wide range of peripheral functions, including USART, SPI, CAN Controller, Ethernet MAC, AES 128 accelerator, TDES, Timer Counter, RTT and Analog-to-Digital Converters on a monolithic chip, the AT91SAM7XC512/256/128 is a powerful device that provides a flexible, cost-effective solution to many embedded control applications requiring secure communication over, for example, Ethernet, CAN wired and Zigbee™ wireless networks.

1.1 Configuration Summary of the AT91SAM7XC512/256/128

The AT91SAM7XC512, AT91SAM7XC256 and AT91SAM7XC128 differ only in memory sizes. Table 1-1 summarizes the configurations of the two devices.

Table 1-1. Configuration Summary

Device	Flash	Flash Organization	SRAM	AES	TDES
AT91SAM7XC512	512K bytes	dual plane	128K bytes	1 AES 256/192/128	1
AT91SAM7XC256	256K bytes	single plane	64K bytes	1 AES 128	1
AT91SAM7XC128	128K bytes	single plane	32K bytes	1 AES 128	1

3. Signal Description

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
Power				
VDDIN	Voltage Regulator and ADC Power Supply Input	Power		3V to 3.6V
VDDOUT	Voltage Regulator Output	Power		1.85V
VDDFLASH	Flash and USB Power Supply	Power		3V to 3.6V
VDDIO	I/O Lines Power Supply	Power		3V to 3.6V
VDDCORE	Core Power Supply	Power		1.65V to 1.95V
VDDPLL	PLL	Power		1.65V to 1.95V
GND	Ground	Ground		
Clocks, Oscillators and PLLs				
XIN	Main Oscillator Input	Input		
XOUT	Main Oscillator Output	Output		
PLLRC	PLL Filter	Input		
PCK0 - PCK3	Programmable Clock Output	Output		
ICE and JTAG				
TCK	Test Clock	Input		No pull-up resistor
TDI	Test Data In	Input		No pull-up resistor
TDO	Test Data Out	Output		
TMS	Test Mode Select	Input		No pull-up resistor
JTAGSEL	JTAG Selection	Input		Pull-down resistor(1)
Flash Memory				
ERASE	Flash and NVM Configuration Bits Erase Command	Input	High	Pull-down resistor(1)
Reset/Test				
NRST	Microcontroller Reset	I/O	Low	Pull-Up resistor, Open Drain Output.
TST	Test Mode Select	Input	High	Pull-down resistor(1)
Debug Unit				
DRXD	Debug Receive Data	Input		
DTXD	Debug Transmit Data	Output		
AIC				
IRQ0 - IRQ1	External Interrupt Inputs	Input		
FIQ	Fast Interrupt Input	Input		
PIO				
PA0 - PA30	Parallel IO Controller A	I/O		Pulled-up input at reset.
PB0 - PB30	Parallel IO Controller B	I/O		Pulled-up input at reset.

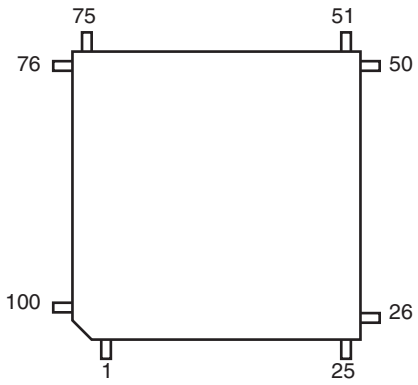
4. Package

The AT91SAM7XC512/256/128 is available in 100-lead LQFP Green and 100-ball TFBGA RoHS-compliant packages.

4.1 100-lead LQFP Package Outline

Figure 4-1 shows the orientation of the 100-lead LQFP package. A detailed mechanical description is given in the Mechanical Characteristics section of the full datasheet.

Figure 4-1. 100-lead LQFP Package Outline (Top View)



4.2 100-lead LQFP Pinout

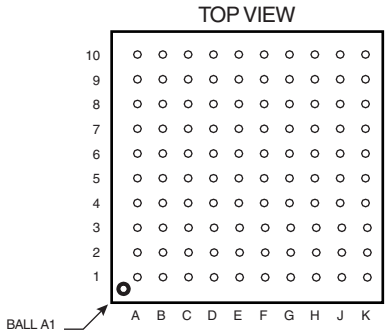
Table 4-1. Pinout in 100-lead LQFP Package

1	ADVREF	26	PA18/PGMD6	51	TDI	76	TDO
2	GND	27	PB9	52	GND	77	JTAGSEL
3	AD4	28	PB8	53	PB16	78	TMS
4	AD5	29	PB14	54	PB4	79	TCK
5	AD6	30	PB13	55	PA23/PGMD11	80	PA30
6	AD7	31	PB6	56	PA24/PGMD12	81	PA0/PGMEN0
7	VDDOUT	32	GND	57	NRST	82	PA1/PGMEN1
8	VDDIN	33	VDDIO	58	TST	83	GND
9	PB27/AD0	34	PB5	59	PA25/PGMD13	84	VDDIO
10	PB28/AD1	35	PB15	60	PA26/PGMD14	85	PA3
11	PB29/AD2	36	PB17	61	VDDIO	86	PA2
12	PB30/AD3	37	VDDCORE	62	VDDCORE	87	VDDCORE
13	PA8/PGMM0	38	PB7	63	PB18	88	PA4/PGMNCMD
14	PA9/PGMM1	39	PB12	64	PB19	89	PA5/PGMRDY
15	VDDCORE	40	PB0	65	PB20	90	PA6/PGMNOE
16	GND	41	PB1	66	PB21	91	PA7/PGMNVALID
17	VDDIO	42	PB2	67	PB22	92	ERASE
18	PA10/PGMM2	43	PB3	68	GND	93	DDM
19	PA11/PGMM3	44	PB10	69	PB23	94	DDP
20	PA12/PGMD0	45	PB11	70	PB24	95	VDDFLASH
21	PA13/PGMD1	46	PA19/PGMD7	71	PB25	96	GND
22	PA14/PGMD2	47	PA20/PGMD8	72	PB26	97	XIN/PGMCK
23	PA15/PGMD3	48	VDDIO	73	PA27/PGMD15	98	XOUT
24	PA16/PGMD4	49	PA21/PGMD9	74	PA28	99	PLLRC
25	PA17/PGMD5	50	PA22/PGMD10	75	PA29	100	VDDPLL

4.3 100-ball TFBGA Package Outline

Figure 4-2 shows the orientation of the 100-ball TFBGA package. A detailed mechanical description is given in the Mechanical Characteristics section of the full datasheet.

Figure 4-2. 100-ball TFBGA Package Orientation (Top View)



4.4 100-ball TFBGA Pinout

Table 4-2. Pinout in 100-ball TFBGA Package

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	PA22/PGMD10	C6	PB17	F1	PB21	H6	PA7/PGMNVALID
A2	PA21/PGMD9	C7	PB13	F2	PB23	H7	PA9/PGMM1
A3	PA20/PGMD8	C8	PA13/PGMD1	F3	PB25	H8	PA8/PGMM0
A4	PB1	C9	PA12/PGMD0	F4	PB26	H9	PB29/AD2
A5	PB7	C10	PA15/PGMD3	F5	TCK	H10	PLLRC
A6	PB5	D1	PA23/PGMD11	F6	PA6/PGMNOE	J1	PA29
A7	PB8	D2	PA24/PGMD12	F7	ERASE	J2	PA30
A8	PB9	D3	NRST	F8	VDDCORE	J3	PA0/PGMEN0
A9	PA18/PGMD6	D4	TST	F9	GND	J4	PA1/PGMEN1
A10	VDDIO	D5	PB19	F10	VDDIN	J5	VDDFLASH
B1	TDI	D6	PB6	G1	PB22	J6	GND
B2	PA19/PGMD7	D7	PA10/PGMM2	G2	PB24	J7	XIN/PGMCK
B3	PB11	D8	VDDIO	G3	PA27/PGMD15	J8	XOUT
B4	PB2	D9	PB27/AD0	G4	TDO	J9	GND
B5	PB12	D10	PA11/PGMM3	G5	PA2	J10	VDDPLL
B6	PB15	E1	PA25/PGMD13	G6	PA5/PGMRDY	K1	VDDCORE
B7	PB14	E2	PA26/PGMD14	G7	VDDCORE	K2	VDDCORE
B8	PA14/PGMD2	E3	PB18	G8	GND	K3	DDP
B9	PA16/PGMD4	E4	PB20	G9	PB30/AD3	K4	DDM
B10	PA17/PGMD5	E5	TMS	G10	VDDOUT	K5	GND
C1	PB16	E6	GND	H1	VDDCORE	K6	AD7
C2	PB4	E7	VDDIO	H2	PA28	K7	AD6
C3	PB10	E8	PB28/AD1	H3	JTAGSEL	K8	AD5
C4	PB3	E9	VDDIO	H4	PA3	K9	AD4
C5	PB0	E10	GND	H5	PA4/PGMNCMD	K10	ADVREF

5. Power Considerations

5.1 Power Supplies

The AT91SAM7XC512/256/128 has six types of power supply pins and integrates a voltage regulator, allowing the device to be supplied with only one voltage. The six power supply pin types are:

- VDDIN pin. It powers the voltage regulator and the ADC; voltage ranges from 3.0V to 3.6V, 3.3V nominal. In order to decrease current consumption, if the voltage regulator and the ADC are not used, VDDIN, ADVREF,AD4, AD5, AD6 and AD7 should be connected to GND. In this case, VDDOUT should be left unconnected.
- VDDOUT pin. It is the output of the 1.8V voltage regulator.
- VDDIO pin. It powers the I/O lines; voltage ranges from 3.0V to 3.6V, 3.3V nominal.
- VDDFLASH pin. It powers the USB transceivers and a part of the Flash and is required for the Flash to operate correctly; voltage ranges from 3.0V to 3.6V, 3.3V nominal.
- VDDCORE pins. They power the logic of the device; voltage ranges from 1.65V to 1.95V, 1.8V typical. It can be connected to the VDDOUT pin with decoupling capacitor. VDDCORE is required for the device, including its embedded Flash, to operate correctly.
- VDDPLL pin. It powers the oscillator and the PLL. It can be connected directly to the VDDOUT pin.

No separate ground pins are provided for the different power supplies. Only GND pins are provided and should be connected as shortly as possible to the system ground plane.

5.2 Power Consumption

The AT91SAM7XC512/256/128 has a static current of less than 60 µA on VDDCORE at 25°C, including the RC oscillator, the voltage regulator and the power-on reset when the brownout detector is deactivated. Activating the brownout detector adds 28 µA static current.

The dynamic power consumption on VDDCORE is less than 90 mA at full speed when running out of the Flash. Under the same conditions, the power consumption on VDDFLASH does not exceed 10 mA.

5.3 Voltage Regulator

The AT91SAM7XC512/256/128 embeds a voltage regulator that is managed by the System Controller.

In Normal Mode, the voltage regulator consumes less than 100 µA static current and draws 100 mA of output current.

The voltage regulator also has a Low-power Mode. In this mode, it consumes less than 25 µA static current and draws 1 mA of output current.

Adequate output supply decoupling is mandatory for VDDOUT to reduce ripple and avoid oscillations. The best way to achieve this is to use two capacitors in parallel: one external 470 pF (or 1 nF) NPO capacitor should be connected between VDDOUT and GND as close to the chip as possible. One external 2.2 µF (or 3.3 µF) X7R capacitor should be connected between VDDOUT and GND.

5V-tolerant means that the I/O lines can drive voltage level according to VDDIO, but can be driven with a voltage of up to 5.5V. However, driving an I/O line with a voltage over VDDIO while the programmable pull-up resistor is enabled will create a current path through the pull-up resistor from the I/O line to VDDIO. Care should be taken, in particular at reset, as all the I/O lines default to input with pull-up resistor enabled at reset.

6.6 I/O Lines Current Drawing

The PIO lines PA0 to PA3 are high-drive current capable. Each of these I/O lines can drive up to 16 mA permanently.

The remaining I/O lines can draw only 8 mA.

However, the total current drawn by all the I/O lines cannot exceed 200 mA.

7. Processor and Architecture

7.1 ARM7TDMI Processor

- RISC processor based on ARMv4T Von Neumann architecture
  - Runs at up to 55 MHz, providing 0.9 MIPS/MHz
- Two instruction sets
  - ARM® high-performance 32-bit instruction set
  - Thumb® high code density 16-bit instruction set
- Three-stage pipeline architecture
  - Instruction Fetch (F)
  - Instruction Decode (D)
  - Execute (E)

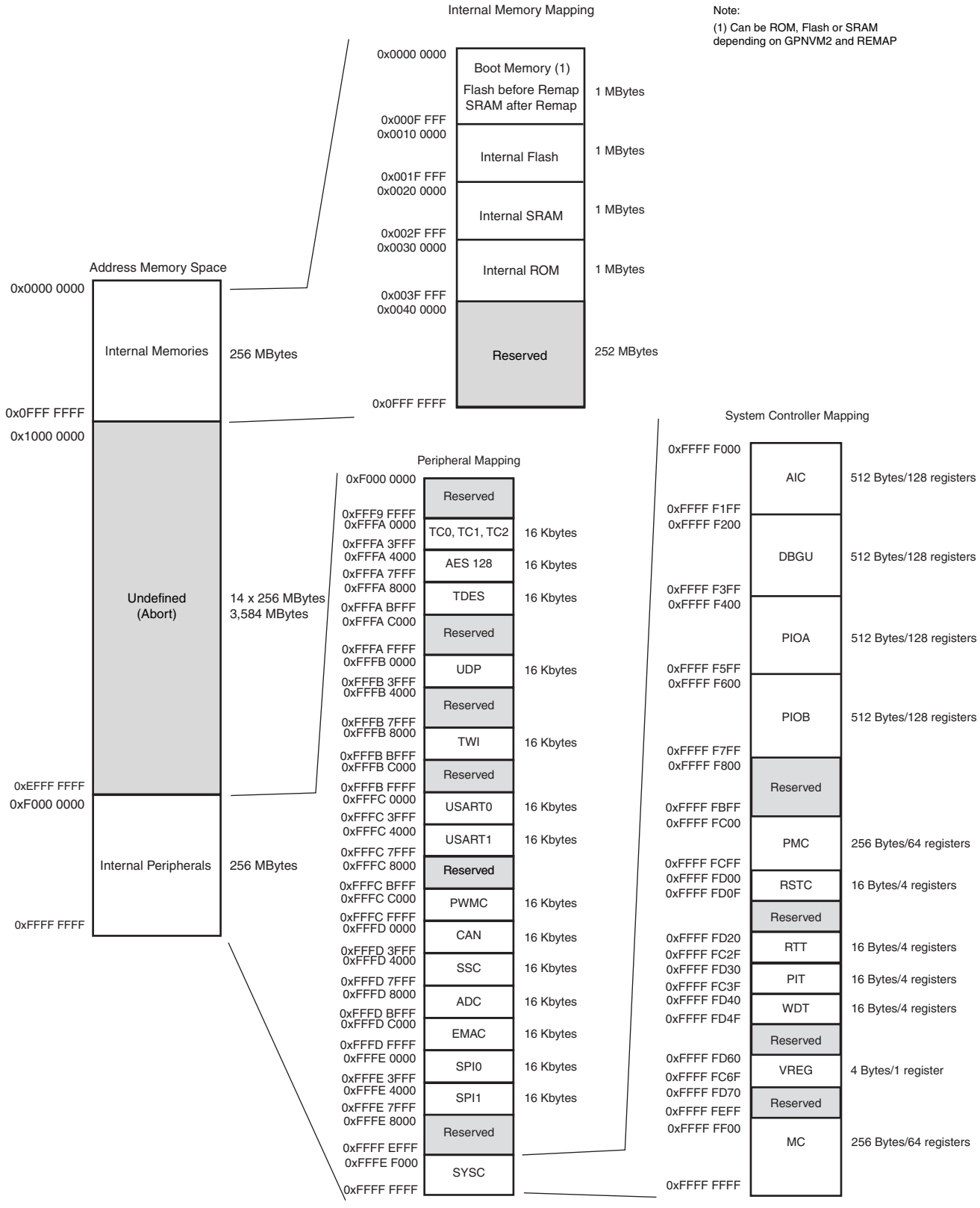
7.2 Debug and Test Features

- Integrated embedded in-circuit emulator
  - Two watchpoint units
  - Test access port accessible through a JTAG protocol
  - Debug communication channel
- Debug Unit
  - Two-pin UART
  - Debug communication channel interrupt handling
  - Chip ID Register
- IEEE1149.1 JTAG Boundary-scan on all digital pins

7.3 Memory Controller

- Programmable Bus Arbiter
  - Handles requests from the ARM7TDMI, the Ethernet MAC and the Peripheral DMA Controller
- Address decoder provides selection signals for
  - Three internal 1 Mbyte memory areas
  - One 256 Mbyte embedded peripheral area
- Abort Status Registers
  - Source, Type and all parameters of the access leading to an abort are saved
  - Facilitates debug by detection of bad pointers
- Misalignment Detector
  - Alignment checking of all data accesses
  - Abort generation in case of misalignment
- Remap Command
  - Remaps the SRAM in place of the embedded non-volatile memory
  - Allows handling of dynamic exception vectors

Figure 8-1. AT91SAM7XC512/256/128 Memory Mapping



plane may be performed even while program or erase functions are being executed in the other memory plane.

One EFC is embedded in the AT91SAM7XC256/128 to control the single plane of 256/128 KBytes.

8.5.3 Lock Regions

8.5.3.1 AT91SAM7XC512

Two Embedded Flash Controllers each manage 16 lock bits to protect 16 regions of the flash against inadvertent flash erasing or programming commands. The AT91SAM7XC512 contains 32 lock regions and each lock region contains 64 pages of 256 bytes. Each lock region has a size of 16 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the EFC trigs an interrupt.

The 32 NVM bits are software programmable through both of the EFC User Interfaces. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

8.5.3.2 AT91SAM7XC256

The Embedded Flash Controller manages 16 lock bits to protect 16 regions of the flash against inadvertent flash erasing or programming commands. The AT91SAM7XC256 contains 16 lock regions and each lock region contains 64 pages of 256 bytes. Each lock region has a size of 16 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the EFC trigs an interrupt.

The 16 NVM bits are software programmable through the EFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

8.5.3.3 AT91SAM7XC128

The Embedded Flash Controller manages 8 lock bits to protect 8 regions of the flash against inadvertent flash erasing or programming commands. The AT91SAM7XC128 contains 8 lock regions and each lock region contains 64 pages of 256 bytes. Each lock region has a size of 16 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the EFC trigs an interrupt.

The 8 NVM bits are software programmable through the EFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

8.5.4 Security Bit Feature

The AT91SAM7XC512/256/128 features a security bit, based on a specific NVM-Bit. When the security is enabled, any access to the Flash, either through the ICE interface or through the Fast

Flash Programming Interface, is forbidden. This ensures the confidentiality of the code programmed in the Flash.

This security bit can only be enabled, through the Command “Set Security Bit” of the EFC User Interface. Disabling the security bit can only be achieved by asserting the ERASE pin at 1, and after a full flash erase is performed. When the security bit is deactivated, all accesses to the flash are permitted.

It is important to note that the assertion of the ERASE pin should always be longer than 220 ms.

As the ERASE pin integrates a permanent pull-down, it can be left unconnected during normal operation. However, it is safer to connect it directly to GND for the final application.

8.5.5 Non-volatile Brownout Detector Control

Two general purpose NVM (GPNVM) bits are used for controlling the brownout detector (BOD), so that even after a power loss, the brownout detector operations remain in their state.

These two GPNVM bits can be cleared or set respectively through the commands “Clear General-purpose NVM Bit” and “Set General-purpose NVM Bit” of the EFC User Interface.

- GPNVM Bit 0 is used as a brownout detector enable bit. Setting the GPNVM Bit 0 enables the BOD, clearing it disables the BOD. Asserting ERASE clears the GPNVM Bit 0 and thus disables the brownout detector by default.
- The GPNVM Bit 1 is used as a brownout reset enable signal for the reset controller. Setting the GPNVM Bit 1 enables the brownout reset when a brownout is detected, Clearing the GPNVM Bit 1 disables the brownout reset. Asserting ERASE disables the brownout reset by default.

8.5.6 Calibration Bits

Eight NVM bits are used to calibrate the brownout detector and the voltage regulator. These bits are factory configured and cannot be changed by the user. The ERASE pin has no effect on the calibration bits.

8.6 Fast Flash Programming Interface

The Fast Flash Programming Interface allows programming the device through either a serial JTAG interface or through a multiplexed fully-handshaked parallel port. It allows gang-programming with market-standard industrial programmers.

The FFPI supports read, page program, page erase, full erase, lock, unlock and protect commands.

The Fast Flash Programming Interface is enabled and the Fast Programming Mode is entered when the TST pin and the PA0 and PA1 pins are all tied high.

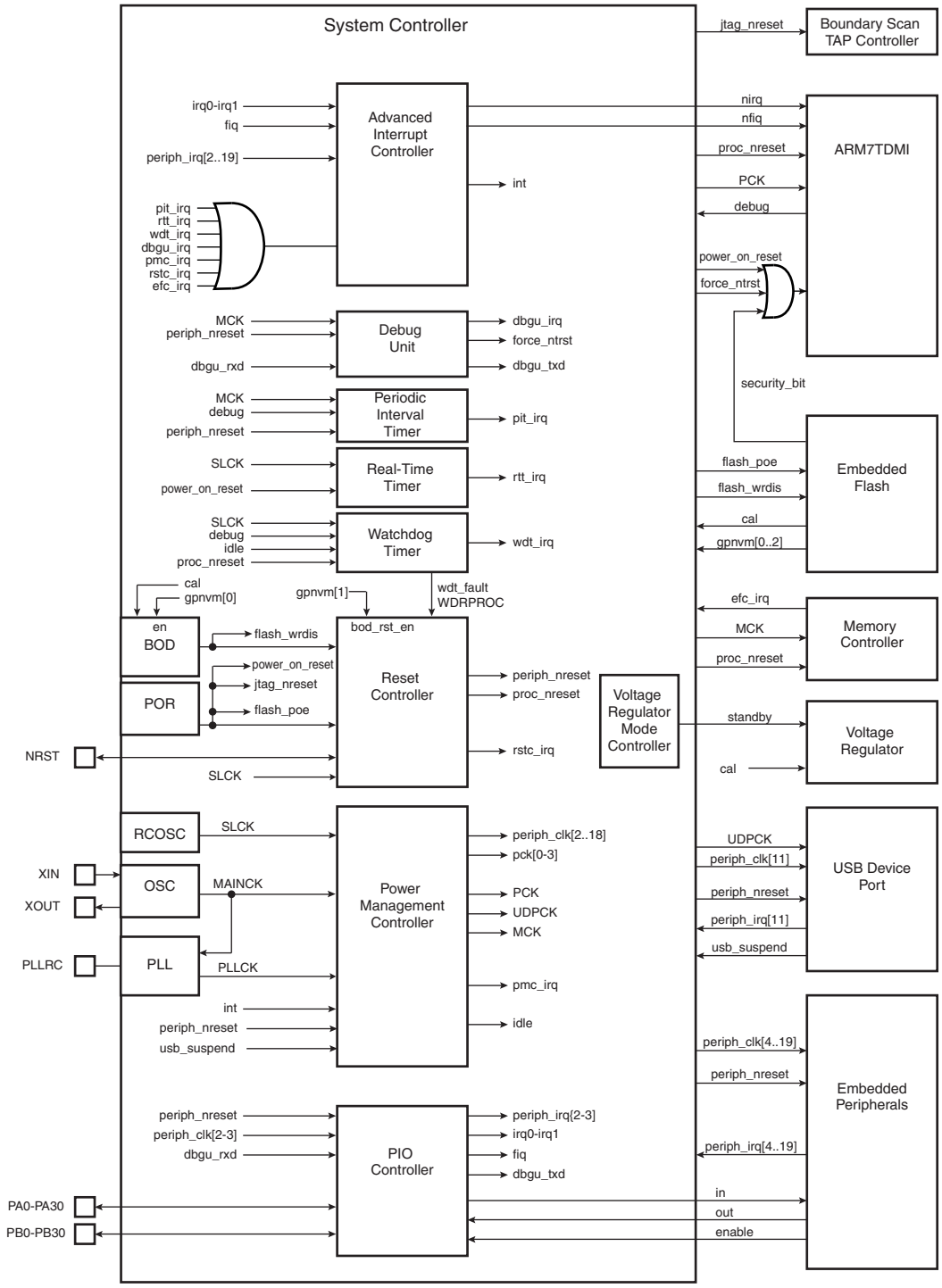
8.7 SAM-BA Boot Assistant

The SAM-BA Boot Assistant is a default Boot Program that provides an easy way to program in-situ the on-chip Flash memory.

The SAM-BA Boot Assistant supports serial communication via the DBGU or the USB Device Port.

- Communication via the DBGU supports a wide range of crystals from 3 to 20 MHz via software auto-detection.

Figure 9-1. System Controller Block Diagram



9.3 Power Management Controller

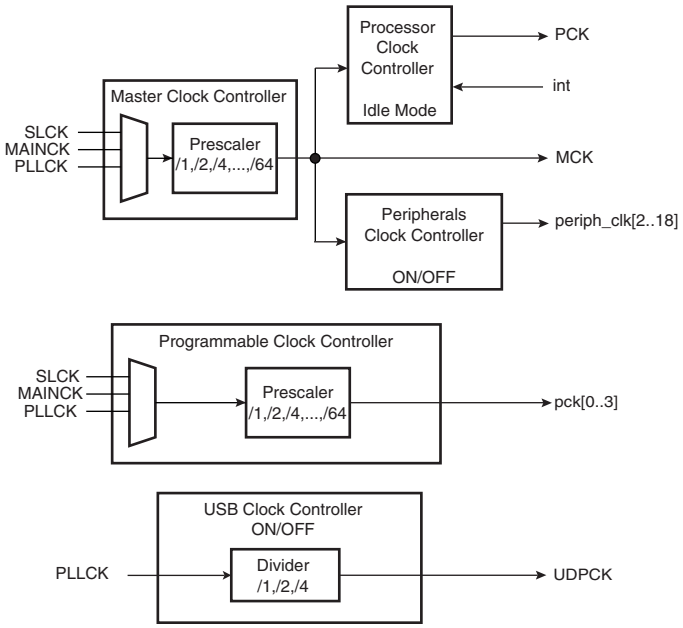
The Power Management Controller uses the Clock Generator outputs to provide:

- the Processor Clock PCK
- the Master Clock MCK
- the USB Clock UDPCK
- all the peripheral clocks, independently controllable
- four programmable clock outputs

The Master Clock (MCK) is programmable from a few hundred Hz to the maximum operating frequency of the device.

The Processor Clock (PCK) switches off when entering processor idle mode, thus allowing reduced power consumption while waiting for an interrupt.

Figure 9-3. Power Management Controller Block Diagram



9.4 Advanced Interrupt Controller

- Controls the interrupt lines (nIRQ and nFIQ) of an ARM Processor
- Individually maskable and vectored interrupt sources
  - Source 0 is reserved for the Fast Interrupt Input (FIQ)
  - Source 1 is reserved for system peripherals (RTT, PIT, EFC, PMC, DBGU, etc.)
  - Other sources control the peripheral interrupts or external interrupts
  - Programmable edge-triggered or level-sensitive internal sources
  - Programmable positive/negative edge-triggered or high/low level-sensitive external sources
- 8-level Priority Controller
  - Drives the normal interrupt nIRQ of the processor
  - Handles priority of the interrupt sources

  - Higher priority interrupts can be served during service of lower priority interrupt
- Vectoring
  - Optimizes interrupt service routine branch and execution
  - One 32-bit vector register per interrupt source
  - Interrupt vector register reads the corresponding current interrupt vector
- Protect Mode
  - Easy debugging by preventing automatic operations
- Fast Forcing
  - Permits redirecting any interrupt source on the fast interrupt
- General Interrupt Mask
  - Provides processor synchronization on events without triggering an interrupt

9.5 Debug Unit

- Comprises:
  - One two-pin UART
  - One Interface for the Debug Communication Channel (DCC) support
  - One set of Chip ID Registers
  - One Interface providing ICE Access Prevention
- Two-pin UART
  - USART-compatible User Interface
  - Programmable Baud Rate Generator
  - Parity, Framing and Overrun Error
  - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
- Debug Communication Channel Support
  - Offers visibility of COMMRX and COMMTX signals from the ARM Processor
- Chip ID Registers
  - Identification of the device revision, sizes of the embedded memories, set of peripherals
  - Chip ID is 0x271C 0A40 (VERSION 0) for AT91SAM7XC512
  - Chip ID is 0x271B 0940 (VERSION 0) for AT91SAM7XC256
  - Chip ID is 0x271A 0740 (VERSION 0) for AT91SAM7XC128

9.6 Periodic Interval Timer

- 20-bit programmable counter plus 12-bit interval counter

9.7 Watchdog Timer

- 12-bit key-protected Programmable Counter running on prescaled SLCK
- Provides reset or interrupt signals to the system
- Counter may be stopped while the processor is in debug state or in idle mode

9.8 Real-time Timer

- 32-bit free-running counter with alarm running on prescaled SLCK

10. Peripherals

10.1 User Interface

The User Peripherals are mapped in the 256 MBytes of address space between 0xF000 0000 and 0xFFFE FFFF. Each peripheral is allocated 16 Kbytes of address space.

A complete memory map is provided in Figure 8-1 on page 19.

10.2 Peripheral Identifiers

The AT91SAM7XC512/256/128 embeds a wide range of peripherals. Table 10-1 defines the Peripheral Identifiers of the AT91SAM7XC512/256/128. Unique peripheral identifiers are defined for both the Advanced Interrupt Controller and the Power Management Controller.

Table 10-1. Peripheral Identifiers

Peripheral ID	Peripheral Mnemonic	Peripheral Name	External Interrupt
0	AIC	Advanced Interrupt Controller	FIQ
1	SYSC(1)	System	
2	PIOA	Parallel I/O Controller A	
3	PIOB	Parallel I/O Controller B	
4	SPI0	Serial Peripheral Interface 0	
5	SPI1	Serial Peripheral Interface 1	
6	US0	USART 0	
7	US1	USART 1	
8	SSC	Synchronous Serial Controller	
9	TWI	Two-wire Interface	
10	PWMC	Pulse Width Modulation Controller	
11	UDP	USB device Port	
12	TC0	Timer/Counter 0	
13	TC1	Timer/Counter 1	
14	TC2	Timer/Counter 2	
15	CAN	CAN Controller	
16	EMAC	Ethernet MAC	
17	ADC(1)	Analog-to Digital Converter	
18	AES	Advanced Encryption Standard 128-bit	
19	TDES	Triple Data Encryption Standard	
20-29	Reserved		
30	AIC	Advanced Interrupt Controller	IRQ0
31	AIC	Advanced Interrupt Controller	IRQ1

Note: 1. Setting SYSC and ADC bits in the clock set/clear registers of the PMC has no effect. The System Controller and ADC are continuously clocked.

10.6 Ethernet MAC

- DMA Master on Receive and Transmit Channels
- Compatible with IEEE Standard 802.3
- 10 and 100 Mbit/s operation
- Full- and half-duplex operation
- Statistics Counter Registers
- MII/RMII interface to the physical layer
- Interrupt generation to signal receive and transmit completion
- 28-byte transmit FIFO and 28-byte receive FIFO
- Automatic pad and CRC generation on transmitted frames
- Automatic discard of frames received with errors
- Address checking logic supports up to four specific 48-bit addresses
- Support Promiscuous Mode where all valid received frames are copied to memory
- Hash matching of unicast and multicast destination addresses
- Physical layer management through MDIO interface
- Half-duplex flow control by forcing collisions on incoming frames
- Full-duplex flow control with recognition of incoming pause frames
- Support for 802.1Q VLAN tagging with recognition of incoming VLAN and priority tagged frames
- Multiple buffers per receive and transmit frame
- Jumbo frames up to 10240 bytes supported

10.7 Serial Peripheral Interface

- Supports communication with external serial devices
  - Four chip selects with external decoder allow communication with up to 15 peripherals
  - Serial memories, such as DataFlash® and 3-wire EEPROMs
  - Serial peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors
  - External co-processors
- Master or slave serial peripheral bus interface
  - 8- to 16-bit programmable data length per chip select
  - Programmable phase and polarity per chip select
  - Programmable transfer delays per chip select, between consecutive transfers and between clock and data
  - Programmable delay between consecutive transfers
  - Selectable mode fault detection
  - Maximum frequency at up to Master Clock

10.13 USB Device Port

- USB V2.0 full-speed compliant,12 Mbits per second
- Embedded USB V2.0 full-speed transceiver
- Embedded 1352-byte dual-port RAM for endpoints
- Six endpoints
  - Endpoint 0: 8 bytes
  - Endpoint 1 and 2: 64 bytes ping-pong
  - Endpoint 3: 64 bytes
  - Endpoint 4 and 5: 256 bytes ping-pong
  - Ping-pong Mode (two memory banks) for bulk endpoints
- Suspend/resume logic

10.14 CAN Controller

- Fully compliant with CAN 2.0A and 2.0B
- Bit rates up to 1Mbit/s
- Eight object oriented mailboxes each with the following properties:
  - CAN Specification 2.0 Part A or 2.0 Part B Programmable for each Message
  - Object configurable to receive (with overwrite or not) or transmit
  - Local tag and mask filters up to 29-bit identifier/channel
  - 32-bit access to data registers for each mailbox data object
  - Uses a 16-bit time stamp on receive and transmit message
  - Hardware concatenation of ID unmasked bitfields to speedup family ID processing
  - 16-bit internal timer for time stamping and network synchronization
  - Programmable reception buffer length up to 8 mailbox objects
  - Priority management between transmission mailboxes
  - Autobaud and listening mode
  - Low power mode and programmable wake-up on bus activity or by the application
  - Data, remote, error and overload frame handling

10.15 128-bit Advanced Encryption Standard

- Compliant with FIPS Publication 197, Advanced Encryption Standard (AES)
- 128-bit (AT91SAM7XC256/128) or 128-bit/192-bit/256-bit (AT91SAM7XC512) Cryptographic Key
- 12-clock Cycles Encryption/Decryption Processing Time (AT91SAM7XC256/128)
- 12/13/14-clock Cycles Encryption/Decryption Processing Time (AT91SAM7XC512)
- Support of the Five Standard Modes of Operation specified in the NIST Special Publication 800-38A:
  - Electronic Codebook (ECB)
  - Cipher Block Chaining (CBC)
  - Cipher Feedback (CFB)
  - Output Feedback (OFB)

  - Counter (CTR)
- 8-, 16-, 32-, 64- and 128-bit Data Sizes Possible in CFB Mode
- Last Output Data Mode allowing Message Authentication Code (MAC) generation
- Hardware Countermeasures against Differential Power Analysis attacks
- Connection to PDC Channel Capabilities Optimizes Data Transfers for all Operating Modes:
  - One Channel for the Receiver, One Channel for the Transmitter
  - Next Buffer Support

10.16 Triple Data Encryption Standard

- Single Data Encryption Standard (DES) and Triple Data Encryption
- Algorithm (TDEA or TDES) supports
- Compliant with FIPS Publication 46-3, Data Encryption Standard (DES)
- 64-bit Cryptographic Key
- Two-key or Three-key Algorithms
- 18-clock Cycles Encryption/Decryption Processing Time for DES
- 50-clock Cycles Encryption/Decryption Processing Time for TDES
- Support the Four Standard Modes of Operation specified in the FIPS Publication 81, DES
- Modes of Operation:
  - Electronic Codebook (ECB)
  - Cipher Block Chaining (CBC)
  - Cipher Feedback (CFB)
  - Output Feedback (OFB)
- 8-, 16-, 32- and 64- Data Sizes Possible in CFB Mode
- Last Output Data Mode allowing Optimized Message (Data) Authentication Code (MAC) generation
- Connection to PDC Channel Capabilities Optimizes Data Transfers for all Operating Modes:
  - One Channel for the Receiver, One Channel for the Transmitter
  - Next Buffer Support

10.17 Analog-to-Digital Converter

- 8-channel ADC
- 10-bit 384 Ksamples/sec. Successive Approximation Register ADC
- ±2 LSB Integral Non Linearity, ±1 LSB Differential Non Linearity
- Integrated 8-to-1 multiplexer, offering eight independent 3.3V analog inputs
- External voltage reference for better accuracy on low voltage inputs
- Individual enable and disable of each channel
- Multiple trigger sources
  - Hardware or software trigger
  - External trigger pin
  - Timer Counter 0 to 2 outputs TIOA0 to TIOA2 trigger
- Sleep Mode and conversion sequencer

Revision History

Table 13-1. Revision History

Doc. Rev	Comments	Change Request Ref.
6209S	First issue - Unqualified on Intranet Legal page updated.Qualified on Intranet	
6209BS	Added AT91SAM7XC512 to product family.“Features” on page 1 and global Reformatted Memories Section 8. “Memory” on page 18. Reordered sub sections in Peripherals Section 10. “Peripherals” on page 32 Consolidated Memory Mapping in Figure 8-1 on page 19. Added package drawings Section 11. “Package Drawings” on page 42. Consolidated Memory Mapping in Figure 8-1 on page 19. Added TFBGA information Section 4.3 “100-ball TFBGA Package Outline” on page 11. and Section 4.4 on page 10 and “Features” on page 1 Added LQFP and TFBGA package drawings Section 11. on page 42. System Controller block diagram Figure 9-1 on page 26, “ice_nreset” signals changed to “power_on_reset”.	2729
6209CS	“Features”, TWI updated to include Atmel TWI compatibility with I^2C Standard. “Features”, “Debug Unit (DBGU)” added “Mode for General Purpose 2-wire UART Serial Communication”. Section 10.8 ”Two-wire Interface”, updated. Section 10.11 ”Timer Counter”,The TC has Two output compare or one input capture per channel. Section 10.17 ”Analog-to-Digital Converter”,INL and DNL updated. Figure 3-1,”Signal Description List”, footnote added to JTAGSEL, ERASE and TST pin comments Section 6.1 ”JTAG Port Pins”, Section 6.2 ”Test Pin” and Section 6.4 ”ERASE Pin”updated. Figure 9-1,”System Controller Block Diagram”, RTT is reset by power_on_reset. Figure 8-1,”AT91SAM7XC512/256/128 Memory Mapping”,TDES base address is 0xFFFA 8000 Section 8.4.3 ”Internal Flash”,updated: “At any time, the Flash is mapped ... if GPNVM bit 2 is set and before the Remap Command.”	4247 5846 4211 4008 5068 5225 5257 5850
6209DS	Section 12. ”AT91SAM7XC512/256/128 Ordering Information”, MLR B chip revision added to ordering information.	6064

≤