Microchip Technology - AT91SAM7XC256B-CU-999 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	55MHz
Connectivity	CANbus, Ethernet, I²C, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	62
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 1.95V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-TFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at91sam7xc256b-cu-999

2. AT91SAM7XC512/256/128 Block Diagram

Figure 2-1. AT91SAM7XC512/256/128 Block Diagram

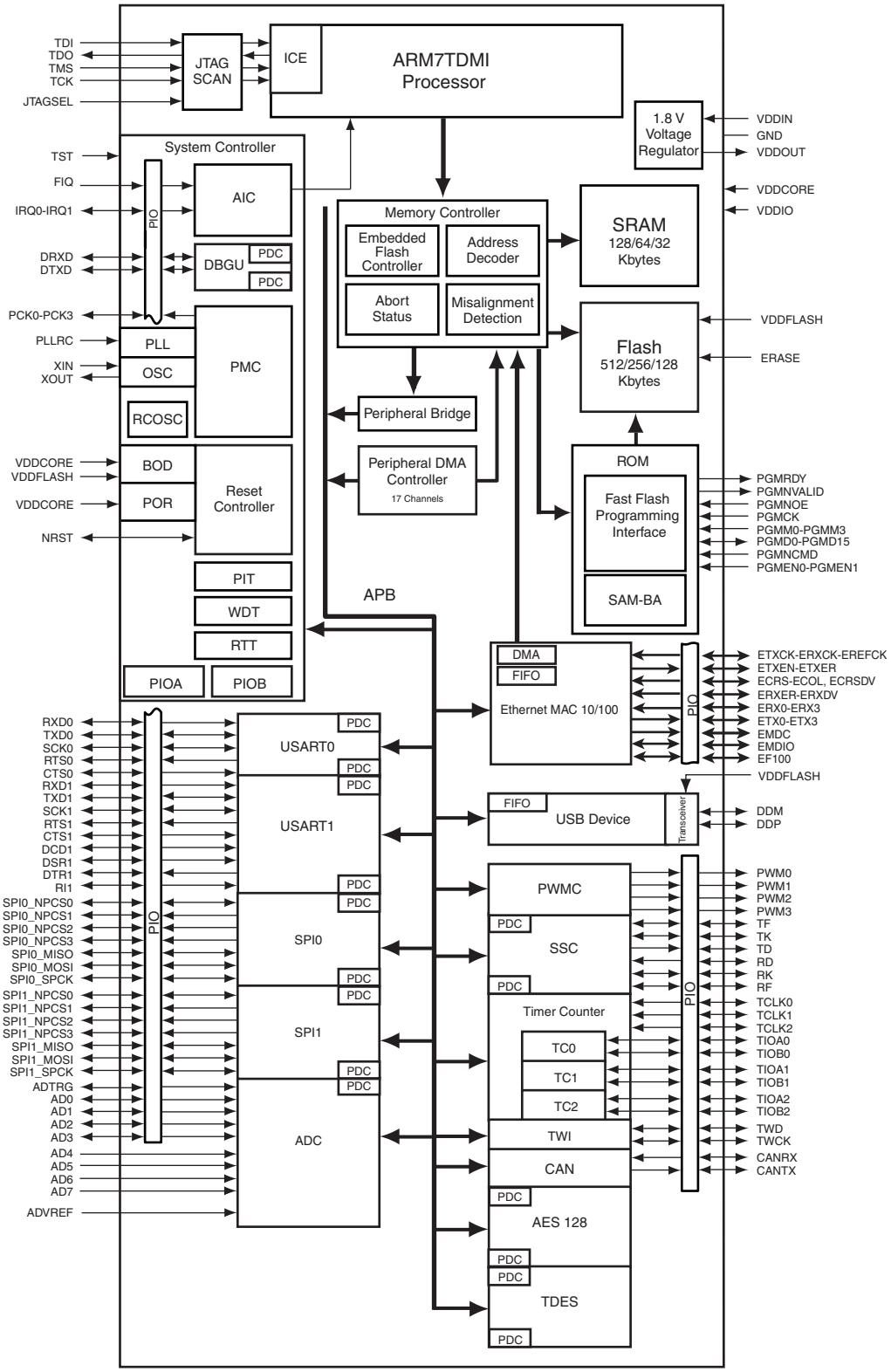


Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
Analog-to-Digital Converter				
AD0-AD3	Analog Inputs	Analog		Digital pulled-up inputs at reset.
AD4-AD7	Analog Inputs	Analog		Analog Inputs
ADTRG	ADC Trigger	Input		
ADVREF	ADC Reference	Analog		
Fast Flash Programming Interface				
PGMEN0-PGMEN1	Programming Enabling	Input		
PGMM0-PGMM3	Programming Mode	Input		
PGMD0-PGMD15	Programming Data	I/O		
PGMRDY	Programming Ready	Output	High	
PGMNVALID	Data Direction	Output	Low	
PGMNOE	Programming Read	Input	Low	
PGMCK	Programming Clock	Input		
PGMNCMD	Programming Command	Input	Low	
CAN Controller				
CANRX	CAN Input	Input		
CANTX	CAN Output	Output		
Ethernet MAC 10/100				
EREFCK	Reference Clock	Input		RMII only
ETXCK	Transmit Clock	Input		MII only
ERXCK	Receive Clock	Input		MII only
ETXEN	Transmit Enable	Output		
ETX0 - ETX3	Transmit Data	Output		ETX0 - ETX1 only in RMII
ETXER	Transmit Coding Error	Output		MII only
ERXDV	Receive Data Valid	Input		MII only
ECRSDV	Carrier Sense and Data Valid	Input		RMII only
ERX0 - ERX3	Receive Data	Input		ERX0 - ERX1 only in RMII
ERXER	Receive Error	Input		
ECRS	Carrier Sense	Input		MII only
ECOL	Collision Detected	Input		MII only
EMDC	Management Data Clock	Output		
EMDIO	Management Data Input/Output	I/O		
EF100	Force 100 Mbits/sec.	Output	High	RMII only

Note: 1. Refer to Section 6. "I/O Lines Considerations".

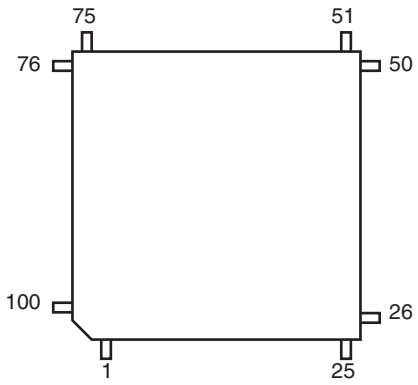
4. Package

The AT91SAM7XC512/256/128 is available in 100-lead LQFP Green and 100-ball TFBGA RoHS-compliant packages.

4.1 100-lead LQFP Package Outline

Figure 4-1 shows the orientation of the 100-lead LQFP package. A detailed mechanical description is given in the Mechanical Characteristics section of the full datasheet.

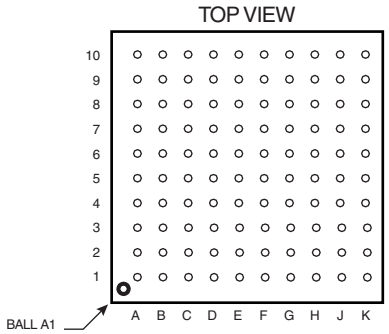
Figure 4-1. 100-lead LQFP Package Outline (Top View)



4.3 100-ball TFBGA Package Outline

Figure 4-2 shows the orientation of the 100-ball TFBGA package. A detailed mechanical description is given in the Mechanical Characteristics section of the full datasheet.

Figure 4-2. 100-ball TFBGA Package Orientation (Top View)



4.4 100-ball TFBGA Pinout

Table 4-2. Pinout in 100-ball TFBGA Package

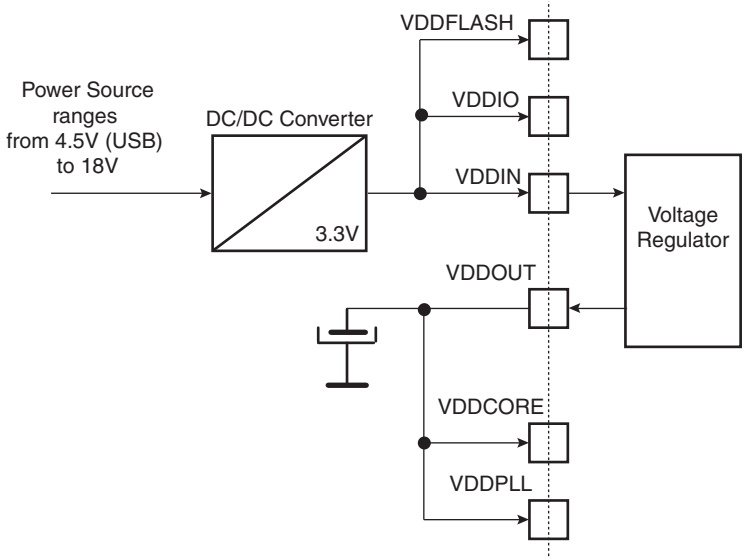
Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	PA22/PGMD10	C6	PB17	F1	PB21	H6	PA7/PGMNVALID
A2	PA21/PGMD9	C7	PB13	F2	PB23	H7	PA9/PGMM1
A3	PA20/PGMD8	C8	PA13/PGMD1	F3	PB25	H8	PA8/PGMM0
A4	PB1	C9	PA12/PGMD0	F4	PB26	H9	PB29/AD2
A5	PB7	C10	PA15/PGMD3	F5	TCK	H10	PLLRC
A6	PB5	D1	PA23/PGMD11	F6	PA6/PGMNOE	J1	PA29
A7	PB8	D2	PA24/PGMD12	F7	ERASE	J2	PA30
A8	PB9	D3	NRST	F8	VDDCORE	J3	PA0/PGMEN0
A9	PA18/PGMD6	D4	TST	F9	GND	J4	PA1/PGMEN1
A10	VDDIO	D5	PB19	F10	VDDIN	J5	VDDFLASH
B1	TDI	D6	PB6	G1	PB22	J6	GND
B2	PA19/PGMD7	D7	PA10/PGMM2	G2	PB24	J7	XIN/PGMCK
B3	PB11	D8	VDDIO	G3	PA27/PGMD15	J8	XOUT
B4	PB2	D9	PB27/AD0	G4	TDO	J9	GND
B5	PB12	D10	PA11/PGMM3	G5	PA2	J10	VDDPLL
B6	PB15	E1	PA25/PGMD13	G6	PA5/PGMRDY	K1	VDDCORE
B7	PB14	E2	PA26/PGMD14	G7	VDDCORE	K2	VDDCORE
B8	PA14/PGMD2	E3	PB18	G8	GND	K3	DDP
B9	PA16/PGMD4	E4	PB20	G9	PB30/AD3	K4	DDM
B10	PA17/PGMD5	E5	TMS	G10	VDDOUT	K5	GND
C1	PB16	E6	GND	H1	VDDCORE	K6	AD7
C2	PB4	E7	VDDIO	H2	PA28	K7	AD6
C3	PB10	E8	PB28/AD1	H3	JTAGSEL	K8	AD5
C4	PB3	E9	VDDIO	H4	PA3	K9	AD4
C5	PB0	E10	GND	H5	PA4/PGMNCMD	K10	ADVREF

Adequate input supply decoupling is mandatory for VDDIN in order to improve startup stability and reduce source voltage drop. The input decoupling capacitor should be placed close to the chip. For example, two capacitors can be used in parallel: 100 nF NPO and 4.7 µF X7R.

5.4 Typical Powering Schematics

The AT91SAM7XC512/256/128 supports a 3.3V single supply mode. The internal regulator input connected to the 3.3V source and its output feeds VDDCORE and the VDDPLL. Figure 5-1 shows the power schematics to be used for USB bus-powered systems.

Figure 5-1. 3.3V System Single Power Supply Schematic



5V-tolerant means that the I/O lines can drive voltage level according to VDDIO, but can be driven with a voltage of up to 5.5V. However, driving an I/O line with a voltage over VDDIO while the programmable pull-up resistor is enabled will create a current path through the pull-up resistor from the I/O line to VDDIO. Care should be taken, in particular at reset, as all the I/O lines default to input with pull-up resistor enabled at reset.

6.6 I/O Lines Current Drawing

The PIO lines PA0 to PA3 are high-drive current capable. Each of these I/O lines can drive up to 16 mA permanently.

The remaining I/O lines can draw only 8 mA.

However, the total current drawn by all the I/O lines cannot exceed 200 mA.

7. Processor and Architecture

7.1 ARM7TDMI Processor

- RISC processor based on ARMv4T Von Neumann architecture
  - Runs at up to 55 MHz, providing 0.9 MIPS/MHz
- Two instruction sets
  - ARM® high-performance 32-bit instruction set
  - Thumb® high code density 16-bit instruction set
- Three-stage pipeline architecture
  - Instruction Fetch (F)
  - Instruction Decode (D)
  - Execute (E)

7.2 Debug and Test Features

- Integrated embedded in-circuit emulator
  - Two watchpoint units
  - Test access port accessible through a JTAG protocol
  - Debug communication channel
- Debug Unit
  - Two-pin UART
  - Debug communication channel interrupt handling
  - Chip ID Register
- IEEE1149.1 JTAG Boundary-scan on all digital pins

7.3 Memory Controller

- Programmable Bus Arbiter
  - Handles requests from the ARM7TDMI, the Ethernet MAC and the Peripheral DMA Controller
- Address decoder provides selection signals for
  - Three internal 1 Mbyte memory areas
  - One 256 Mbyte embedded peripheral area
- Abort Status Registers
  - Source, Type and all parameters of the access leading to an abort are saved
  - Facilitates debug by detection of bad pointers
- Misalignment Detector
  - Alignment checking of all data accesses
  - Abort generation in case of misalignment
- Remap Command
  - Remaps the SRAM in place of the embedded non-volatile memory
  - Allows handling of dynamic exception vectors

Figure 8-1. AT91SAM7XC512/256/128 Memory Mapping

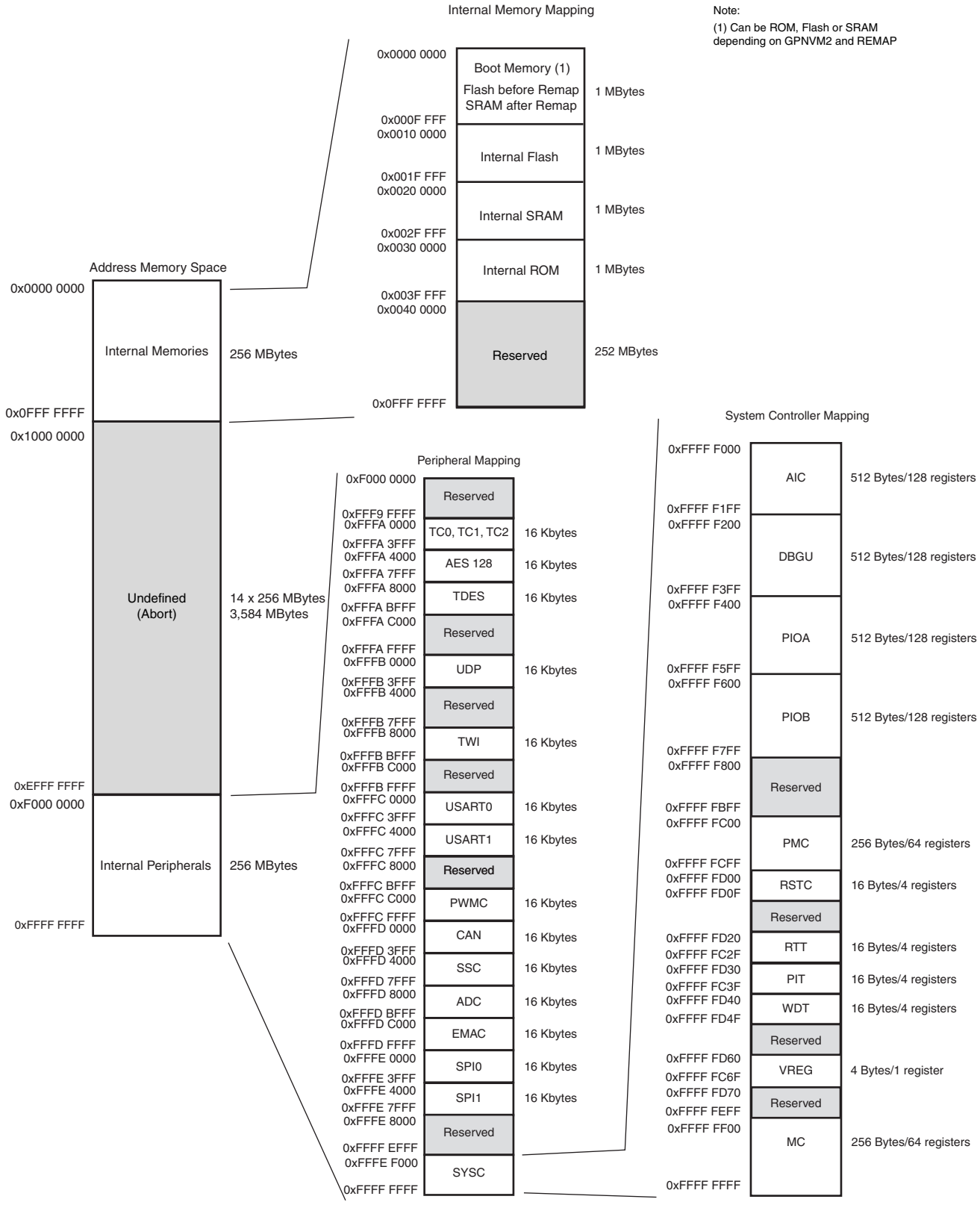
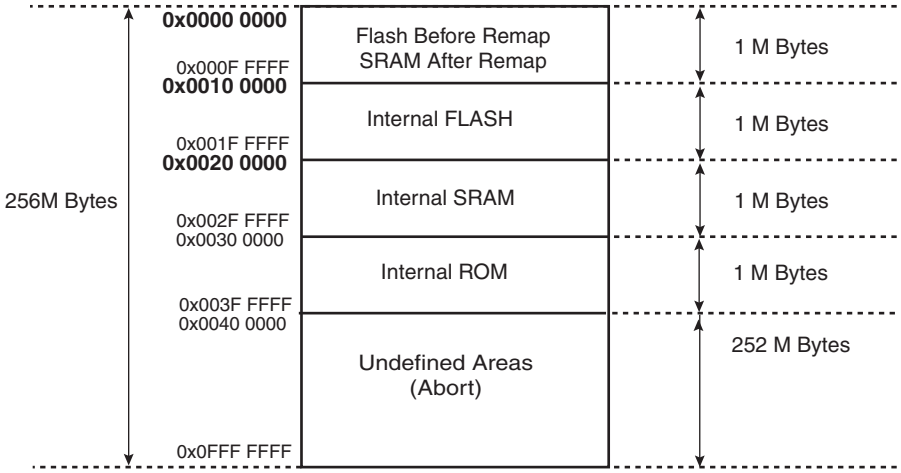


Figure 8-3. Internal Memory Mapping with GPNVM Bit 2 = 1



8.5 Embedded Flash

8.5.1 Flash Overview

- The Flash of the AT91SAM7XC512 is organized in two banks (dual plane) 0f 1254 pages of 256 bytes. The 524, 288 bytes are organized in 32-bit words.
- The Flash of the AT91SAM7XC256 is organized in 1024 pages of 256 bytes (single plane). It reads as 65,536 32-bit words.
- The Flash of the AT91SAM7XC128 is organized in 512 pages of 256 bytes (single plane). It reads as 32,768 32-bit words.

The Flash contains a 256-byte write buffer, accessible through a 32-bit interface.

The Flash benefits from the integration of a power reset cell and from the brownout detector. This prevents code corruption during power supply changes, even in the worst conditions.

When Flash is not used (read or write access), it is automatically placed into standby mode.

8.5.2 Embedded Flash Controller

The Embedded Flash Controller (EFC) manages accesses performed by the masters of the system. It enables reading the Flash and writing the write buffer. It also contains a User Interface, mapped within the Memory Controller on the APB. The User Interface allows:

- programming of the access parameters of the Flash (number of wait states, timings, etc.)
- starting commands such as full erase, page erase, page program, NVM bit set, NVM bit clear, etc.
- getting the end status of the last command
- getting error status
- programming interrupts on the end of the last commands or on errors

The Embedded Flash Controller also provides a dual 32-bit Prefetch Buffer that optimizes 16-bit access to the Flash. This is particularly efficient when the processor is running in Thumb mode.

Two EFCs are embedded in the AT91SAM7XC512 to control each bank of 256 KBytes. Dual-plane organization allows concurrent read and program functionality. Read from one memory

plane may be performed even while program or erase functions are being executed in the other memory plane.

One EFC is embedded in the AT91SAM7XC256/128 to control the single plane of 256/128 KBytes.

8.5.3 Lock Regions

8.5.3.1 AT91SAM7XC512

Two Embedded Flash Controllers each manage 16 lock bits to protect 16 regions of the flash against inadvertent flash erasing or programming commands. The AT91SAM7XC512 contains 32 lock regions and each lock region contains 64 pages of 256 bytes. Each lock region has a size of 16 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the EFC trigs an interrupt.

The 32 NVM bits are software programmable through both of the EFC User Interfaces. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

8.5.3.2 AT91SAM7XC256

The Embedded Flash Controller manages 16 lock bits to protect 16 regions of the flash against inadvertent flash erasing or programming commands. The AT91SAM7XC256 contains 16 lock regions and each lock region contains 64 pages of 256 bytes. Each lock region has a size of 16 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the EFC trigs an interrupt.

The 16 NVM bits are software programmable through the EFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

8.5.3.3 AT91SAM7XC128

The Embedded Flash Controller manages 8 lock bits to protect 8 regions of the flash against inadvertent flash erasing or programming commands. The AT91SAM7XC128 contains 8 lock regions and each lock region contains 64 pages of 256 bytes. Each lock region has a size of 16 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the EFC trigs an interrupt.

The 8 NVM bits are software programmable through the EFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

8.5.4 Security Bit Feature

The AT91SAM7XC512/256/128 features a security bit, based on a specific NVM-Bit. When the security is enabled, any access to the Flash, either through the ICE interface or through the Fast

Flash Programming Interface, is forbidden. This ensures the confidentiality of the code programmed in the Flash.

This security bit can only be enabled, through the Command “Set Security Bit” of the EFC User Interface. Disabling the security bit can only be achieved by asserting the ERASE pin at 1, and after a full flash erase is performed. When the security bit is deactivated, all accesses to the flash are permitted.

It is important to note that the assertion of the ERASE pin should always be longer than 220 ms.

As the ERASE pin integrates a permanent pull-down, it can be left unconnected during normal operation. However, it is safer to connect it directly to GND for the final application.

8.5.5 Non-volatile Brownout Detector Control

Two general purpose NVM (GPNVM) bits are used for controlling the brownout detector (BOD), so that even after a power loss, the brownout detector operations remain in their state.

These two GPNVM bits can be cleared or set respectively through the commands “Clear General-purpose NVM Bit” and “Set General-purpose NVM Bit” of the EFC User Interface.

- GPNVM Bit 0 is used as a brownout detector enable bit. Setting the GPNVM Bit 0 enables the BOD, clearing it disables the BOD. Asserting ERASE clears the GPNVM Bit 0 and thus disables the brownout detector by default.
- The GPNVM Bit 1 is used as a brownout reset enable signal for the reset controller. Setting the GPNVM Bit 1 enables the brownout reset when a brownout is detected, Clearing the GPNVM Bit 1 disables the brownout reset. Asserting ERASE disables the brownout reset by default.

8.5.6 Calibration Bits

Eight NVM bits are used to calibrate the brownout detector and the voltage regulator. These bits are factory configured and cannot be changed by the user. The ERASE pin has no effect on the calibration bits.

8.6 Fast Flash Programming Interface

The Fast Flash Programming Interface allows programming the device through either a serial JTAG interface or through a multiplexed fully-handshaked parallel port. It allows gang-programming with market-standard industrial programmers.

The FFPI supports read, page program, page erase, full erase, lock, unlock and protect commands.

The Fast Flash Programming Interface is enabled and the Fast Programming Mode is entered when the TST pin and the PA0 and PA1 pins are all tied high.

8.7 SAM-BA Boot Assistant

The SAM-BA Boot Assistant is a default Boot Program that provides an easy way to program in-situ the on-chip Flash memory.

The SAM-BA Boot Assistant supports serial communication via the DBGU or the USB Device Port.

- Communication via the DBGU supports a wide range of crystals from 3 to 20 MHz via software auto-detection.

9. System Controller

The System Controller manages all vital blocks of the microcontroller: interrupts, clocks, power, time, debug and reset.

The System Controller peripherals are all mapped to the highest 4 Kbytes of address space, between addresses 0xFFFF F000 and 0xFFFF FFFF.

Figure 9-1 on page 26 shows the System Controller Block Diagram.

Figure 8-1 on page 19 shows the mapping of the User Interface of the System Controller peripherals. Note that the Memory Controller configuration user interface is also mapped within this address space.

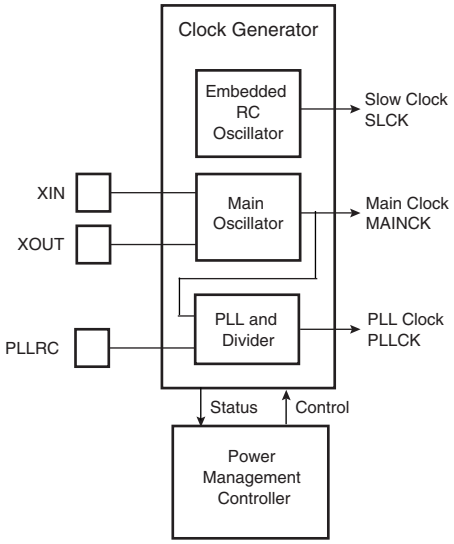
9.2 Clock Generator

The Clock Generator embeds one low-power RC Oscillator, one Main Oscillator and one PLL with the following characteristics:

- RC Oscillator ranges between 22 KHz and 42 KHz
- Main Oscillator frequency ranges between 3 and 20 MHz
- Main Oscillator can be bypassed
- PLL output ranges between 80 and 200 MHz

It provides SLCK, MAINCK and PLLCK.

Figure 9-2. Clock Generator Block Diagram



  - Higher priority interrupts can be served during service of lower priority interrupt
- Vectoring
  - Optimizes interrupt service routine branch and execution
  - One 32-bit vector register per interrupt source
  - Interrupt vector register reads the corresponding current interrupt vector
- Protect Mode
  - Easy debugging by preventing automatic operations
- Fast Forcing
  - Permits redirecting any interrupt source on the fast interrupt
- General Interrupt Mask
  - Provides processor synchronization on events without triggering an interrupt

9.5 Debug Unit

- Comprises:
  - One two-pin UART
  - One Interface for the Debug Communication Channel (DCC) support
  - One set of Chip ID Registers
  - One Interface providing ICE Access Prevention
- Two-pin UART
  - USART-compatible User Interface
  - Programmable Baud Rate Generator
  - Parity, Framing and Overrun Error
  - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
- Debug Communication Channel Support
  - Offers visibility of COMMRX and COMMTX signals from the ARM Processor
- Chip ID Registers
  - Identification of the device revision, sizes of the embedded memories, set of peripherals
  - Chip ID is 0x271C 0A40 (VERSION 0) for AT91SAM7XC512
  - Chip ID is 0x271B 0940 (VERSION 0) for AT91SAM7XC256
  - Chip ID is 0x271A 0740 (VERSION 0) for AT91SAM7XC128

9.6 Periodic Interval Timer

- 20-bit programmable counter plus 12-bit interval counter

9.7 Watchdog Timer

- 12-bit key-protected Programmable Counter running on prescaled SLCK
- Provides reset or interrupt signals to the system
- Counter may be stopped while the processor is in debug state or in idle mode

9.8 Real-time Timer

- 32-bit free-running counter with alarm running on prescaled SLCK

10. Peripherals

10.1 User Interface

The User Peripherals are mapped in the 256 MBytes of address space between 0xF000 0000 and 0xFFFE FFFF. Each peripheral is allocated 16 Kbytes of address space.

A complete memory map is provided in Figure 8-1 on page 19.

10.2 Peripheral Identifiers

The AT91SAM7XC512/256/128 embeds a wide range of peripherals. Table 10-1 defines the Peripheral Identifiers of the AT91SAM7XC512/256/128. Unique peripheral identifiers are defined for both the Advanced Interrupt Controller and the Power Management Controller.

Table 10-1. Peripheral Identifiers

Peripheral ID	Peripheral Mnemonic	Peripheral Name	External Interrupt
0	AIC	Advanced Interrupt Controller	FIQ
1	SYSC(1)	System	
2	PIOA	Parallel I/O Controller A	
3	PIOB	Parallel I/O Controller B	
4	SPI0	Serial Peripheral Interface 0	
5	SPI1	Serial Peripheral Interface 1	
6	US0	USART 0	
7	US1	USART 1	
8	SSC	Synchronous Serial Controller	
9	TWI	Two-wire Interface	
10	PWMC	Pulse Width Modulation Controller	
11	UDP	USB device Port	
12	TC0	Timer/Counter 0	
13	TC1	Timer/Counter 1	
14	TC2	Timer/Counter 2	
15	CAN	CAN Controller	
16	EMAC	Ethernet MAC	
17	ADC(1)	Analog-to Digital Converter	
18	AES	Advanced Encryption Standard 128-bit	
19	TDES	Triple Data Encryption Standard	
20-29	Reserved		
30	AIC	Advanced Interrupt Controller	IRQ0
31	AIC	Advanced Interrupt Controller	IRQ1

Note: 1. Setting SYSC and ADC bits in the clock set/clear registers of the PMC has no effect. The System Controller and ADC are continuously clocked.

10.4 PIO Controller A Multiplexing

Table 10-2. Multiplexing on PIO Controller A

PIO Controller A				Application Usage	
I/O Line	Peripheral A	Peripheral B	Comments	Function	Comments
PA0	RXD0		High-Drive		
PA1	TXD0		High-Drive		
PA2	SCK0	SPI1_NPCS1	High-Drive		
PA3	RTS0	SPI1_NPCS2	High-Drive		
PA4	CTS0	SPI1_NPCS3			
PA5	RXD1				
PA6	TXD1				
PA7	SCK1	SPI0_NPCS1			
PA8	RTS1	SPI0_NPCS2			
PA9	CTS1	SPI0_NPCS3			
PA10	TWD				
PA11	TWCK				
PA12	SPI_NPCS0				
PA13	SPI0_NPCS1	PCK1			
PA14	SPI0_NPCS2	IRQ1			
PA15	SPI0_NPCS3	TCLK2			
PA16	SPI0_MISO				
PA17	SPI0_MOSI				
PA18	SPI0_SPCK				
PA19	CANRX				
PA20	CANTX				
PA21	TF	SPI1_NPCS0			
PA22	TK	SPI1_SPCK			
PA23	TD	SPI1_MOSI			
PA24	RD	SPI1_MISO			
PA25	RK	SPI1_NPCS1			
PA26	RF	SPI1_NPCS2			
PA27	DRXD	PCK3			
PA28	DTXD				
PA29	FIQ	SPI1_NPCS3			
PA30	IRQ0	PCK2			

10.8 Two-wire Interface

- Master Mode only
- Compatibility with I^2C compatible devices (refer to the TWI section of the datasheet)
- One, two or three bytes internal address registers for easy Serial Memory access
- 7-bit or 10-bit slave addressing
- Sequential read/write operations

10.9 USART

- Programmable Baud Rate Generator
- 5- to 9-bit full-duplex synchronous or asynchronous serial communications
  - 1, 1.5 or 2 stop bits in Asynchronous Mode
  - 1 or 2 stop bits in Synchronous Mode
  - Parity generation and error detection
  - Framing error detection, overrun error detection
  - MSB or LSB first
  - Optional break generation and detection
  - By 8 or by 16 over-sampling receiver frequency
  - Hardware handshaking RTS - CTS
  - Modem Signals Management DTR-DSR-DCD-RI on USART1
  - Receiver time-out and transmitter timeguard
  - Multi-drop Mode with address generation and detection
- RS485 with driver control signal
- ISO7816, T = 0 or T = 1 Protocols for interfacing with smart cards
  - NACK handling, error counter with repetition and iteration limit
- IrDA modulation and demodulation
  - Communication at up to 115.2 Kbps
- Test Modes
  - Remote Loopback, Local Loopback, Automatic Echo

10.10 Serial Synchronous Controller

- Provides serial synchronous communication links used in audio and telecom applications
- Contains an independent receiver and transmitter and a common clock divider
- Offers a configurable frame sync and data length
- Receiver and transmitter can be programmed to start automatically or on detection of different event on the frame sync signal
- Receiver and transmitter include a data signal, a clock signal and a frame synchronization signal

11. Package Drawings

Figure 11-1. LQFP Package Drawing

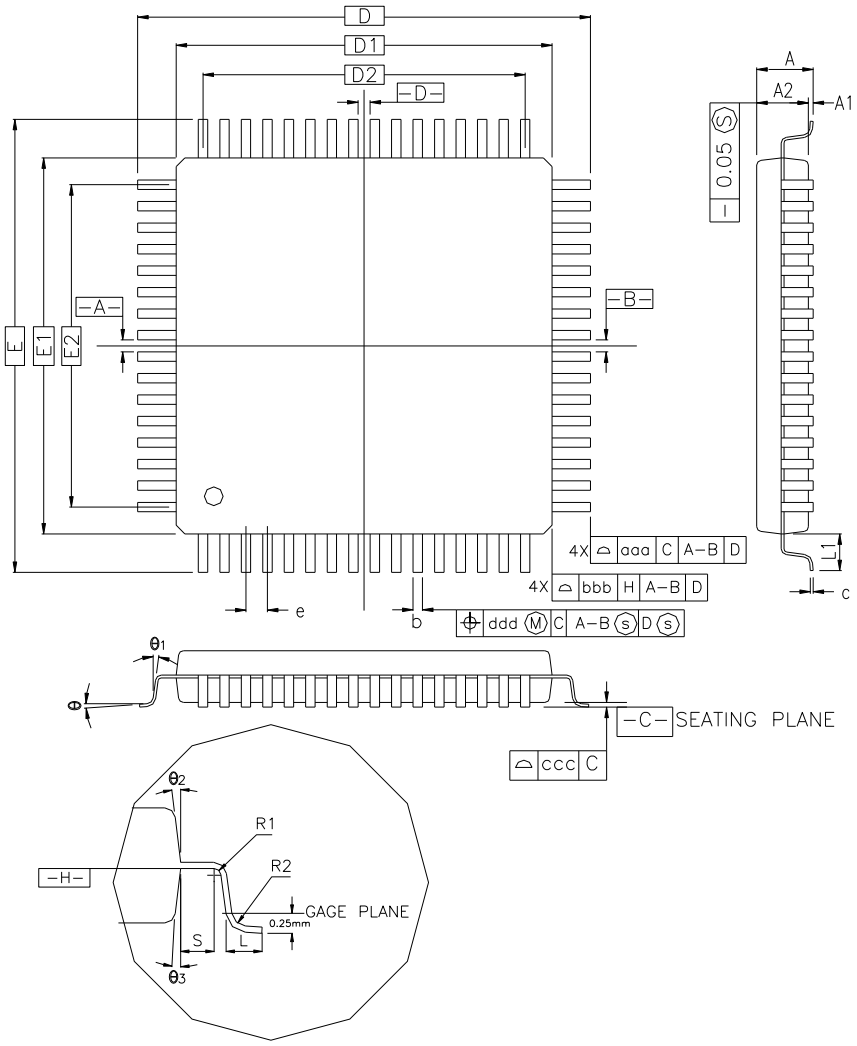


Table 11-1. 100-lead LQFP Package Dimensions

Symbol	Millimeter			Inch		
	Min	Nom	Max	Min	Nom	Max
A			1.60			0.63
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D		16.00 BSC			0.630 BSC	
D1		14.00 BSC			0.551 BSC	
E		16.00 BSC			0.630 BSC	
E1		14.00 BSC			0.551 BSC	
R2	0.08		0.20	0.003		0.008
R1	0.08			0.003		
Q	0·	3.5·	7·	0·	3.5·	7·
θ1	0·			0·		
θ2	11·	12·	13·	11·	12·	13·
θ3	11·	12·	13·	11·	12·	13·
c	0.09		0.20	0.004		0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00 REF			0.039 REF	
S	0.20			0.008		
b	0.17	0.20	0.27	0.007	0.008	0.011
e		0.50 BSC			0.020 BSC	
D2		12.00			0.472	
E2		12.00			0.472	
Tolerances of Form and Position						
aaa		0.20			0.008	
bbb		0.20			0.008	
ccc		0.08			0.003	
ddd		0.08			0.003	

Revision History

Table 13-1. Revision History

Doc. Rev	Comments	Change Request Ref.
6209S	First issue - Unqualified on Intranet Legal page updated.Qualified on Intranet	
6209BS	Added AT91SAM7XC512 to product family.“Features” on page 1 and global Reformatted Memories Section 8. “Memory” on page 18. Reordered sub sections in Peripherals Section 10. “Peripherals” on page 32 Consolidated Memory Mapping in Figure 8-1 on page 19. Added package drawings Section 11. “Package Drawings” on page 42. Consolidated Memory Mapping in Figure 8-1 on page 19. Added TFBGA information Section 4.3 “100-ball TFBGA Package Outline” on page 11. and Section 4.4 on page 10 and “Features” on page 1 Added LQFP and TFBGA package drawings Section 11. on page 42. System Controller block diagram Figure 9-1 on page 26, “ice_nreset” signals changed to “power_on_reset”.	2729
6209CS	“Features”, TWI updated to include Atmel TWI compatibility with I^2C Standard. “Features”, “Debug Unit (DBGU)” added “Mode for General Purpose 2-wire UART Serial Communication”. Section 10.8 ”Two-wire Interface”, updated. Section 10.11 ”Timer Counter”,The TC has Two output compare or one input capture per channel. Section 10.17 ”Analog-to-Digital Converter”,INL and DNL updated. Figure 3-1,”Signal Description List”, footnote added to JTAGSEL, ERASE and TST pin comments Section 6.1 ”JTAG Port Pins”, Section 6.2 ”Test Pin” and Section 6.4 ”ERASE Pin”updated. Figure 9-1,”System Controller Block Diagram”, RTT is reset by power_on_reset. Figure 8-1,”AT91SAM7XC512/256/128 Memory Mapping”,TDES base address is 0xFFFA 8000 Section 8.4.3 ”Internal Flash”,updated: “At any time, the Flash is mapped ... if GPNVM bit 2 is set and before the Remap Command.”	4247 5846 4211 4008 5068 5225 5257 5850
6209DS	Section 12. ”AT91SAM7XC512/256/128 Ordering Information”, MLR B chip revision added to ordering information.	6064

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