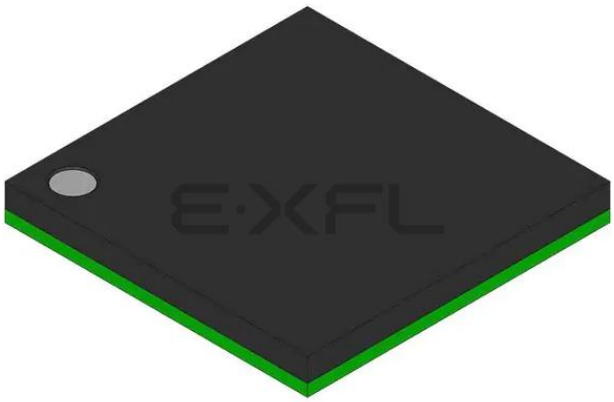

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	55MHz
Connectivity	CANbus, Ethernet, I²C, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	62
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 1.95V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-TFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/atmel/at91sam7xc256b-cu

- **Fully Static Operation: Up to 55 MHz at 1.65V and 85· C Worst Case Conditions**
- **Available in 100-lead LQFP Green and 100-ball TFBGA Green Packages**

3. Signal Description

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
Power				
VDDIN	Voltage Regulator and ADC Power Supply Input	Power		3V to 3.6V
VDDOUT	Voltage Regulator Output	Power		1.85V
VDDFLASH	Flash and USB Power Supply	Power		3V to 3.6V
VDDIO	I/O Lines Power Supply	Power		3V to 3.6V
VDDCORE	Core Power Supply	Power		1.65V to 1.95V
VDDPLL	PLL	Power		1.65V to 1.95V
GND	Ground	Ground		
Clocks, Oscillators and PLLs				
XIN	Main Oscillator Input	Input		
XOUT	Main Oscillator Output	Output		
PLLRC	PLL Filter	Input		
PCK0 - PCK3	Programmable Clock Output	Output		
ICE and JTAG				
TCK	Test Clock	Input		No pull-up resistor
TDI	Test Data In	Input		No pull-up resistor
TDO	Test Data Out	Output		
TMS	Test Mode Select	Input		No pull-up resistor
JTAGSEL	JTAG Selection	Input		Pull-down resistor(1)
Flash Memory				
ERASE	Flash and NVM Configuration Bits Erase Command	Input	High	Pull-down resistor(1)
Reset/Test				
NRST	Microcontroller Reset	I/O	Low	Pull-Up resistor, Open Drain Output.
TST	Test Mode Select	Input	High	Pull-down resistor(1)
Debug Unit				
DRXD	Debug Receive Data	Input		
DTXD	Debug Transmit Data	Output		
AIC				
IRQ0 - IRQ1	External Interrupt Inputs	Input		
FIQ	Fast Interrupt Input	Input		
PIO				
PA0 - PA30	Parallel IO Controller A	I/O		Pulled-up input at reset.
PB0 - PB30	Parallel IO Controller B	I/O		Pulled-up input at reset.

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
USB Device Port				
DDM	USB Device Port Data -	Analog		
DDP	USB Device Port Data +	Analog		
USART				
SCK0 - SCK1	Serial Clock	I/O		
TXD0 - TXD1	Transmit Data	I/O		
RXD0 - RXD1	Receive Data	Input		
RTS0 - RTS1	Request To Send	Output		
CTS0 - CTS1	Clear To Send	Input		
DCD1	Data Carrier Detect	Input		
DTR1	Data Terminal Ready	Output		
DSR1	Data Set Ready	Input		
RI1	Ring Indicator	Input		
Synchronous Serial Controller				
TD	Transmit Data	Output		
RD	Receive Data	Input		
TK	Transmit Clock	I/O		
RK	Receive Clock	I/O		
TF	Transmit Frame Sync	I/O		
RF	Receive Frame Sync	I/O		
Timer/Counter				
TCLK0 - TCLK2	External Clock Inputs	Input		
TIOA0 - TIOA2	I/O Line A	I/O		
TIOB0 - TIOB2	I/O Line B	I/O		
PWM Controller				
PWM0 - PWM3	PWM Channels	Output		
Serial Peripheral Interface - SPIx				
SPIx_MISO	Master In Slave Out	I/O		
SPIx_MOSI	Master Out Slave In	I/O		
SPIx_SPCK	SPI Serial Clock	I/O		
SPIx_NPCS0	SPI Peripheral Chip Select 0	I/O	Low	
SPIx_NPCS1-NPCS3	SPI Peripheral Chip Select 1 to 3	Output	Low	
Two-wire Interface				
TWD	Two-wire Serial Data	I/O		
TWCK	Two-wire Serial Clock	I/O		

6. I/O Lines Considerations

6.1 JTAG Port Pins

TMS, TDI and TCK are schmitt trigger inputs and are not 5-V tolerant. TMS, TDI and TCK do not integrate a pull-up resistor.

TDO is an output, driven at up to VDDIO, and has no pull-up resistor.

The JTAGSEL pin is used to select the JTAG boundary scan when asserted at a high level. The JTAGSEL pin integrates a permanent pull-down resistor of about 15 kΩ.

To eliminate any risk of spuriously entering the JTAG boundary scan mode due to noise on JTAGSEL, it should be tied externally to GND if boundary scan is not used, or pulled down with an external low-value resistor (such as 1 kΩ).

6.2 Test Pin

The TST pin is used for manufacturing test or fast programming mode of the AT91SAM7XC512/256/128 when asserted high. The TST pin integrates a permanent pull-down resistor of about 15 kΩ to GND.

To eliminate any risk of entering the test mode due to noise on the TST pin, it should be tied to GND if the FFPI is not used, or pulled down with an external low-value resistor (such as 1 kΩ).

To enter fast programming mode, the TST pin and the PA0 and PA1 pins should be tied high and PA2 tied to low.

Driving the TST pin at a high level while PA0 or PA1 is driven at 0 leads to unpredictable results.

6.3 Reset Pin

The NRST pin is bidirectional with an open drain output buffer. It is handled by the on-chip reset controller and can be driven low to provide a reset signal to the external components or asserted low externally to reset the microcontroller. There is no constraint on the length of the reset pulse, and the reset controller can guarantee a minimum pulse length. This allows connection of a simple push-button on the NRST pin as system user reset, and the use of the signal NRST to reset all the components of the system.

The NRST pin integrates a permanent pull-up resistor to VDDIO.

6.4 ERASE Pin

The ERASE pin is used to re-initialize the Flash content and some of its NVM bits. It integrates a permanent pull-down resistor of about 15 kΩ to GND.

To eliminate any risk of erasing the Flash due to noise on the ERASE pin, it shoul be tied externally to GND, which prevents erasing the Flash from the applicatiion, or pulled down with an external low-value resistor (such as 1 kΩ).

This pin is debounced by the RC oscillator to improve the glitch tolerance. Minimum debouncing time is 200 ms.

6.5 PIO Controller Lines

All the I/O lines, PA0 to PA30 and PB0 to PB30, are 5V-tolerant and all integrate a programmable pull-up resistor. Programming of this pull-up resistor is performed independently for each I/O line through the PIO controllers.

7. Processor and Architecture

7.1 ARM7TDMI Processor

- RISC processor based on ARMv4T Von Neumann architecture
  - Runs at up to 55 MHz, providing 0.9 MIPS/MHz
- Two instruction sets
  - ARM® high-performance 32-bit instruction set
  - Thumb® high code density 16-bit instruction set
- Three-stage pipeline architecture
  - Instruction Fetch (F)
  - Instruction Decode (D)
  - Execute (E)

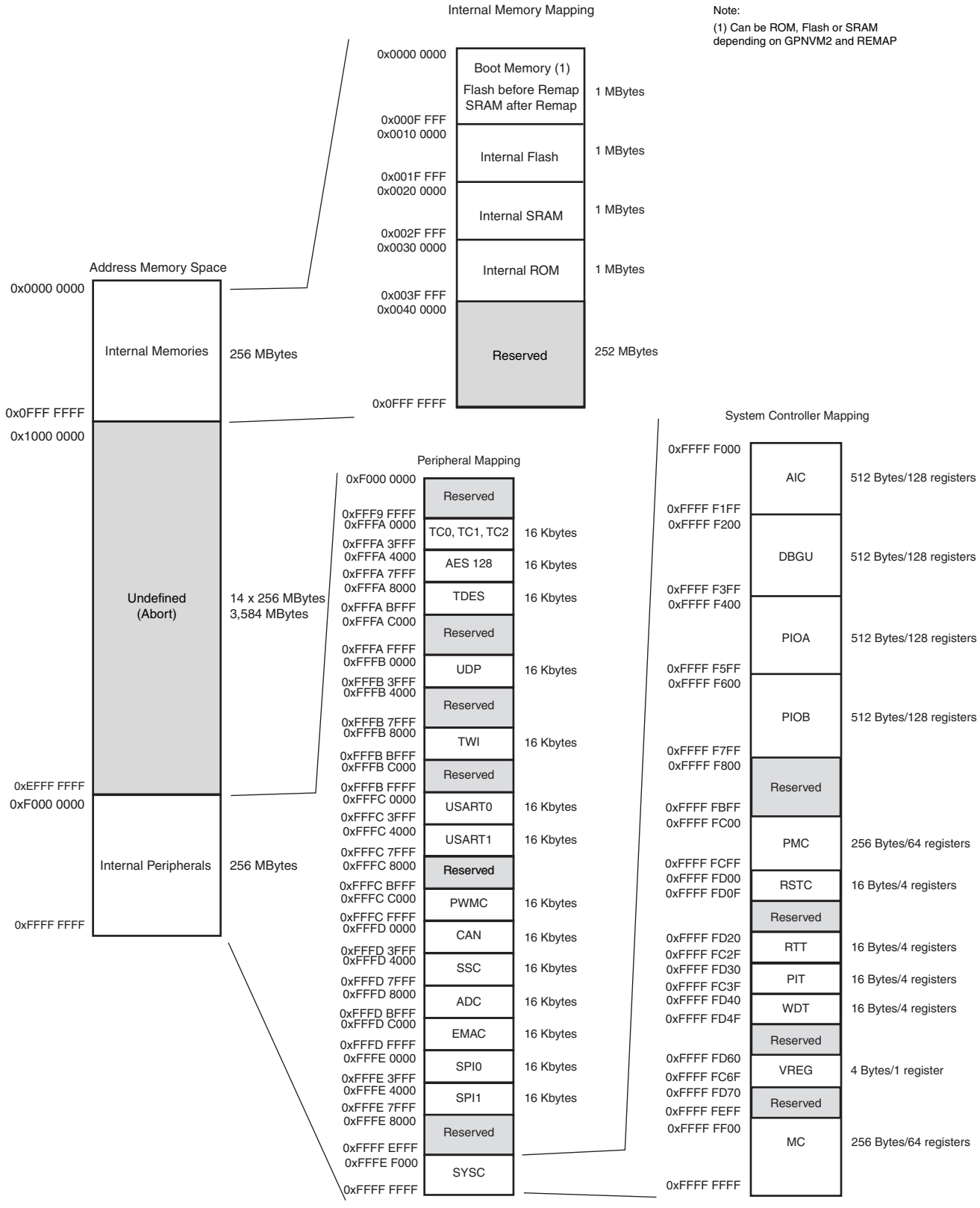
7.2 Debug and Test Features

- Integrated embedded in-circuit emulator
  - Two watchpoint units
  - Test access port accessible through a JTAG protocol
  - Debug communication channel
- Debug Unit
  - Two-pin UART
  - Debug communication channel interrupt handling
  - Chip ID Register
- IEEE1149.1 JTAG Boundary-scan on all digital pins

7.3 Memory Controller

- Programmable Bus Arbiter
  - Handles requests from the ARM7TDMI, the Ethernet MAC and the Peripheral DMA Controller
- Address decoder provides selection signals for
  - Three internal 1 Mbyte memory areas
  - One 256 Mbyte embedded peripheral area
- Abort Status Registers
  - Source, Type and all parameters of the access leading to an abort are saved
  - Facilitates debug by detection of bad pointers
- Misalignment Detector
  - Alignment checking of all data accesses
  - Abort generation in case of misalignment
- Remap Command
  - Remaps the SRAM in place of the embedded non-volatile memory
  - Allows handling of dynamic exception vectors

Figure 8-1. AT91SAM7XC512/256/128 Memory Mapping



8.4 Memory Mapping

8.4.1 Internal RAM

- The AT91SAM7XC512 embeds a high-speed 128-Kbyte SRAM bank.
- The AT91SAM7XC256 embeds a high-speed 64-Kbyte SRAM bank.
- The AT91SAM7XC128 embeds a high-speed 32-Kbyte SRAM bank.

After reset and until the Remap Command is performed, the SRAM is only accessible at address 0x0020 0000. After Remap, the SRAM also becomes available at address 0x0.

8.4.2 Internal ROM

The AT91SAM7XC512/256/128 embeds an Internal ROM. At any time, the ROM is mapped at address 0x30 0000. The ROM contains the FFPI and the SAM-BA program.

8.4.3 Internal Flash

- The AT91SAM7XC512 features two banks (dual plane) of 256 Kbytes of Flash.
- The AT91SAM7XC256 features one bank (single plane) of 256 Kbytes of Flash.
- The AT91SAM7XC128 features one bank (single plane) of 128 Kbytes of Flash.

At any time, the Flash is mapped to address 0x0010 0000. It is also accessible at address 0x0 after the reset, if GPNVM bit 2 is set and before the Remap Command.

A general purpose NVM (GPNVM) bit is used to boot either on the ROM (default) or from the Flash.

This GPNVM bit can be cleared or set respectively through the commands “Clear General-purpose NVM Bit” and “Set General-purpose NVM Bit” of the EFC User Interface.

Setting the GPNVM Bit 2 selects the boot from the Flash. Asserting ERASE clears the GPNVM Bit 2 and thus selects the boot from the ROM by default.

Figure 8-2. Internal Memory Mapping with GPNVM Bit 2 = 0 (default)

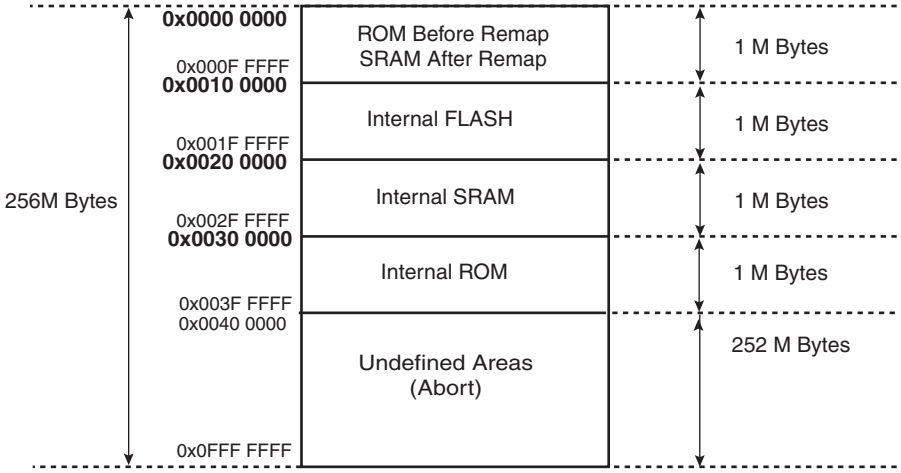
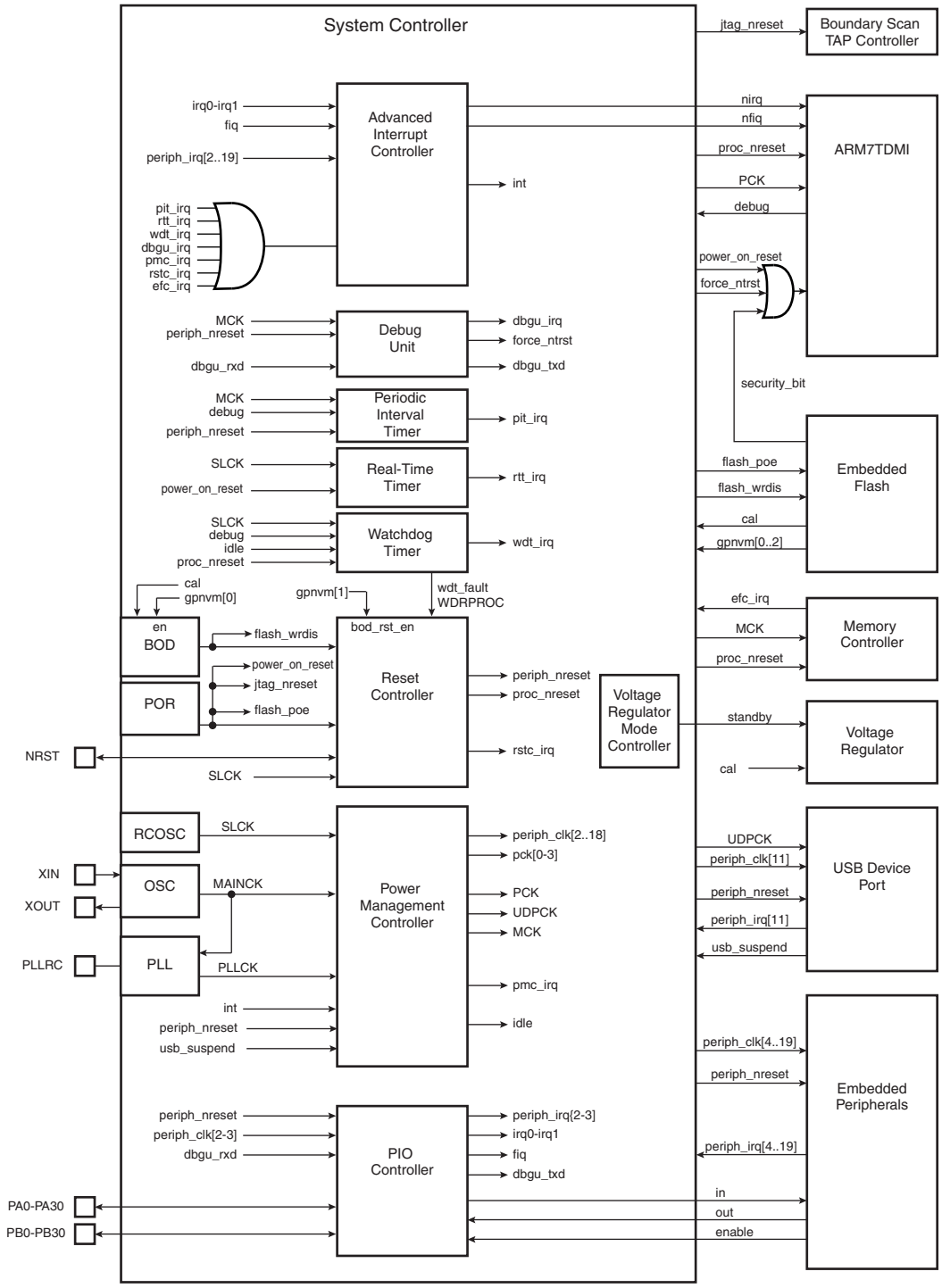


Figure 9-1. System Controller Block Diagram



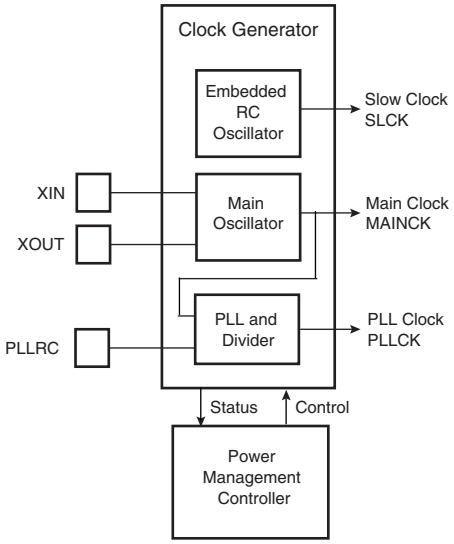
9.2 Clock Generator

The Clock Generator embeds one low-power RC Oscillator, one Main Oscillator and one PLL with the following characteristics:

- RC Oscillator ranges between 22 KHz and 42 KHz
- Main Oscillator frequency ranges between 3 and 20 MHz
- Main Oscillator can be bypassed
- PLL output ranges between 80 and 200 MHz

It provides SLCK, MAINCK and PLLCK.

Figure 9-2. Clock Generator Block Diagram



9.3 Power Management Controller

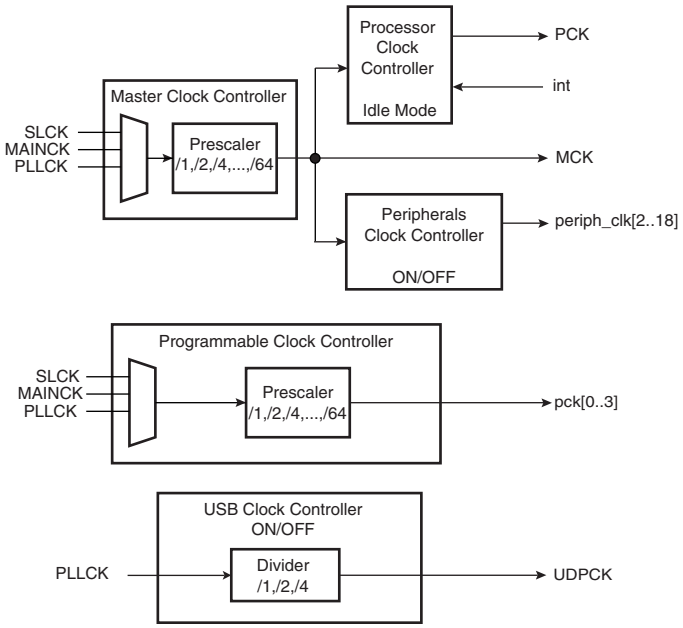
The Power Management Controller uses the Clock Generator outputs to provide:

- the Processor Clock PCK
- the Master Clock MCK
- the USB Clock UDPCK
- all the peripheral clocks, independently controllable
- four programmable clock outputs

The Master Clock (MCK) is programmable from a few hundred Hz to the maximum operating frequency of the device.

The Processor Clock (PCK) switches off when entering processor idle mode, thus allowing reduced power consumption while waiting for an interrupt.

Figure 9-3. Power Management Controller Block Diagram



9.4 Advanced Interrupt Controller

- Controls the interrupt lines (nIRQ and nFIQ) of an ARM Processor
- Individually maskable and vectored interrupt sources
  - Source 0 is reserved for the Fast Interrupt Input (FIQ)
  - Source 1 is reserved for system peripherals (RTT, PIT, EFC, PMC, DBGU, etc.)
  - Other sources control the peripheral interrupts or external interrupts
  - Programmable edge-triggered or level-sensitive internal sources
  - Programmable positive/negative edge-triggered or high/low level-sensitive external sources
- 8-level Priority Controller
  - Drives the normal interrupt nIRQ of the processor
  - Handles priority of the interrupt sources

10.3 Peripheral Multiplexing on PIO Lines

The AT91SAM7XC512/256/128 features two PIO controllers, PIOA and PIOB, that multiplex the I/O lines of the peripheral set.

Each PIO Controller controls 31 lines. Each line can be assigned to one of two peripheral functions, A or B. Some of them can also be multiplexed with the analog inputs of the ADC Controller.

Table 10-2 on page 34 and Table 10-3 on page 35 defines how the I/O lines of the peripherals A, B or the analog inputs are multiplexed on the PIO Controller A and PIO Controller B. The two columns “Function” and “Comments” have been inserted for the user’s own comments; they may be used to track how pins are defined in an application.

Note that some peripheral functions that are output only, may be duplicated in the table.

At reset, all I/O lines are automatically configured as input with the programmable pull-up enabled, so that the device is maintained in a static state as soon as a reset is detected.

10.5 PIO Controller B Multiplexing

Table 10-3. Multiplexing on PIO Controller B

PIO Controller B				Application Usage	
I/O Line	Peripheral A	Peripheral B	Comments	Function	Comments
PB0	ETXCK/EREFCK	PCK0			
PB1	ETXEN				
PB2	ETX0				
PB3	ETX1				
PB4	ECRS				
PB5	ERX0				
PB6	ERX1				
PB7	ERXER				
PB8	EMDC				
PB9	EMDIO				
PB10	ETX2	SPI1_NPCS1			
PB11	ETX3	SPI1_NPCS2			
PB12	ETXER	TCLK0			
PB13	ERX2	SPI0_NPCS1			
PB14	ERX3	SPI0_NPCS2			
PB15	ERXDV/ECRSDV				
PB16	ECOL	SPI1_NPCS3			
PB17	ERXCK	SPI0_NPCS3			
PB18	EF100	ADTRG			
PB19	PWM0	TCLK1			
PB20	PWM1	PCK0			
PB21	PWM2	PCK1			
PB22	PWM3	PCK2			
PB23	TIOA0	DCD1			
PB24	TIOB0	DSR1			
PB25	TIOA1	DTR1			
PB26	TIOB1	RI1			
PB27	TIOA2	PWM0	AD0		
PB28	TIOB2	PWM1	AD1		
PB29	PCK1	PWM2	AD2		
PB30	PCK2	PWM3	AD3		

10.8 Two-wire Interface

- Master Mode only
- Compatibility with I^2C compatible devices (refer to the TWI section of the datasheet)
- One, two or three bytes internal address registers for easy Serial Memory access
- 7-bit or 10-bit slave addressing
- Sequential read/write operations

10.9 USART

- Programmable Baud Rate Generator
- 5- to 9-bit full-duplex synchronous or asynchronous serial communications
  - 1, 1.5 or 2 stop bits in Asynchronous Mode
  - 1 or 2 stop bits in Synchronous Mode
  - Parity generation and error detection
  - Framing error detection, overrun error detection
  - MSB or LSB first
  - Optional break generation and detection
  - By 8 or by 16 over-sampling receiver frequency
  - Hardware handshaking RTS - CTS
  - Modem Signals Management DTR-DSR-DCD-RI on USART1
  - Receiver time-out and transmitter timeguard
  - Multi-drop Mode with address generation and detection
- RS485 with driver control signal
- ISO7816, T = 0 or T = 1 Protocols for interfacing with smart cards
  - NACK handling, error counter with repetition and iteration limit
- IrDA modulation and demodulation
  - Communication at up to 115.2 Kbps
- Test Modes
  - Remote Loopback, Local Loopback, Automatic Echo

10.10 Serial Synchronous Controller

- Provides serial synchronous communication links used in audio and telecom applications
- Contains an independent receiver and transmitter and a common clock divider
- Offers a configurable frame sync and data length
- Receiver and transmitter can be programmed to start automatically or on detection of different event on the frame sync signal
- Receiver and transmitter include a data signal, a clock signal and a frame synchronization signal

10.11 Timer Counter

- Three 16-bit Timer Counter Channels
  - Two output compare or one input capture per channel
- Wide range of functions including:
  - Frequency measurement
  - Event counting
  - Interval measurement
  - Pulse generation
  - Delay timing
  - Pulse Width Modulation
  - Up/down capabilities
- Each channel is user-configurable and contains:
  - Three external clock inputs
- Five internal clock inputs, as defined in Table 10-4

Table 10-4. Timer Counter Clocks Assignment

TC Clock input	Clock
TIMER_CLOCK1	MCK/2
TIMER_CLOCK2	MCK/8
TIMER_CLOCK3	MCK/32
TIMER_CLOCK4	MCK/128
TIMER_CLOCK5	MCK/1024

  - Two multi-purpose input/output signals
  - Two global registers that act on all three TC channels

10.12 Pulse Width Modulation Controller

- Four channels, one 16-bit counter per channel
- Common clock generator, providing thirteen different clocks
  - One Modulo n counter providing eleven clocks
  - Two independent linear dividers working on modulo n counter outputs
- Independent channel programming
  - Independent enable/disable commands
  - Independent clock selection
  - Independent period and duty cycle, with double buffering
  - Programmable selection of the output waveform polarity
  - Programmable center or left aligned output waveform

10.13 USB Device Port

- USB V2.0 full-speed compliant,12 Mbits per second
- Embedded USB V2.0 full-speed transceiver
- Embedded 1352-byte dual-port RAM for endpoints
- Six endpoints
  - Endpoint 0: 8 bytes
  - Endpoint 1 and 2: 64 bytes ping-pong
  - Endpoint 3: 64 bytes
  - Endpoint 4 and 5: 256 bytes ping-pong
  - Ping-pong Mode (two memory banks) for bulk endpoints
- Suspend/resume logic

10.14 CAN Controller

- Fully compliant with CAN 2.0A and 2.0B
- Bit rates up to 1Mbit/s
- Eight object oriented mailboxes each with the following properties:
  - CAN Specification 2.0 Part A or 2.0 Part B Programmable for each Message
  - Object configurable to receive (with overwrite or not) or transmit
  - Local tag and mask filters up to 29-bit identifier/channel
  - 32-bit access to data registers for each mailbox data object
  - Uses a 16-bit time stamp on receive and transmit message
  - Hardware concatenation of ID unmasked bitfields to speedup family ID processing
  - 16-bit internal timer for time stamping and network synchronization
  - Programmable reception buffer length up to 8 mailbox objects
  - Priority management between transmission mailboxes
  - Autobaud and listening mode
  - Low power mode and programmable wake-up on bus activity or by the application
  - Data, remote, error and overload frame handling

10.15 128-bit Advanced Encryption Standard

- Compliant with FIPS Publication 197, Advanced Encryption Standard (AES)
- 128-bit (AT91SAM7XC256/128) or 128-bit/192-bit/256-bit (AT91SAM7XC512) Cryptographic Key
- 12-clock Cycles Encryption/Decryption Processing Time (AT91SAM7XC256/128)
- 12/13/14-clock Cycles Encryption/Decryption Processing Time (AT91SAM7XC512)
- Support of the Five Standard Modes of Operation specified in the NIST Special Publication 800-38A:
  - Electronic Codebook (ECB)
  - Cipher Block Chaining (CBC)
  - Cipher Feedback (CFB)
  - Output Feedback (OFB)

  - Automatic wakeup on trigger and back to sleep mode after conversions of all enabled channels
- Four of eight analog inputs shared with digital signals

11. Package Drawings

Figure 11-1. LQFP Package Drawing

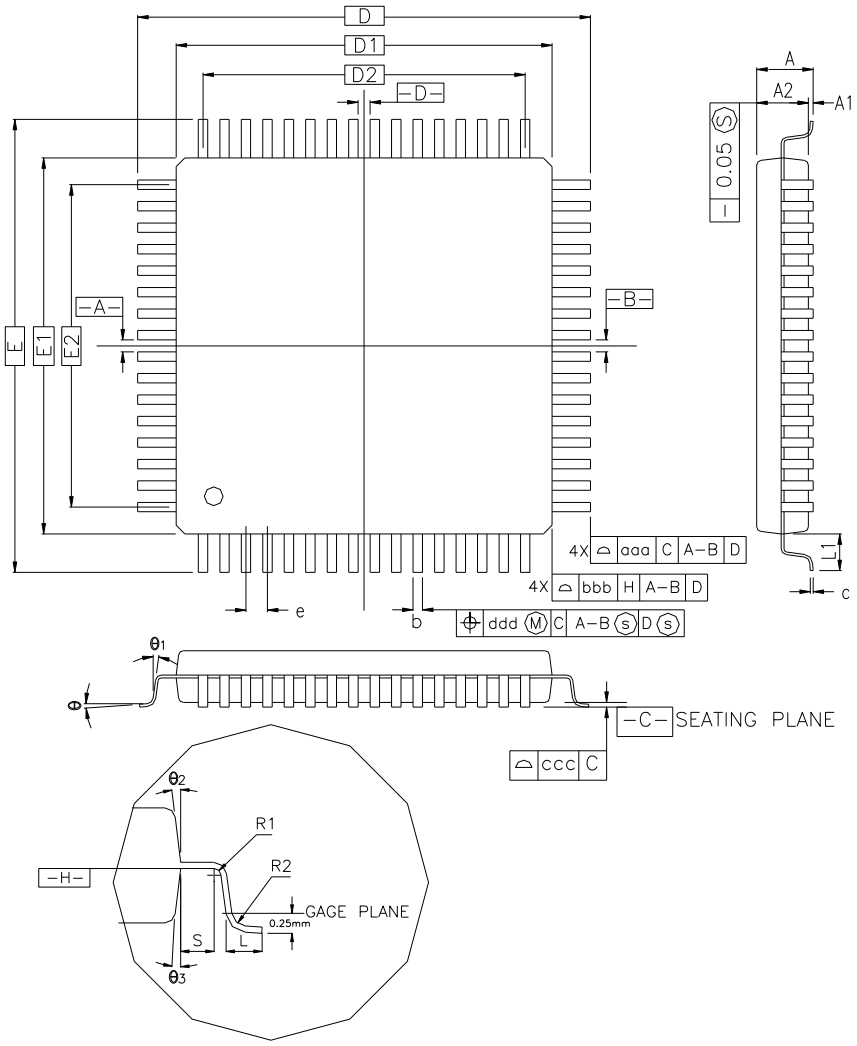
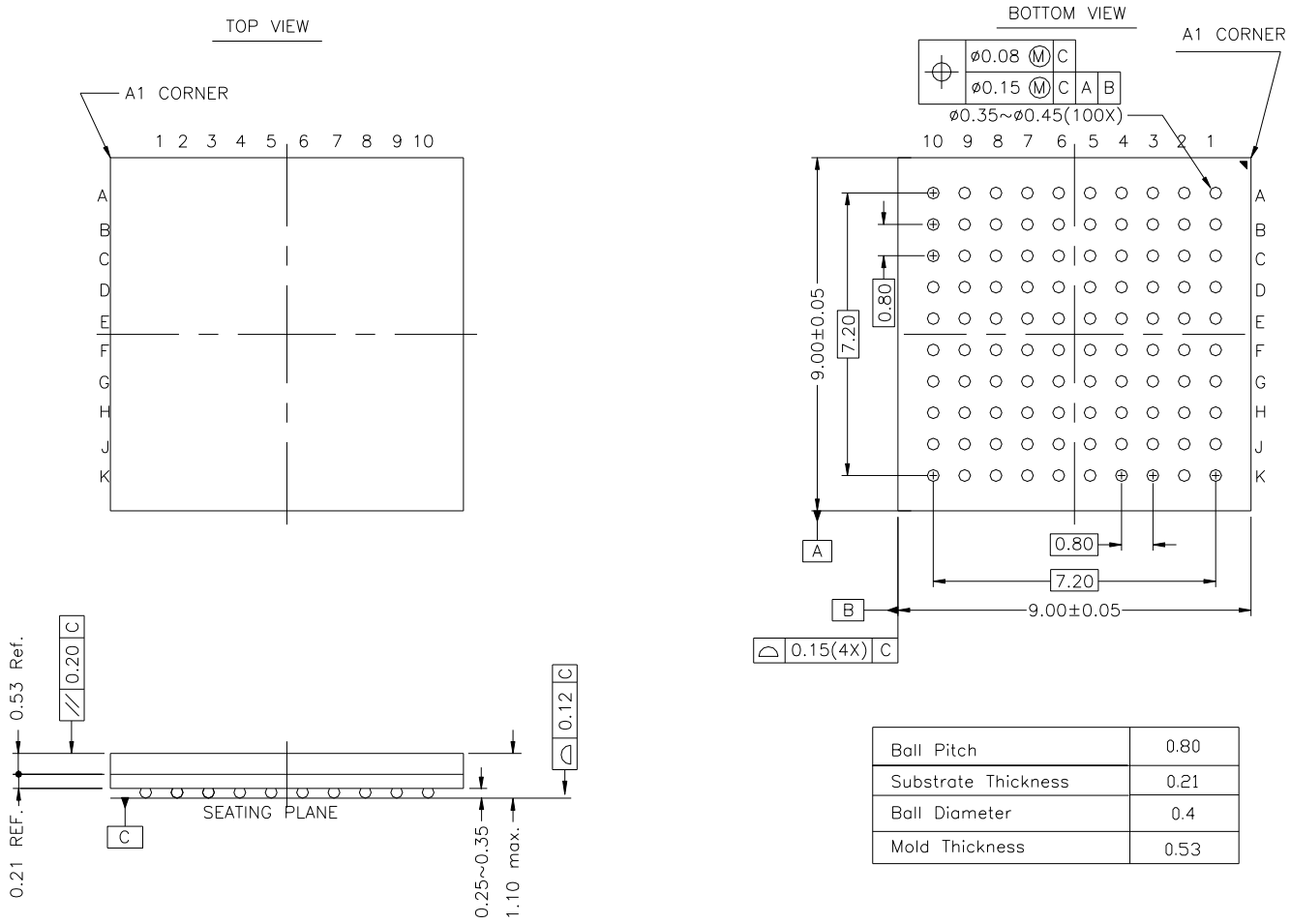


Figure 11-2. 100-TFBGA Package Drawing



Ball Pitch	0.80
Substrate Thickness	0.21
Ball Diameter	0.4
Mold Thickness	0.53

All dimensions are in mm

12. AT91SAM7XC512/256/128 Ordering Information

Table 12-1. Ordering Information

MLR A Ordering Code	MLR B Ordering Code	Package	Package Type	Temperature Operating Range
AT91SAM7XC512-AU AT91SAM7XC512-CU	–	LQFP 100 TFBGA 100	Green	Industrial (-40· C to 85· C)
AT91SAM7XC256-AU AT91SAM7XC256-CU	AT91SAM7XC256B-AU AT91SAM7XC256B-CU	LQFP 100 TFBGA 100	Green	Industrial (-40· C to 85· C)
AT91SAM7XC128-AU AT91SAM7XC128-CU	AT91SAM7XC128B-AU AT91SAM7XC128B-CU	LQFP 100 TFBGA 100	Green	Industrial (-40· C to 85· C)

13. Export Regulations Statement

These commodities, technology or software will be exported from France and the applicable Export Administration Regulations will apply. French, United States and other relevant laws, regulations and requirements regarding the export of products may restrict sale, export and re-export of these products; please assure you conduct your activities in accordance with the applicable relevant export regulations.

Revision History

Table 13-1. Revision History

Doc. Rev	Comments	Change Request Ref.
6209S	First issue - Unqualified on Intranet Legal page updated.Qualified on Intranet	
6209BS	Added AT91SAM7XC512 to product family.“Features” on page 1 and global Reformatted Memories Section 8. “Memory” on page 18. Reordered sub sections in Peripherals Section 10. “Peripherals” on page 32 Consolidated Memory Mapping in Figure 8-1 on page 19. Added package drawings Section 11. “Package Drawings” on page 42. Consolidated Memory Mapping in Figure 8-1 on page 19. Added TFBGA information Section 4.3 “100-ball TFBGA Package Outline” on page 11. and Section 4.4 on page 10 and “Features” on page 1 Added LQFP and TFBGA package drawings Section 11. on page 42. System Controller block diagram Figure 9-1 on page 26, “ice_nreset” signals changed to “power_on_reset”.	2729
6209CS	“Features”, TWI updated to include Atmel TWI compatibility with I^2C Standard. “Features”, “Debug Unit (DBGU)” added “Mode for General Purpose 2-wire UART Serial Communication”. Section 10.8 ”Two-wire Interface”, updated. Section 10.11 ”Timer Counter”,The TC has Two output compare or one input capture per channel. Section 10.17 ”Analog-to-Digital Converter”,INL and DNL updated. Figure 3-1,”Signal Description List”, footnote added to JTAGSEL, ERASE and TST pin comments Section 6.1 ”JTAG Port Pins”, Section 6.2 ”Test Pin” and Section 6.4 ”ERASE Pin”updated. Figure 9-1,”System Controller Block Diagram”, RTT is reset by power_on_reset. Figure 8-1,”AT91SAM7XC512/256/128 Memory Mapping”,TDES base address is 0xFFFA 8000 Section 8.4.3 ”Internal Flash”,updated: “At any time, the Flash is mapped ... if GPNVM bit 2 is set and before the Remap Command.”	4247 5846 4211 4008 5068 5225 5257 5850
6209DS	Section 12. ”AT91SAM7XC512/256/128 Ordering Information”, MLR B chip revision added to ordering information.	6064

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