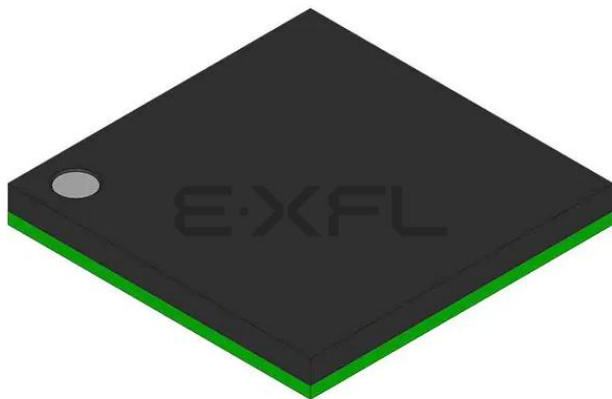




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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	55MHz
Connectivity	CANbus, Ethernet, I ² C, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	62
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 1.95V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-TFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/atmel/at91sam7xc512-cu

- Real-time Timer (RTT)
 - 32-bit Free-running Counter with Alarm
 - Runs Off the Internal RC Oscillator
- Two Parallel Input/Output Controllers (PIO)
 - Sixty-two Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os
 - Input Change Interrupt Capability on Each I/O Line
 - Individually Programmable Open-drain, Pull-up Resistor and Synchronous Output
- Seventeen Peripheral DMA Controller (PDC) Channels
- One Advanced Encryption System (AES)
 - 256-, 192-, 128-bit Key Algorithm, Compliant with FIPS PUB 197 Specifications (AT91SAM7XC512)
 - 128-bit Key Algorithm, Compliant with FIPS PUB 197 Specifications (AT91SAM7XC256/128)
 - Buffer Encryption/Decryption Capabilities with PDC
- One Triple Data Encryption System (TDES)
 - Two-key or Three-key Algorithms, Compliant with FIPS PUB 46-3 Specifications
 - Optimized for Triple Data Encryption Capability
- One USB 2.0 Full Speed (12 Mbits per second) Device Port
 - On-chip Transceiver, 1352-byte Configurable Integrated FIFOs
- One Ethernet MAC 10/100 base-T
 - Media Independent Interface (MII) or Reduced Media Independent Interface (RMII)
 - Integrated 28-byte FIFOs and Dedicated DMA Channels for Transmit and Receive
- One Part 2.0A and Part 2.0B Compliant CAN Controller
 - Eight Fully-programmable Message Object Mailboxes, 16-bit Time Stamp Counter
- One Synchronous Serial Controller (SSC)
 - Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
 - I²S Analog Interface Support, Time Division Multiplex Support
 - High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer
- Two Universal Synchronous/Asynchronous Receiver Transmitters (USART)
 - Individual Baud Rate Generator, IrDA Infrared Modulation/Demodulation
 - Support for ISO7816 T0/T1 Smart Card, Hardware Handshaking, RS485 Support
 - Full Modem Line Support on USART1
- Two Master/Slave Serial Peripheral Interfaces (SPI)
 - 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects
- One Three-channel 16-bit Timer/Counter (TC)
 - Three External Clock Inputs, Two Multi-purpose I/O Pins per Channel
 - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability
- One Four-channel 16-bit Power Width Modulation Controller (PWMC)
- One Two-wire Interface (TWI)
 - Master Mode Support Only, All Two-wire Atmel EEPROMs and I²C Compatible Devices Supported
- One 8-channel 10-bit Analog-to-Digital Converter, Four Channels Multiplexed with Digital I/Os
- SAM-BA™ Boot Assistant
 - Default Boot program
 - Interface with SAM-BA Graphic User Interface
- IEEE 1149.1 JTAG Boundary Scan on All Digital Pins
- 5V-tolerant I/Os, Including Four High-current Drive I/O lines, Up to 16 mA Each
- Power Supplies
 - Embedded 1.8V Regulator, Drawing up to 100 mA for the Core and External Components
 - 3.3V VDDIO I/O Lines Power Supply, Independent 3.3V VDDFLASH Flash Power Supply
 - 1.8V VDDCORE Core Power Supply with Brownout Detector

1. Description

Atmel's AT91SAM7XC512/256/128 is a member of a series of highly integrated Flash microcontrollers based on the 32-bit ARM RISC processor. It features 512/256/128 Kbyte high-speed Flash and 128/64/32 Kbyte SRAM, a large set of peripherals, including an 802.3 Ethernet MAC, a CAN controller, an AES 128 Encryption accelerator and a Triple Data Encryption System. A complete set of system functions minimizes the number of external components.

The embedded Flash memory can be programmed in-system via the JTAG-ICE interface or via a parallel interface on a production programmer prior to mounting. Built-in lock bits and a security bit protect the firmware from accidental overwrite and preserve its confidentiality.

The AT91SAM7XC512/256/128 system controller includes a reset controller capable of managing the power-on sequence of the microcontroller and the complete system. Correct device operation can be monitored by a built-in brownout detector and a watchdog running off an integrated RC oscillator.

By combining the ARM7TDMI processor with on-chip Flash and SRAM, and a wide range of peripheral functions, including USART, SPI, CAN Controller, Ethernet MAC, AES 128 accelerator, TDES, Timer Counter, RTT and Analog-to-Digital Converters on a monolithic chip, the AT91SAM7XC512/256/128 is a powerful device that provides a flexible, cost-effective solution to many embedded control applications requiring secure communication over, for example, Ethernet, CAN wired and Zigbee™ wireless networks.

1.1 Configuration Summary of the AT91SAM7XC512/256/128

The AT91SAM7XC512, AT91SAM7XC256 and AT91SAM7XC128 differ only in memory sizes. [Table 1-1](#) summarizes the configurations of the two devices.

Table 1-1. Configuration Summary

Device	Flash	Flash Organization	SRAM	AES	TDES
AT91SAM7XC512	512K bytes	dual plane	128K bytes	1 AES 256/192/128	1
AT91SAM7XC256	256K bytes	single plane	64K bytes	1 AES 128	1
AT91SAM7XC128	128K bytes	single plane	32K bytes	1 AES 128	1

3. Signal Description

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
Power				
VDDIN	Voltage Regulator and ADC Power Supply Input	Power		3V to 3.6V
VDDOUT	Voltage Regulator Output	Power		1.85V
VDDFLASH	Flash and USB Power Supply	Power		3V to 3.6V
VDDIO	I/O Lines Power Supply	Power		3V to 3.6V
VDDCORE	Core Power Supply	Power		1.65V to 1.95V
VDDPLL	PLL	Power		1.65V to 1.95V
GND	Ground	Ground		
Clocks, Oscillators and PLLs				
XIN	Main Oscillator Input	Input		
XOUT	Main Oscillator Output	Output		
PLLRC	PLL Filter	Input		
PCK0 - PCK3	Programmable Clock Output	Output		
ICE and JTAG				
TCK	Test Clock	Input		No pull-up resistor
TDI	Test Data In	Input		No pull-up resistor
TDO	Test Data Out	Output		
TMS	Test Mode Select	Input		No pull-up resistor
JTAGSEL	JTAG Selection	Input		Pull-down resistor ⁽¹⁾
Flash Memory				
ERASE	Flash and NVM Configuration Bits Erase Command	Input	High	Pull-down resistor ⁽¹⁾
Reset/Test				
NRST	Microcontroller Reset	I/O	Low	Pull-Up resistor, Open Drain Output.
TST	Test Mode Select	Input	High	Pull-down resistor ⁽¹⁾
Debug Unit				
DRXD	Debug Receive Data	Input		
DTXD	Debug Transmit Data	Output		
AIC				
IRQ0 - IRQ1	External Interrupt Inputs	Input		
FIQ	Fast Interrupt Input	Input		
PIO				
PA0 - PA30	Parallel IO Controller A	I/O		Pulled-up input at reset.
PB0 - PB30	Parallel IO Controller B	I/O		Pulled-up input at reset.

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
USB Device Port				
DDM	USB Device Port Data -	Analog		
DDP	USB Device Port Data +	Analog		
USART				
SCK0 - SCK1	Serial Clock	I/O		
TXD0 - TXD1	Transmit Data	I/O		
RXD0 - RXD1	Receive Data	Input		
RTS0 - RTS1	Request To Send	Output		
CTS0 - CTS1	Clear To Send	Input		
DCD1	Data Carrier Detect	Input		
DTR1	Data Terminal Ready	Output		
DSR1	Data Set Ready	Input		
RI1	Ring Indicator	Input		
Synchronous Serial Controller				
TD	Transmit Data	Output		
RD	Receive Data	Input		
TK	Transmit Clock	I/O		
RK	Receive Clock	I/O		
TF	Transmit Frame Sync	I/O		
RF	Receive Frame Sync	I/O		
Timer/Counter				
TCLK0 - TCLK2	External Clock Inputs	Input		
TIOA0 - TIOA2	I/O Line A	I/O		
TIOB0 - TIOB2	I/O Line B	I/O		
PWM Controller				
PWM0 - PWM3	PWM Channels	Output		
Serial Peripheral Interface - SPIx				
SPIx_MISO	Master In Slave Out	I/O		
SPIx_MOSI	Master Out Slave In	I/O		
SPIx_SPCK	SPI Serial Clock	I/O		
SPIx_NPCS0	SPI Peripheral Chip Select 0	I/O	Low	
SPIx_NPCS1-NPCS3	SPI Peripheral Chip Select 1 to 3	Output	Low	
Two-wire Interface				
TWD	Two-wire Serial Data	I/O		
TWCK	Two-wire Serial Clock	I/O		

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Comments
Analog-to-Digital Converter				
AD0-AD3	Analog Inputs	Analog		Digital pulled-up inputs at reset.
AD4-AD7	Analog Inputs	Analog		Analog Inputs
ADTRG	ADC Trigger	Input		
ADVREF	ADC Reference	Analog		
Fast Flash Programming Interface				
PGMEN0-PGMEN1	Programming Enabling	Input		
PGMM0-PGMM3	Programming Mode	Input		
PGMD0-PGMD15	Programming Data	I/O		
PGMRDY	Programming Ready	Output	High	
PGMNVALID	Data Direction	Output	Low	
PGMNOE	Programming Read	Input	Low	
PGMCK	Programming Clock	Input		
PGMNCMD	Programming Command	Input	Low	
CAN Controller				
CANRX	CAN Input	Input		
CANTX	CAN Output	Output		
Ethernet MAC 10/100				
EREFCK	Reference Clock	Input		RMII only
ETXCK	Transmit Clock	Input		MII only
ERXCK	Receive Clock	Input		MII only
ETXEN	Transmit Enable	Output		
ETX0 - ETX3	Transmit Data	Output		ETX0 - ETX1 only in RMII
ETXER	Transmit Coding Error	Output		MII only
ERXDV	Receive Data Valid	Input		MII only
ECRSDV	Carrier Sense and Data Valid	Input		RMII only
ERX0 - ERX3	Receive Data	Input		ERX0 - ERX1 only in RMII
ERXER	Receive Error	Input		
ECRS	Carrier Sense	Input		MII only
ECOL	Collision Detected	Input		MII only
EMDC	Management Data Clock	Output		
EMDIO	Management Data Input/Output	I/O		
EF100	Force 100 Mb/s/sec.	Output	High	RMII only

Note: 1. Refer to [Section 6. "I/O Lines Considerations"](#).

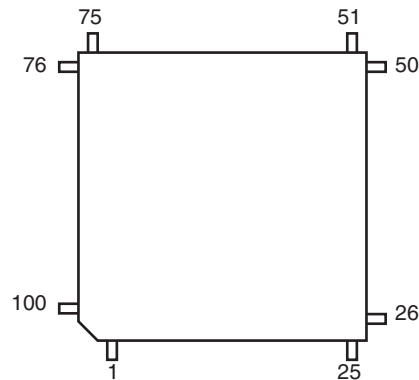
4. Package

The AT91SAM7XC512/256/128 is available in 100-lead LQFP Green and 100-ball TFBGA RoHS-compliant packages.

4.1 100-lead LQFP Package Outline

Figure 4-1 shows the orientation of the 100-lead LQFP package. A detailed mechanical description is given in the Mechanical Characteristics section of the full datasheet.

Figure 4-1. 100-lead LQFP Package Outline (Top View)



5. Power Considerations

5.1 Power Supplies

The AT91SAM7XC512/256/128 has six types of power supply pins and integrates a voltage regulator, allowing the device to be supplied with only one voltage. The six power supply pin types are:

- VDDIN pin. It powers the voltage regulator and the ADC; voltage ranges from 3.0V to 3.6V, 3.3V nominal. In order to decrease current consumption, if the voltage regulator and the ADC are not used, VDDIN, ADVREF, AD4, AD5, AD6 and AD7 should be connected to GND. In this case, VDDOUT should be left unconnected.
- VDDOUT pin. It is the output of the 1.8V voltage regulator.
- VDDIO pin. It powers the I/O lines; voltage ranges from 3.0V to 3.6V, 3.3V nominal.
- VDDFLASH pin. It powers the USB transceivers and a part of the Flash and is required for the Flash to operate correctly; voltage ranges from 3.0V to 3.6V, 3.3V nominal.
- VDDCORE pins. They power the logic of the device; voltage ranges from 1.65V to 1.95V, 1.8V typical. It can be connected to the VDDOUT pin with decoupling capacitor. VDDCORE is required for the device, including its embedded Flash, to operate correctly.
- VDDPLL pin. It powers the oscillator and the PLL. It can be connected directly to the VDDOUT pin.

No separate ground pins are provided for the different power supplies. Only GND pins are provided and should be connected as shortly as possible to the system ground plane.

5.2 Power Consumption

The AT91SAM7XC512/256/128 has a static current of less than 60 μ A on VDDCORE at 25°C, including the RC oscillator, the voltage regulator and the power-on reset when the brownout detector is deactivated. Activating the brownout detector adds 28 μ A static current.

The dynamic power consumption on VDDCORE is less than 90 mA at full speed when running out of the Flash. Under the same conditions, the power consumption on VDDFLASH does not exceed 10 mA.

5.3 Voltage Regulator

The AT91SAM7XC512/256/128 embeds a voltage regulator that is managed by the System Controller.

In Normal Mode, the voltage regulator consumes less than 100 μ A static current and draws 100 mA of output current.

The voltage regulator also has a Low-power Mode. In this mode, it consumes less than 25 μ A static current and draws 1 mA of output current.

Adequate output supply decoupling is mandatory for VDDOUT to reduce ripple and avoid oscillations. The best way to achieve this is to use two capacitors in parallel: one external 470 pF (or 1 nF) NPO capacitor should be connected between VDDOUT and GND as close to the chip as possible. One external 2.2 μ F (or 3.3 μ F) X7R capacitor should be connected between VDDOUT and GND.

- Embedded Flash Controller
 - Embedded Flash interface, up to three programmable wait states
 - Prefetch buffer, buffering and anticipating the 16-bit requests, reducing the required wait states
 - Key-protected program, erase and lock/unlock sequencer
 - Single command for erasing, programming and locking operations
 - Interrupt generation in case of forbidden operation

7.4 Peripheral DMA Controller

- Handles data transfer between peripherals and memories
- Seventeen channels
 - Two for each USART
 - Two for the Debug Unit
 - Two for the Serial Synchronous Controller
 - Two for each Serial Peripheral Interface
 - Two for the Advanced Encryption Standard 128-bit accelerator
 - Two for the Triple Data Encryption Standard 128-bit accelerator
 - One for the Analog-to-digital Converter
- Low bus arbitration overhead
 - One Master Clock cycle needed for a transfer from memory to peripheral
 - Two Master Clock cycles needed for a transfer from peripheral to memory
- Next Pointer management for reducing interrupt latency requirements

8. Memory

8.1 AT91SAM7XC512

- 512 Kbytes of dual-plane Flash Memory
 - 2 contiguous banks of 1024 pages of 256 bytes
 - Fast access time, 30 MHz single-cycle access in Worst Case conditions
 - Page programming time: 6 ms, including page auto-erase
 - Page programming without auto-erase: 3 ms
 - Full chip erase time: 15 ms
 - 10,000 write cycles, 10-year data retention capability
 - 32 lock bits, protecting 32 sectors of 64 pages
 - Protection Mode to secure contents of the Flash
- 128 Kbytes of Fast SRAM
 - Single-cycle access at full speed

8.2 AT91SAM7XC256

- 256 Kbytes of Flash Memory
 - 1024 pages of 256 bytes
 - Fast access time, 30 MHz single-cycle access in Worst Case conditions
 - Page programming time: 6 ms, including page auto-erase
 - Page programming without auto-erase: 3 ms
 - Full chip erase time: 15 ms
 - 10,000 write cycles, 10-year data retention capability
 - 16 lock bits, each protecting 16 sectors of 64 pages
 - Protection Mode to secure contents of the Flash
- 64 Kbytes of Fast SRAM
 - Single-cycle access at full speed

8.3 AT91SAM7XC128

- 128 Kbytes of Flash Memory
 - 512 pages of 256 bytes
 - Fast access time, 30 MHz single-cycle access in Worst Case conditions
 - Page programming time: 6 ms, including page auto-erase
 - Page programming without auto-erase: 3 ms
 - Full chip erase time: 15 ms
 - 10,000 write cycles, 10-year data retention capability
 - 8 lock bits, each protecting 8 sectors of 64 pages
 - Protection Mode to secure contents of the Flash
- 32 Kbytes of Fast SRAM
 - Single-cycle access at full speed

8.4 Memory Mapping

8.4.1 Internal RAM

- The AT91SAM7XC512 embeds a high-speed 128-Kbyte SRAM bank.
- The AT91SAM7XC256 embeds a high-speed 64-Kbyte SRAM bank.
- The AT91SAM7XC128 embeds a high-speed 32-Kbyte SRAM bank.

After reset and until the Remap Command is performed, the SRAM is only accessible at address 0x0020 0000. After Remap, the SRAM also becomes available at address 0x0.

8.4.2 Internal ROM

The AT91SAM7XC512/256/128 embeds an Internal ROM. At any time, the ROM is mapped at address 0x30 0000. The ROM contains the FFPI and the SAM-BA program.

8.4.3 Internal Flash

- The AT91SAM7XC512 features two banks (dual plane) of 256 Kbytes of Flash.
- The AT91SAM7XC256 features one bank (single plane) of 256 Kbytes of Flash.
- The AT91SAM7XC128 features one bank (single plane) of 128 Kbytes of Flash.

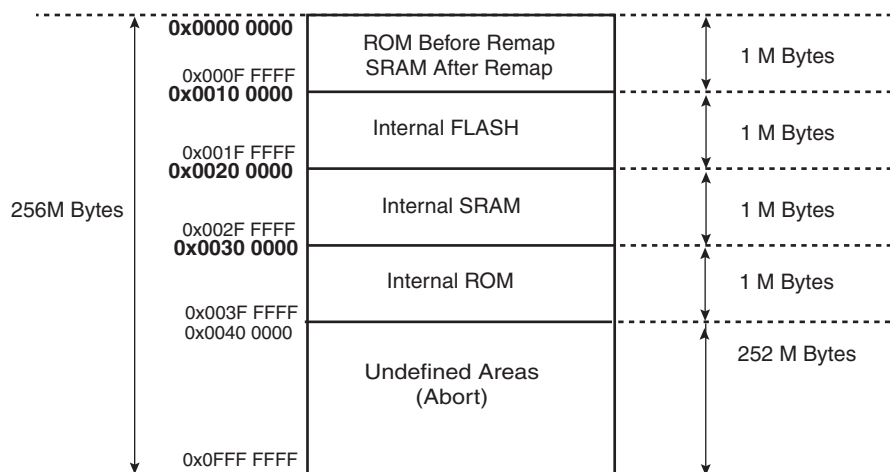
At any time, the Flash is mapped to address 0x0010 0000. It is also accessible at address 0x0 after the reset, if GPNVM bit 2 is set and before the Remap Command.

A general purpose NVM (GPNVM) bit is used to boot either on the ROM (default) or from the Flash.

This GPNVM bit can be cleared or set respectively through the commands “Clear General-purpose NVM Bit” and “Set General-purpose NVM Bit” of the EFC User Interface.

Setting the GPNVM Bit 2 selects the boot from the Flash. Asserting ERASE clears the GPNVM Bit 2 and thus selects the boot from the ROM by default.

Figure 8-2. Internal Memory Mapping with GPNVM Bit 2 = 0 (default)



plane may be performed even while program or erase functions are being executed in the other memory plane.

One EFC is embedded in the AT91SAM7XC256/128 to control the single plane of 256/128 KBytes.

8.5.3 Lock Regions

8.5.3.1 AT91SAM7XC512

Two Embedded Flash Controllers each manage 16 lock bits to protect 16 regions of the flash against inadvertent flash erasing or programming commands. The AT91SAM7XC512 contains 32 lock regions and each lock region contains 64 pages of 256 bytes. Each lock region has a size of 16 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the EFC trigs an interrupt.

The 32 NVM bits are software programmable through both of the EFC User Interfaces. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

8.5.3.2 AT91SAM7XC256

The Embedded Flash Controller manages 16 lock bits to protect 16 regions of the flash against inadvertent flash erasing or programming commands. The AT91SAM7XC256 contains 16 lock regions and each lock region contains 64 pages of 256 bytes. Each lock region has a size of 16 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the EFC trigs an interrupt.

The 16 NVM bits are software programmable through the EFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

8.5.3.3 AT91SAM7XC128

The Embedded Flash Controller manages 8 lock bits to protect 8 regions of the flash against inadvertent flash erasing or programming commands. The AT91SAM7XC128 contains 8 lock regions and each lock region contains 64 pages of 256 bytes. Each lock region has a size of 16 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the EFC trigs an interrupt.

The 8 NVM bits are software programmable through the EFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

8.5.4 Security Bit Feature

The AT91SAM7XC512/256/128 features a security bit, based on a specific NVM-Bit. When the security is enabled, any access to the Flash, either through the ICE interface or through the Fast



- Communication via the USB Device Port is limited to an 18.432 MHz crystal.

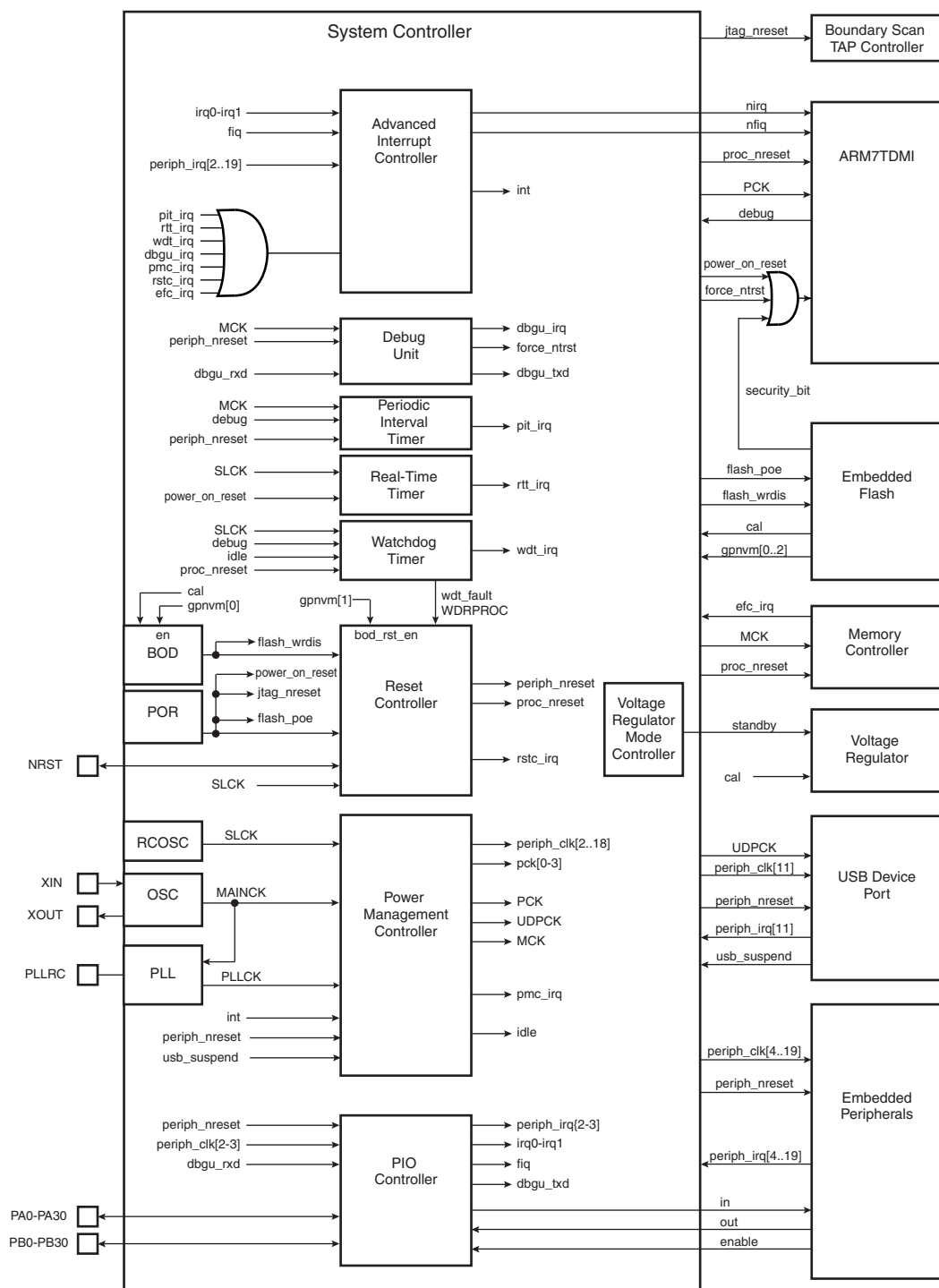
The SAM-BA Boot provides an interface with SAM-BA Graphic User Interface (GUI).

The SAM-BA Boot is in ROM and is mapped at address 0x0 when the GPNVM Bit 2 is set to 0.

When GPNVM bit 2 is set to 1, the device boots from the Flash.

When GPNVM bit 2 is set to 0, the device boots from ROM (SAM-BA).

Figure 9-1. System Controller Block Diagram



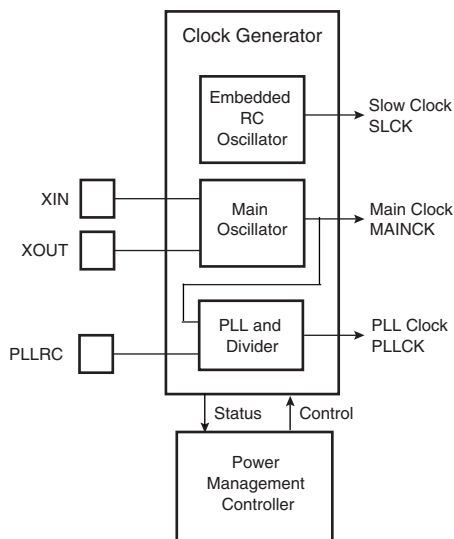
9.2 Clock Generator

The Clock Generator embeds one low-power RC Oscillator, one Main Oscillator and one PLL with the following characteristics:

- RC Oscillator ranges between 22 KHz and 42 KHz
- Main Oscillator frequency ranges between 3 and 20 MHz
- Main Oscillator can be bypassed
- PLL output ranges between 80 and 200 MHz

It provides SLCK, MAINCK and PLLCK.

Figure 9-2. Clock Generator Block Diagram



10.4 PIO Controller A Multiplexing

Table 10-2. Multiplexing on PIO Controller A

PIO Controller A				Application Usage	
I/O Line	Peripheral A	Peripheral B	Comments	Function	Comments
PA0	RXD0		High-Drive		
PA1	TXD0		High-Drive		
PA2	SCK0	SPI1_NPCS1	High-Drive		
PA3	RTS0	SPI1_NPCS2	High-Drive		
PA4	CTS0	SPI1_NPCS3			
PA5	RXD1				
PA6	TXD1				
PA7	SCK1	SPI0_NPCS1			
PA8	RTS1	SPI0_NPCS2			
PA9	CTS1	SPI0_NPCS3			
PA10	TWD				
PA11	TWCK				
PA12	SPI_NPCS0				
PA13	SPI0_NPCS1	PCK1			
PA14	SPI0_NPCS2	IRQ1			
PA15	SPI0_NPCS3	TCLK2			
PA16	SPI0_MISO				
PA17	SPI0_MOSI				
PA18	SPI0_SPCK				
PA19	CANRX				
PA20	CANTX				
PA21	TF	SPI1_NPCS0			
PA22	TK	SPI1_SPCK			
PA23	TD	SPI1_MOSI			
PA24	RD	SPI1_MISO			
PA25	RK	SPI1_NPCS1			
PA26	RF	SPI1_NPCS2			
PA27	DRXD	PCK3			
PA28	DTXD				
PA29	FIQ	SPI1_NPCS3			
PA30	IRQ0	PCK2			

10.5 PIO Controller B Multiplexing

Table 10-3. Multiplexing on PIO Controller B

PIO Controller B				Application Usage	
I/O Line	Peripheral A	Peripheral B	Comments	Function	Comments
PB0	ETXCK/EREFCK	PCK0			
PB1	ETXEN				
PB2	ETX0				
PB3	ETX1				
PB4	ECRS				
PB5	ERX0				
PB6	ERX1				
PB7	ERXER				
PB8	EMDC				
PB9	EMDIO				
PB10	ETX2	SPI1_NPCS1			
PB11	ETX3	SPI1_NPCS2			
PB12	ETXER	TCLK0			
PB13	ERX2	SPI0_NPCS1			
PB14	ERX3	SPI0_NPCS2			
PB15	ERXDV/ECRSDV				
PB16	ECOL	SPI1_NPCS3			
PB17	ERXCK	SPI0_NPCS3			
PB18	EF100	ADTRG			
PB19	PWM0	TCLK1			
PB20	PWM1	PCK0			
PB21	PWM2	PCK1			
PB22	PWM3	PCK2			
PB23	TIOA0	DCD1			
PB24	TIOB0	DSR1			
PB25	TIOA1	DTR1			
PB26	TIOB1	RI1			
PB27	TIOA2	PWM0	AD0		
PB28	TIOB2	PWM1	AD1		
PB29	PCK1	PWM2	AD2		
PB30	PCK2	PWM3	AD3		

10.6 Ethernet MAC

- DMA Master on Receive and Transmit Channels
- Compatible with IEEE Standard 802.3
- 10 and 100 Mbit/s operation
- Full- and half-duplex operation
- Statistics Counter Registers
- MII/RMII interface to the physical layer
- Interrupt generation to signal receive and transmit completion
- 28-byte transmit FIFO and 28-byte receive FIFO
- Automatic pad and CRC generation on transmitted frames
- Automatic discard of frames received with errors
- Address checking logic supports up to four specific 48-bit addresses
- Support Promiscuous Mode where all valid received frames are copied to memory
- Hash matching of unicast and multicast destination addresses
- Physical layer management through MDIO interface
- Half-duplex flow control by forcing collisions on incoming frames
- Full-duplex flow control with recognition of incoming pause frames
- Support for 802.1Q VLAN tagging with recognition of incoming VLAN and priority tagged frames
- Multiple buffers per receive and transmit frame
- Jumbo frames up to 10240 bytes supported

10.7 Serial Peripheral Interface

- Supports communication with external serial devices
 - Four chip selects with external decoder allow communication with up to 15 peripherals
 - Serial memories, such as DataFlash® and 3-wire EEPROMs
 - Serial peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors
 - External co-processors
- Master or slave serial peripheral bus interface
 - 8- to 16-bit programmable data length per chip select
 - Programmable phase and polarity per chip select
 - Programmable transfer delays per chip select, between consecutive transfers and between clock and data
 - Programmable delay between consecutive transfers
 - Selectable mode fault detection
 - Maximum frequency at up to Master Clock

10.11 Timer Counter

- Three 16-bit Timer Counter Channels
 - Two output compare or one input capture per channel
- Wide range of functions including:
 - Frequency measurement
 - Event counting
 - Interval measurement
 - Pulse generation
 - Delay timing
 - Pulse Width Modulation
 - Up/down capabilities
- Each channel is user-configurable and contains:
 - Three external clock inputs
- Five internal clock inputs, as defined in [Table 10-4](#)

Table 10-4. Timer Counter Clocks Assignment

TC Clock input	Clock
TIMER_CLOCK1	MCK/2
TIMER_CLOCK2	MCK/8
TIMER_CLOCK3	MCK/32
TIMER_CLOCK4	MCK/128
TIMER_CLOCK5	MCK/1024

- Two multi-purpose input/output signals
- Two global registers that act on all three TC channels

10.12 Pulse Width Modulation Controller

- Four channels, one 16-bit counter per channel
- Common clock generator, providing thirteen different clocks
 - One Modulo n counter providing eleven clocks
 - Two independent linear dividers working on modulo n counter outputs
- Independent channel programming
 - Independent enable/disable commands
 - Independent clock selection
 - Independent period and duty cycle, with double buffering
 - Programmable selection of the output waveform polarity
 - Programmable center or left aligned output waveform

Table 11-1. 100-lead LQFP Package Dimensions

Symbol	Millimeter			Inch		
	Min	Nom	Max	Min	Nom	Max
A			1.60			0.63
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BSC			0.630 BSC		
D1	14.00 BSC			0.551 BSC		
E	16.00 BSC			0.630 BSC		
E1	14.00 BSC			0.551 BSC		
R2	0.08		0.20	0.003		0.008
R1	0.08			0.003		
Q	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09		0.20	0.004		0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20			0.008		
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC			0.020 BSC		
D2	12.00			0.472		
E2	12.00			0.472		
Tolerances of Form and Position						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

12. AT91SAM7XC512/256/128 Ordering Information

Table 12-1. Ordering Information

MLR A Ordering Code	MLR B Ordering Code	Package	Package Type	Temperature Operating Range
AT91SAM7XC512-AU AT91SAM7XC512-CU	—	LQFP 100 TFBGA 100	Green	Industrial (-40· C to 85· C)
AT91SAM7XC256-AU AT91SAM7XC256-CU	AT91SAM7XC256B-AU AT91SAM7XC256B-CU	LQFP 100 TFBGA 100	Green	Industrial (-40· C to 85· C)
AT91SAM7XC128-AU AT91SAM7XC128-CU	AT91SAM7XC128B-AU AT91SAM7XC128B-CU	LQFP 100 TFBGA 100	Green	Industrial (-40· C to 85· C)

13. Export Regulations Statement

These commodities, technology or software will be exported from France and the applicable Export Administration Regulations will apply. French, United States and other relevant laws, regulations and requirements regarding the export of products may restrict sale, export and re-export of these products; please assure you conduct your activities in accordance with the applicable relevant export regulations.