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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

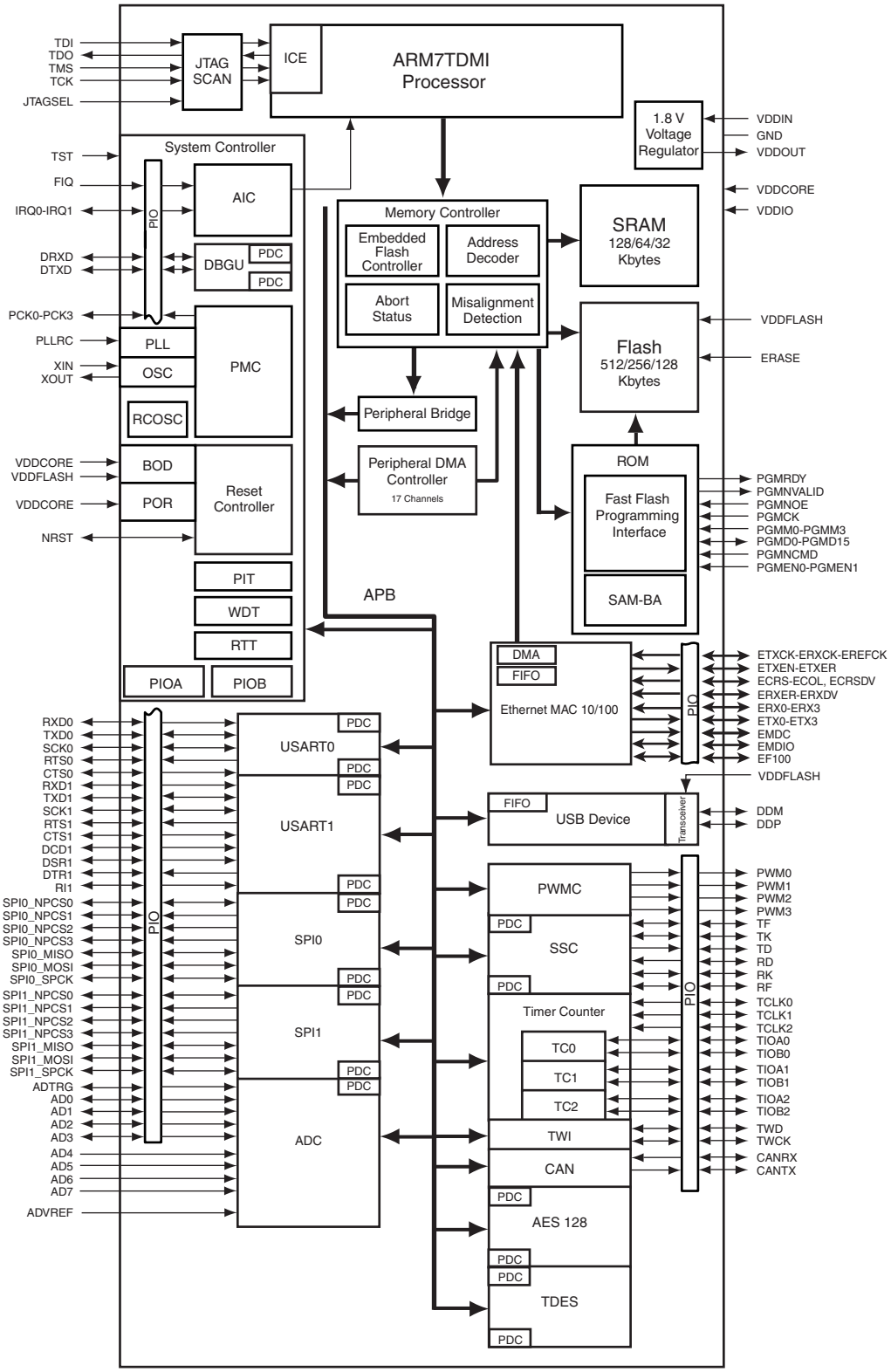
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	55MHz
Connectivity	CANbus, Ethernet, I²C, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	62
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 1.95V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at91sam7xc512b-au

- **Fully Static Operation: Up to 55 MHz at 1.65V and 85· C Worst Case Conditions**
- **Available in 100-lead LQFP Green and 100-ball TFBGA Green Packages**

2. AT91SAM7XC512/256/128 Block Diagram

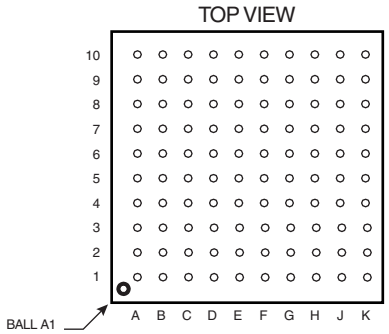
Figure 2-1. AT91SAM7XC512/256/128 Block Diagram



4.3 100-ball TFBGA Package Outline

Figure 4-2 shows the orientation of the 100-ball TFBGA package. A detailed mechanical description is given in the Mechanical Characteristics section of the full datasheet.

Figure 4-2. 100-ball TFBGA Package Orientation (Top View)



4.4 100-ball TFBGA Pinout

Table 4-2. Pinout in 100-ball TFBGA Package

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	PA22/PGMD10	C6	PB17	F1	PB21	H6	PA7/PGMNVALID
A2	PA21/PGMD9	C7	PB13	F2	PB23	H7	PA9/PGMM1
A3	PA20/PGMD8	C8	PA13/PGMD1	F3	PB25	H8	PA8/PGMM0
A4	PB1	C9	PA12/PGMD0	F4	PB26	H9	PB29/AD2
A5	PB7	C10	PA15/PGMD3	F5	TCK	H10	PLLRC
A6	PB5	D1	PA23/PGMD11	F6	PA6/PGMNOE	J1	PA29
A7	PB8	D2	PA24/PGMD12	F7	ERASE	J2	PA30
A8	PB9	D3	NRST	F8	VDDCORE	J3	PA0/PGMEN0
A9	PA18/PGMD6	D4	TST	F9	GND	J4	PA1/PGMEN1
A10	VDDIO	D5	PB19	F10	VDDIN	J5	VDDFLASH
B1	TDI	D6	PB6	G1	PB22	J6	GND
B2	PA19/PGMD7	D7	PA10/PGMM2	G2	PB24	J7	XIN/PGMCK
B3	PB11	D8	VDDIO	G3	PA27/PGMD15	J8	XOUT
B4	PB2	D9	PB27/AD0	G4	TDO	J9	GND
B5	PB12	D10	PA11/PGMM3	G5	PA2	J10	VDDPLL
B6	PB15	E1	PA25/PGMD13	G6	PA5/PGMRDY	K1	VDDCORE
B7	PB14	E2	PA26/PGMD14	G7	VDDCORE	K2	VDDCORE
B8	PA14/PGMD2	E3	PB18	G8	GND	K3	DDP
B9	PA16/PGMD4	E4	PB20	G9	PB30/AD3	K4	DDM
B10	PA17/PGMD5	E5	TMS	G10	VDDOUT	K5	GND
C1	PB16	E6	GND	H1	VDDCORE	K6	AD7
C2	PB4	E7	VDDIO	H2	PA28	K7	AD6
C3	PB10	E8	PB28/AD1	H3	JTAGSEL	K8	AD5
C4	PB3	E9	VDDIO	H4	PA3	K9	AD4
C5	PB0	E10	GND	H5	PA4/PGMNCMD	K10	ADVREF

5. Power Considerations

5.1 Power Supplies

The AT91SAM7XC512/256/128 has six types of power supply pins and integrates a voltage regulator, allowing the device to be supplied with only one voltage. The six power supply pin types are:

- VDDIN pin. It powers the voltage regulator and the ADC; voltage ranges from 3.0V to 3.6V, 3.3V nominal. In order to decrease current consumption, if the voltage regulator and the ADC are not used, VDDIN, ADVREF,AD4, AD5, AD6 and AD7 should be connected to GND. In this case, VDDOUT should be left unconnected.
- VDDOUT pin. It is the output of the 1.8V voltage regulator.
- VDDIO pin. It powers the I/O lines; voltage ranges from 3.0V to 3.6V, 3.3V nominal.
- VDDFLASH pin. It powers the USB transceivers and a part of the Flash and is required for the Flash to operate correctly; voltage ranges from 3.0V to 3.6V, 3.3V nominal.
- VDDCORE pins. They power the logic of the device; voltage ranges from 1.65V to 1.95V, 1.8V typical. It can be connected to the VDDOUT pin with decoupling capacitor. VDDCORE is required for the device, including its embedded Flash, to operate correctly.
- VDDPLL pin. It powers the oscillator and the PLL. It can be connected directly to the VDDOUT pin.

No separate ground pins are provided for the different power supplies. Only GND pins are provided and should be connected as shortly as possible to the system ground plane.

5.2 Power Consumption

The AT91SAM7XC512/256/128 has a static current of less than 60 µA on VDDCORE at 25°C, including the RC oscillator, the voltage regulator and the power-on reset when the brownout detector is deactivated. Activating the brownout detector adds 28 µA static current.

The dynamic power consumption on VDDCORE is less than 90 mA at full speed when running out of the Flash. Under the same conditions, the power consumption on VDDFLASH does not exceed 10 mA.

5.3 Voltage Regulator

The AT91SAM7XC512/256/128 embeds a voltage regulator that is managed by the System Controller.

In Normal Mode, the voltage regulator consumes less than 100 µA static current and draws 100 mA of output current.

The voltage regulator also has a Low-power Mode. In this mode, it consumes less than 25 µA static current and draws 1 mA of output current.

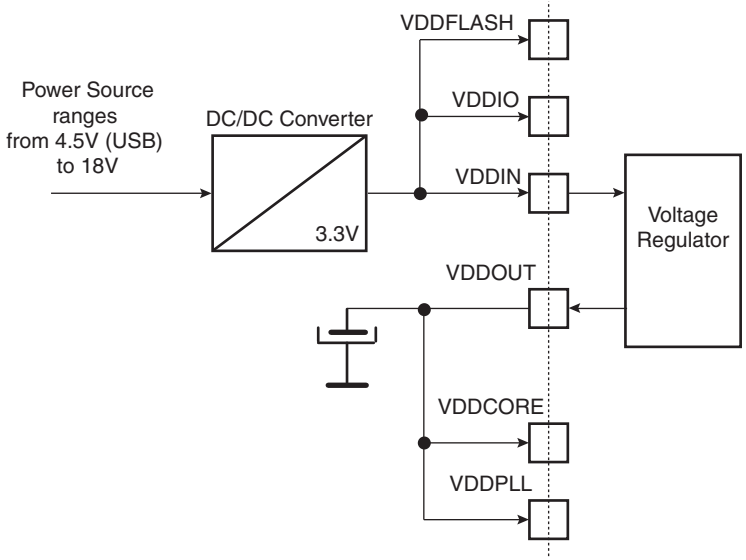
Adequate output supply decoupling is mandatory for VDDOUT to reduce ripple and avoid oscillations. The best way to achieve this is to use two capacitors in parallel: one external 470 pF (or 1 nF) NPO capacitor should be connected between VDDOUT and GND as close to the chip as possible. One external 2.2 µF (or 3.3 µF) X7R capacitor should be connected between VDDOUT and GND.

Adequate input supply decoupling is mandatory for VDDIN in order to improve startup stability and reduce source voltage drop. The input decoupling capacitor should be placed close to the chip. For example, two capacitors can be used in parallel: 100 nF NPO and 4.7 µF X7R.

5.4 Typical Powering Schematics

The AT91SAM7XC512/256/128 supports a 3.3V single supply mode. The internal regulator input connected to the 3.3V source and its output feeds VDDCORE and the VDDPLL. Figure 5-1 shows the power schematics to be used for USB bus-powered systems.

Figure 5-1. 3.3V System Single Power Supply Schematic



5V-tolerant means that the I/O lines can drive voltage level according to VDDIO, but can be driven with a voltage of up to 5.5V. However, driving an I/O line with a voltage over VDDIO while the programmable pull-up resistor is enabled will create a current path through the pull-up resistor from the I/O line to VDDIO. Care should be taken, in particular at reset, as all the I/O lines default to input with pull-up resistor enabled at reset.

6.6 I/O Lines Current Drawing

The PIO lines PA0 to PA3 are high-drive current capable. Each of these I/O lines can drive up to 16 mA permanently.

The remaining I/O lines can draw only 8 mA.

However, the total current drawn by all the I/O lines cannot exceed 200 mA.

- Embedded Flash Controller
  - Embedded Flash interface, up to three programmable wait states
  - Prefetch buffer, buffering and anticipating the 16-bit requests, reducing the required wait states
  - Key-protected program, erase and lock/unlock sequencer
  - Single command for erasing, programming and locking operations
  - Interrupt generation in case of forbidden operation

7.4 Peripheral DMA Controller

- Handles data transfer between peripherals and memories
- Seventeen channels
  - Two for each USART
  - Two for the Debug Unit
  - Two for the Serial Synchronous Controller
  - Two for each Serial Peripheral Interface
  - Two for the Advanced Encryption Standard 128-bit accelerator
  - Two for the Triple Data Encryption Standard 128-bit accelerator
  - One for the Analog-to-digital Converter
- Low bus arbitration overhead
  - One Master Clock cycle needed for a transfer from memory to peripheral
  - Two Master Clock cycles needed for a transfer from peripheral to memory
- Next Pointer management for reducing interrupt latency requirements

Figure 8-1. AT91SAM7XC512/256/128 Memory Mapping

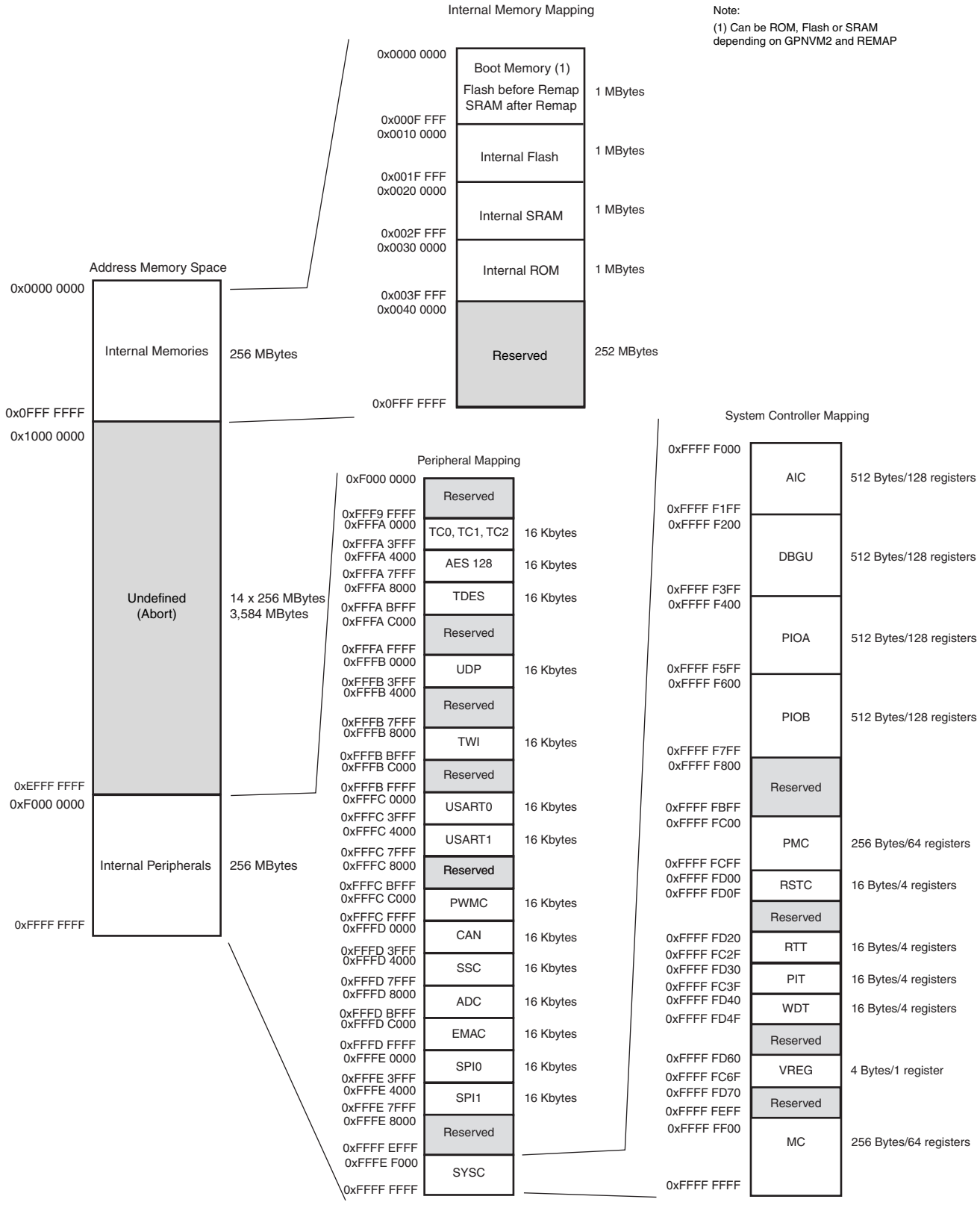
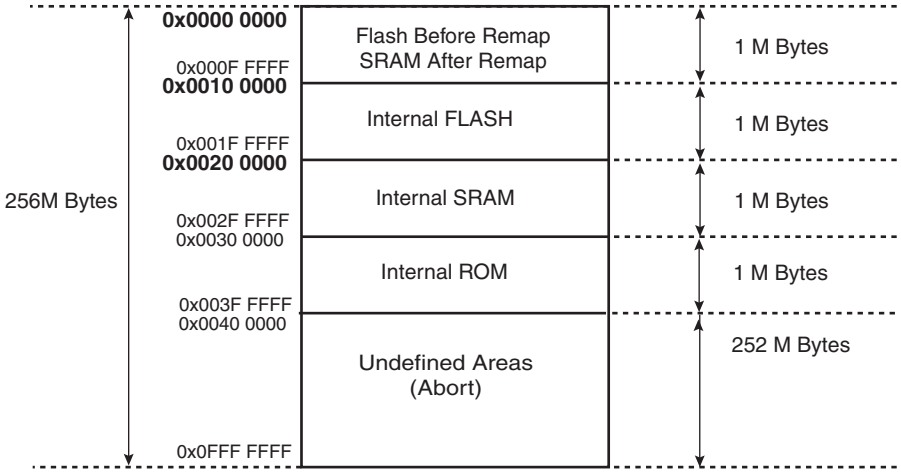


Figure 8-3. Internal Memory Mapping with GPNVM Bit 2 = 1



8.5 Embedded Flash

8.5.1 Flash Overview

- The Flash of the AT91SAM7XC512 is organized in two banks (dual plane) 0f 1254 pages of 256 bytes. The 524, 288 bytes are organized in 32-bit words.
- The Flash of the AT91SAM7XC256 is organized in 1024 pages of 256 bytes (single plane). It reads as 65,536 32-bit words.
- The Flash of the AT91SAM7XC128 is organized in 512 pages of 256 bytes (single plane). It reads as 32,768 32-bit words.

The Flash contains a 256-byte write buffer, accessible through a 32-bit interface.

The Flash benefits from the integration of a power reset cell and from the brownout detector. This prevents code corruption during power supply changes, even in the worst conditions.

When Flash is not used (read or write access), it is automatically placed into standby mode.

8.5.2 Embedded Flash Controller

The Embedded Flash Controller (EFC) manages accesses performed by the masters of the system. It enables reading the Flash and writing the write buffer. It also contains a User Interface, mapped within the Memory Controller on the APB. The User Interface allows:

- programming of the access parameters of the Flash (number of wait states, timings, etc.)
- starting commands such as full erase, page erase, page program, NVM bit set, NVM bit clear, etc.
- getting the end status of the last command
- getting error status
- programming interrupts on the end of the last commands or on errors

The Embedded Flash Controller also provides a dual 32-bit Prefetch Buffer that optimizes 16-bit access to the Flash. This is particularly efficient when the processor is running in Thumb mode.

Two EFCs are embedded in the AT91SAM7XC512 to control each bank of 256 KBytes. Dual-plane organization allows concurrent read and program functionality. Read from one memory

- Communication via the USB Device Port is limited to an 18.432 MHz crystal.

The SAM-BA Boot provides an interface with SAM-BA Graphic User Interface (GUI).

The SAM-BA Boot is in ROM and is mapped at address 0x0 when the GPNVM Bit 2 is set to 0.

When GPNVM bit 2 is set to 1, the device boots from the Flash.

When GPNVM bit 2 is set to 0, the device boots from ROM (SAM-BA).

9. System Controller

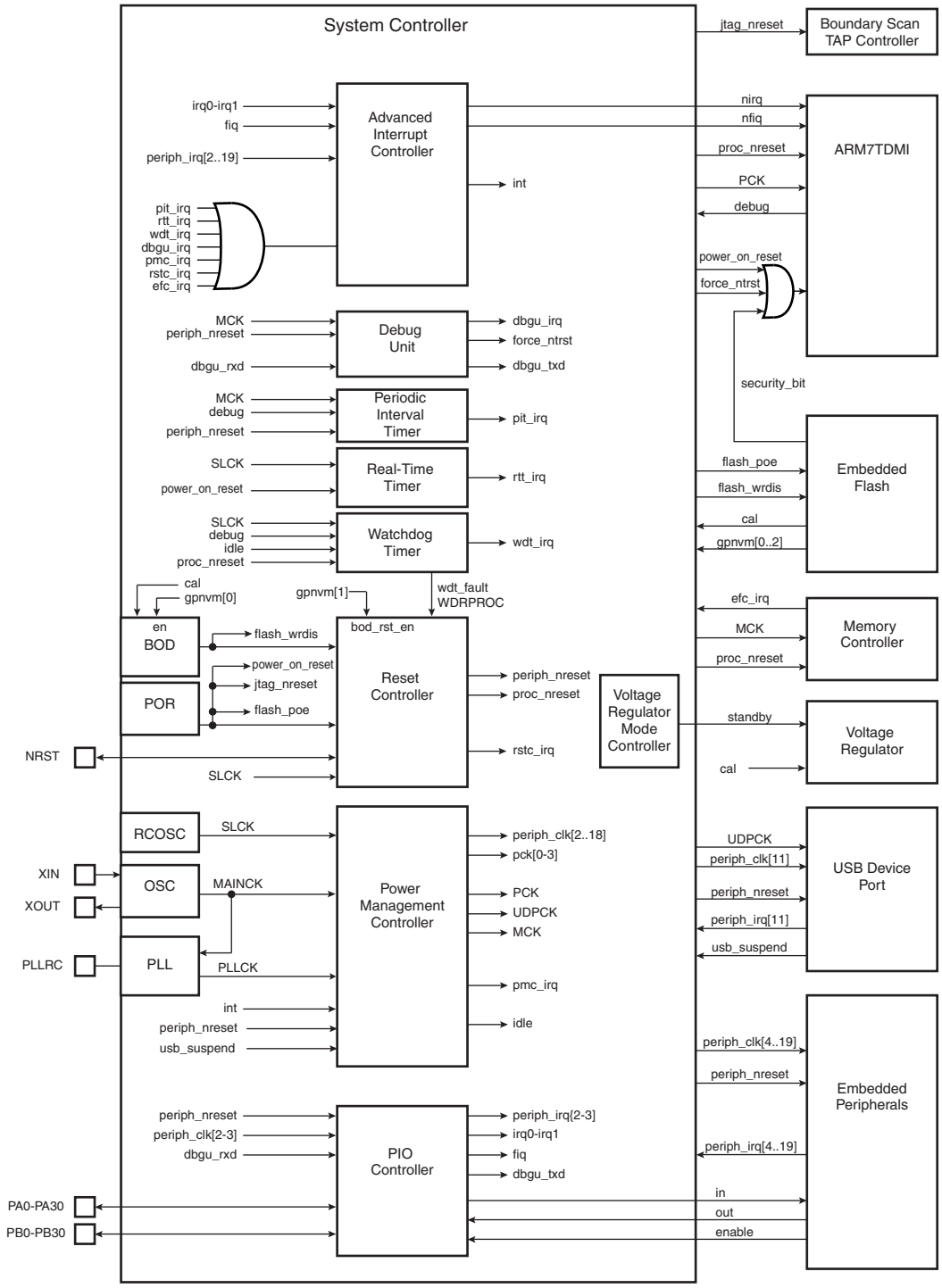
The System Controller manages all vital blocks of the microcontroller: interrupts, clocks, power, time, debug and reset.

The System Controller peripherals are all mapped to the highest 4 Kbytes of address space, between addresses 0xFFFF F000 and 0xFFFF FFFF.

Figure 9-1 on page 26 shows the System Controller Block Diagram.

Figure 8-1 on page 19 shows the mapping of the User Interface of the System Controller peripherals. Note that the Memory Controller configuration user interface is also mapped within this address space.

Figure 9-1. System Controller Block Diagram



9.1 Reset Controller

- Based on one power-on reset cell and one brownout detector
- Status of the last reset, either Power-up Reset, Software Reset, User Reset, Watchdog Reset, Brownout Reset
- Controls the internal resets and the NRST pin output
- Allows to shape a signal on the NRST line, guaranteeing that the length of the pulse meets any requirement.

9.1.1 Brownout Detector and Power-on Reset

The AT91SAM7XC512/256/128 embeds one brownout detection circuit and a power-on reset cell. The power-on reset is supplied with and monitors VDDCORE.

Both signals are provided to the Flash to prevent any code corruption during power-up or power-down sequences or if brownouts occur on the power supplies.

The power-on reset cell has a limited-accuracy threshold at around 1.5V. Its output remains low during power-up until VDDCORE goes over this voltage level. This signal goes to the reset controller and allows a full re-initialization of the device.

The brownout detector monitors the VDDCORE and VDDFLASH levels during operation by comparing them to a fixed trigger level. It secures system operations in the most difficult environments and prevents code corruption in case of brownout on the VDDCORE or VDDFLASH.

When the brownout detector is enabled and VDDCORE decreases to a value below the trigger level (Vbot18-, defined as Vbot18 - hyst/2), the brownout output is immediately activated.

When VDDCORE increases above the trigger level (Vbot18+, defined as Vbot18 + hyst/2), the reset is released. The brownout detector only detects a drop if the voltage on VDDCORE stays below the threshold voltage for longer than about 1µs.

The VDDCORE threshold voltage has a hysteresis of about 50 mV, to ensure spike free brownout detection. The typical value of the brownout detector threshold is 1.68V with an accuracy of ± 2% and is factory calibrated.

When the brownout detector is enabled and VDDFLASH decreases to a value below the trigger level (Vbot33-, defined as Vbot33 - hyst/2), the brownout output is immediately activated.

When VDDFLASH increases above the trigger level (Vbot33+, defined as Vbot33 + hyst/2), the reset is released. The brownout detector only detects a drop if the voltage on VDDCORE stays below the threshold voltage for longer than about 1µs.

The VDDFLASH threshold voltage has a hysteresis of about 50 mV, to ensure spike free brownout detection. The typical value of the brownout detector threshold is 2.80V with an accuracy of ± 3.5% and is factory calibrated.

The brownout detector is low-power, as it consumes less than 28 µA static current. However, it can be deactivated to save its static current. In this case, it consumes less than 1µA. The deactivation is configured through the GPNVM bit 0 of the Flash.

9.3 Power Management Controller

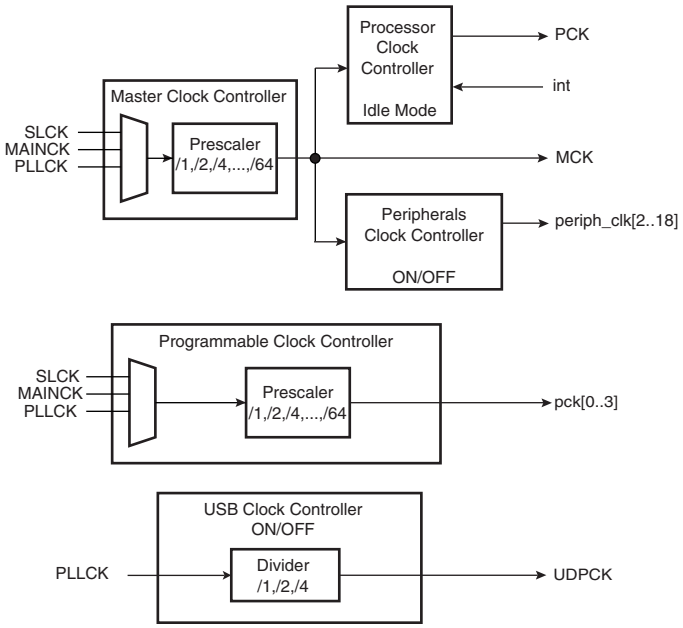
The Power Management Controller uses the Clock Generator outputs to provide:

- the Processor Clock PCK
- the Master Clock MCK
- the USB Clock UDPCK
- all the peripheral clocks, independently controllable
- four programmable clock outputs

The Master Clock (MCK) is programmable from a few hundred Hz to the maximum operating frequency of the device.

The Processor Clock (PCK) switches off when entering processor idle mode, thus allowing reduced power consumption while waiting for an interrupt.

Figure 9-3. Power Management Controller Block Diagram



9.4 Advanced Interrupt Controller

- Controls the interrupt lines (nIRQ and nFIQ) of an ARM Processor
- Individually maskable and vectored interrupt sources
  - Source 0 is reserved for the Fast Interrupt Input (FIQ)
  - Source 1 is reserved for system peripherals (RTT, PIT, EFC, PMC, DBGU, etc.)
  - Other sources control the peripheral interrupts or external interrupts
  - Programmable edge-triggered or level-sensitive internal sources
  - Programmable positive/negative edge-triggered or high/low level-sensitive external sources
- 8-level Priority Controller
  - Drives the normal interrupt nIRQ of the processor
  - Handles priority of the interrupt sources

10. Peripherals

10.1 User Interface

The User Peripherals are mapped in the 256 MBytes of address space between 0xF000 0000 and 0xFFFE FFFF. Each peripheral is allocated 16 Kbytes of address space.

A complete memory map is provided in Figure 8-1 on page 19.

10.2 Peripheral Identifiers

The AT91SAM7XC512/256/128 embeds a wide range of peripherals. Table 10-1 defines the Peripheral Identifiers of the AT91SAM7XC512/256/128. Unique peripheral identifiers are defined for both the Advanced Interrupt Controller and the Power Management Controller.

Table 10-1. Peripheral Identifiers

Peripheral ID	Peripheral Mnemonic	Peripheral Name	External Interrupt
0	AIC	Advanced Interrupt Controller	FIQ
1	SYSC(1)	System	
2	PIOA	Parallel I/O Controller A	
3	PIOB	Parallel I/O Controller B	
4	SPI0	Serial Peripheral Interface 0	
5	SPI1	Serial Peripheral Interface 1	
6	US0	USART 0	
7	US1	USART 1	
8	SSC	Synchronous Serial Controller	
9	TWI	Two-wire Interface	
10	PWMC	Pulse Width Modulation Controller	
11	UDP	USB device Port	
12	TC0	Timer/Counter 0	
13	TC1	Timer/Counter 1	
14	TC2	Timer/Counter 2	
15	CAN	CAN Controller	
16	EMAC	Ethernet MAC	
17	ADC(1)	Analog-to Digital Converter	
18	AES	Advanced Encryption Standard 128-bit	
19	TDES	Triple Data Encryption Standard	
20-29	Reserved		
30	AIC	Advanced Interrupt Controller	IRQ0
31	AIC	Advanced Interrupt Controller	IRQ1

Note: 1. Setting SYSC and ADC bits in the clock set/clear registers of the PMC has no effect. The System Controller and ADC are continuously clocked.

10.6 Ethernet MAC

- DMA Master on Receive and Transmit Channels
- Compatible with IEEE Standard 802.3
- 10 and 100 Mbit/s operation
- Full- and half-duplex operation
- Statistics Counter Registers
- MII/RMII interface to the physical layer
- Interrupt generation to signal receive and transmit completion
- 28-byte transmit FIFO and 28-byte receive FIFO
- Automatic pad and CRC generation on transmitted frames
- Automatic discard of frames received with errors
- Address checking logic supports up to four specific 48-bit addresses
- Support Promiscuous Mode where all valid received frames are copied to memory
- Hash matching of unicast and multicast destination addresses
- Physical layer management through MDIO interface
- Half-duplex flow control by forcing collisions on incoming frames
- Full-duplex flow control with recognition of incoming pause frames
- Support for 802.1Q VLAN tagging with recognition of incoming VLAN and priority tagged frames
- Multiple buffers per receive and transmit frame
- Jumbo frames up to 10240 bytes supported

10.7 Serial Peripheral Interface

- Supports communication with external serial devices
  - Four chip selects with external decoder allow communication with up to 15 peripherals
  - Serial memories, such as DataFlash® and 3-wire EEPROMs
  - Serial peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors
  - External co-processors
- Master or slave serial peripheral bus interface
  - 8- to 16-bit programmable data length per chip select
  - Programmable phase and polarity per chip select
  - Programmable transfer delays per chip select, between consecutive transfers and between clock and data
  - Programmable delay between consecutive transfers
  - Selectable mode fault detection
  - Maximum frequency at up to Master Clock

10.11 Timer Counter

- Three 16-bit Timer Counter Channels
  - Two output compare or one input capture per channel
- Wide range of functions including:
  - Frequency measurement
  - Event counting
  - Interval measurement
  - Pulse generation
  - Delay timing
  - Pulse Width Modulation
  - Up/down capabilities
- Each channel is user-configurable and contains:
  - Three external clock inputs
- Five internal clock inputs, as defined in Table 10-4

Table 10-4. Timer Counter Clocks Assignment

TC Clock input	Clock
TIMER_CLOCK1	MCK/2
TIMER_CLOCK2	MCK/8
TIMER_CLOCK3	MCK/32
TIMER_CLOCK4	MCK/128
TIMER_CLOCK5	MCK/1024

  - Two multi-purpose input/output signals
  - Two global registers that act on all three TC channels

10.12 Pulse Width Modulation Controller

- Four channels, one 16-bit counter per channel
- Common clock generator, providing thirteen different clocks
  - One Modulo n counter providing eleven clocks
  - Two independent linear dividers working on modulo n counter outputs
- Independent channel programming
  - Independent enable/disable commands
  - Independent clock selection
  - Independent period and duty cycle, with double buffering
  - Programmable selection of the output waveform polarity
  - Programmable center or left aligned output waveform

  - Automatic wakeup on trigger and back to sleep mode after conversions of all enabled channels
- Four of eight analog inputs shared with digital signals

12. AT91SAM7XC512/256/128 Ordering Information

Table 12-1. Ordering Information

MLR A Ordering Code	MLR B Ordering Code	Package	Package Type	Temperature Operating Range
AT91SAM7XC512-AU AT91SAM7XC512-CU	–	LQFP 100 TFBGA 100	Green	Industrial (-40· C to 85· C)
AT91SAM7XC256-AU AT91SAM7XC256-CU	AT91SAM7XC256B-AU AT91SAM7XC256B-CU	LQFP 100 TFBGA 100	Green	Industrial (-40· C to 85· C)
AT91SAM7XC128-AU AT91SAM7XC128-CU	AT91SAM7XC128B-AU AT91SAM7XC128B-CU	LQFP 100 TFBGA 100	Green	Industrial (-40· C to 85· C)

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