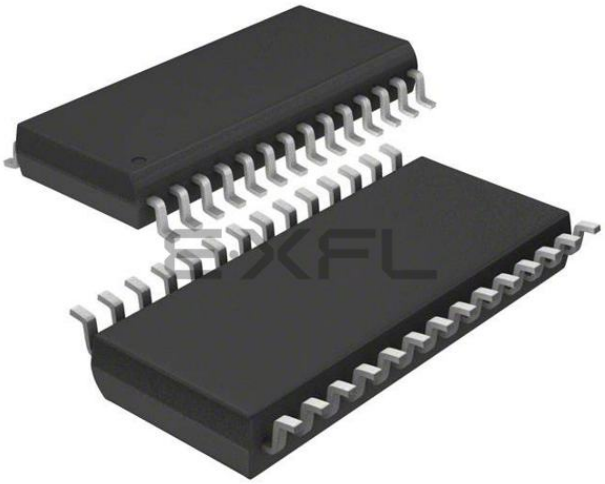
Infineon Technologies - CY8C24423A-12PVXET Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	12MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	24
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.25V
Data Converters	A/D 12x14b; D/A 2x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c24423a-12pvxet

Contents

PSoC Functional Overview

The PSoC family consists of many programmable system-on-chips with on-chip Controller devices. These devices are designed to replace multiple traditional microcontroller unit (MCU)-based system components with one, low cost single-chip programmable device. PSoC devices include configurable blocks of analog and digital logic, and programmable interconnects. This architecture enables the user to create customized peripheral configurations that match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts and packages.

The PSoC architecture, as shown in the Logic Block Diagram on page 1, is comprised of four main areas: PSoC Core, Digital System, Analog System, and System Resources. Configurable global buses allow all the device resources to be combined into a complete custom system. Each CY8C24x23A PSoC device includes four digital blocks and six analog blocks. Depending on the PSoC package, up to 24 GPIO are also included. The GPIO provide access to the global digital and analog interconnects.

PSoC Core

The PSoC Core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable GPIO.

The M8C CPU core is a powerful processor with speeds up to 12 MHz, providing a two MIPS 8-bit Harvard architecture microprocessor. The CPU uses an interrupt controller with multiple vectors, to simplify programming of real time embedded events. Program execution is timed and protected using the included Sleep Timer and Watchdog Timer (WDT).

Memory includes 4 KB of Flash for program storage and 256 bytes of SRAM for data storage. Program Flash uses four protection levels on blocks of 64 bytes, allowing customized software IP protection.

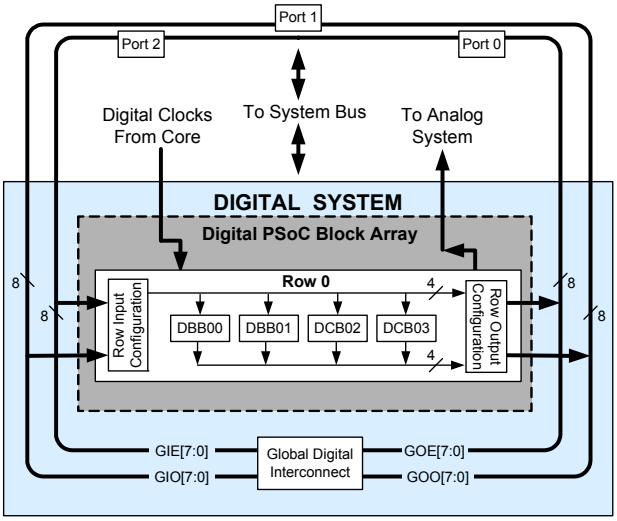
The PSoC device incorporates flexible internal clock generators, including a 24 MHz IMO (internal main oscillator) accurate to ±4% over temperature and voltage. A low power 32 kHz internal low speed oscillator (ILO) is provided for the Sleep Timer and WDT. If crystal accuracy is desired, the ECO (32.768 kHz external crystal oscillator) is available for use as a Real Time Clock (RTC) and can optionally generate a crystal-accurate 24 MHz system clock using a PLL. The clocks, together with programmable clock dividers (as a System Resource), provide the flexibility to integrate almost any timing requirement into the PSoC device.

PSoC GPIOs provide connection to the CPU, digital, and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt.

Digital System

The Digital System is composed of four digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user modules.

Figure 1. Digital System Block Diagram



Digital peripheral configurations include:

- PWMs (8- and 16-bit)
- PWMs with Dead Band (8- and 16-bit)
- Counters (8 to 32 bit)
- Timers (8 to 32 bit)
- Full or Half-Duplex 8-bit UART with selectable parity
- SPI master and slave
- I^2C master, slave, or multi-master
- Cyclical Redundancy Checker/Generator (16 bit)
- IrDA
- Pseudo Random Sequence Generators (8 to 32 bit)

The digital blocks can be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This allows the optimum choice of system resources for your application. Family resources are shown in Table 1 on page 5.

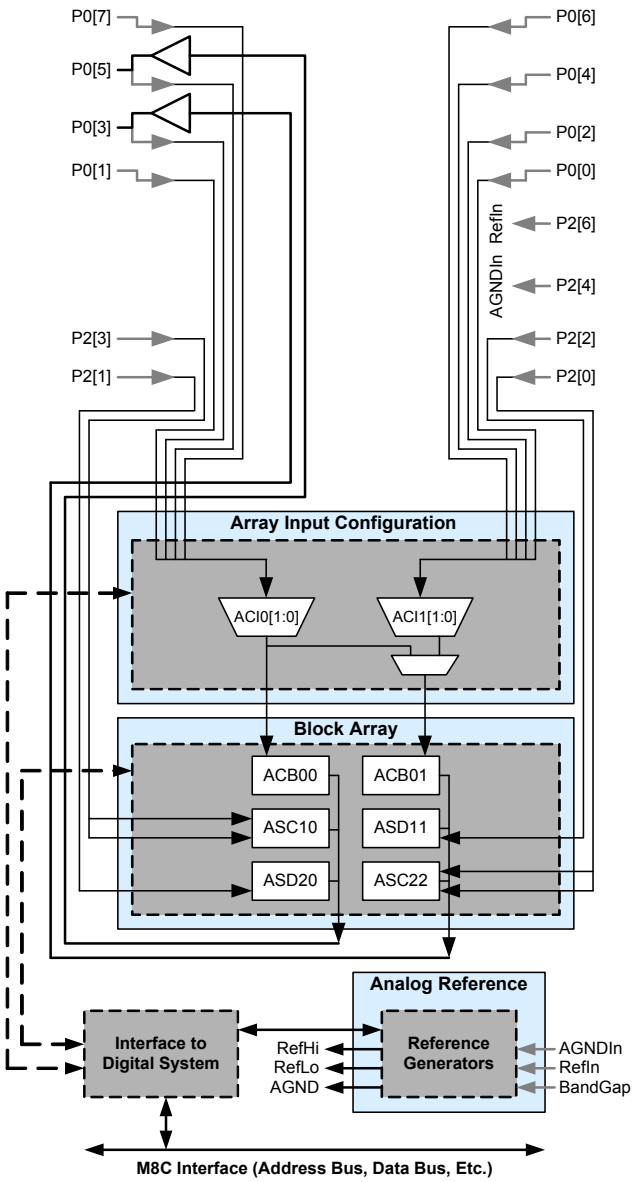
Analog System

The Analog System is composed of six configurable blocks, each comprised of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the common PSoC analog functions for this device (most available as user modules) are:

- ADCs (up to two, with 6 to 14-bit resolution, selectable as Incremental, Delta-Sigma, and SAR)
- Filters (two and four pole band-pass, low-pass, and notch)
- Amplifiers (up to two, with selectable gain up to 48x)
- Instrumentation amplifiers (one with selectable gain up to 93x)
- Comparators (up to two, with 16 selectable thresholds)
- DACs (up to two, with 6 to 9-bit resolution)
- Multiplying DACs (up to two, with 6 to 9-bit resolution)
- High current output drivers (two with 30 mA drive)
- 1.3V reference (as a System Resource)
- DTMF Dialer
- Modulators
- Correlators
- Peak Detectors
- Many other topologies possible

Analog blocks are arranged in a column of three, which includes one Continuous Time (CT) and two Switched Capacitor (SC) blocks, as shown in Figure 2.

Figure 2. Analog System Block Diagram



Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is summarized in four steps:

1. Select User Modules.
2. Configure User Modules.
3. Organize and Connect.
4. Generate, Verify, and Debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run-time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in either C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events. These include monitoring address and data bus values, memory locations, and external signals.

Pinouts

The automotive CY8C24x23A PSoC device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of Digital I/O. However, Vss, Vdd, and XRES are not capable of Digital I/O.

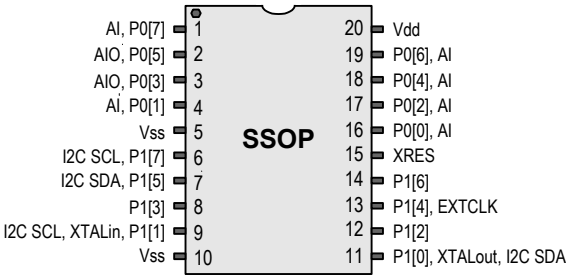
20-Pin Part Pinout

Table 3. 20-Pin Part Pinout (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P0[7]	Analog column mux input
2	I/O	I/O	P0[5]	Analog column mux input and column output
3	I/O	I/O	P0[3]	Analog column mux input and column output
4	I/O	I	P0[1]	Analog column mux input
5	Power		Vss	Ground connection
6	I/O		P1[7]	I^2C Serial Clock (SCL)
7	I/O		P1[5]	I^2C Serial Data (SDA)
8	I/O		P1[3]	
9	I/O		P1[1]	Crystal Input (XTALin), I^2C Serial Clock (SCL), ISSP-SCLK[5]
10	Power		Vss	Ground connection
11	I/O		P1[0]	Crystal Output (XTALout), I^2C Serial Data (SDA), ISSP-SDATA[5]
12	I/O		P1[2]	
13	I/O		P1[4]	Optional External Clock Input (EXTCLK)
14	I/O		P1[6]	
15	Input		XRES	Active high external reset with internal pull down
16	I/O	I	P0[0]	Analog column mux input
17	I/O	I	P0[2]	Analog column mux input
18	I/O	I	P0[4]	Analog column mux input
19	I/O	I	P0[6]	Analog column mux input
20	Power		Vdd	Supply voltage

LEGEND: A = Analog, I = Input, and O = Output.

Figure 3. CY8C24223A 20-Pin PSoC Device



Note
5. These are the ISSP pins, which are not High Z when coming out of POR (Power On Reset). See the *PSoC Technical Reference Manual* for details.

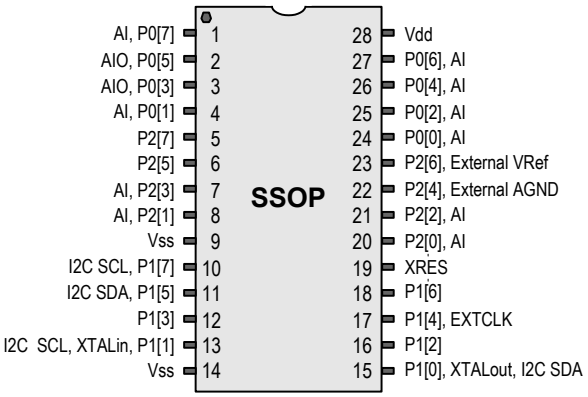
28-Pin Part Pinout

Table 4. 28-Pin Part Pinout (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P0[7]	Analog column mux input
2	I/O	I/O	P0[5]	Analog column mux input and column output
3	I/O	I/O	P0[3]	Analog column mux input and column output
4	I/O	I	P0[1]	Analog column mux input
5	I/O		P2[7]	
6	I/O		P2[5]	
7	I/O	I	P2[3]	Direct switched capacitor block input
8	I/O	I	P2[1]	Direct switched capacitor block input
9	Power		Vss	Ground connection
10	I/O		P1[7]	I^2C Serial Clock (SCL)
11	I/O		P1[5]	I^2C Serial Data (SDA)
12	I/O		P1[3]	
13	I/O		P1[1]	Crystal Input (XTALin), I^2C Serial Clock (SCL), ISSP-SCLK[5]
14	Power		Vss	Ground connection
15	I/O		P1[0]	Crystal Output (XTALout), I^2C Serial Data (SDA), ISSP-SDATA[5]
16	I/O		P1[2]	
17	I/O		P1[4]	Optional External Clock Input (EXTCLK)
18	I/O		P1[6]	
19	Input		XRES	Active high external reset with internal pull down
20	I/O	I	P2[0]	Direct switched capacitor block input
21	I/O	I	P2[2]	Direct switched capacitor block input
22	I/O		P2[4]	External Analog Ground (AGND)
23	I/O		P2[6]	External Voltage Reference (VRef)
24	I/O	I	P0[0]	Analog column mux input
25	I/O	I	P0[2]	Analog column mux input
26	I/O	I	P0[4]	Analog column mux input
27	I/O	I	P0[6]	Analog column mux input
28	Power		Vdd	Supply voltage

LEGEND: A = Analog, I = Input, and O = Output.

Figure 4. CY8C24423A 28-Pin PSoC Device



Registers

Register Conventions

This section lists the registers of the automotive CY8C24x23A PSoC device. For detailed register information, refer to the *PSoC Technical Reference Manual*.

The register conventions specific to this section are listed in the following table.

Table 5. Abbreviations

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks. The XIO bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XIO bit is set the user is in Bank 1.

Note In the following register mapping tables, blank fields are Reserved and must not be accessed.

Table 6. Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40		ASC10CR0	80	RW		C0	
PRT0IE	01	RW		41		ASC10CR1	81	RW		C1	
PRT0GS	02	RW		42		ASC10CR2	82	RW		C2	
PRT0DM2	03	RW		43		ASC10CR3	83	RW		C3	
PRT1DR	04	RW		44		ASD11CR0	84	RW		C4	
PRT1IE	05	RW		45		ASD11CR1	85	RW		C5	
PRT1GS	06	RW		46		ASD11CR2	86	RW		C6	
PRT1DM2	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DR	08	RW		48			88			C8	
PRT2IE	09	RW		49			89			C9	
PRT2GS	0A	RW		4A			8A			CA	
PRT2DM2	0B	RW		4B			8B			CB	
	0C			4C			8C			CC	
	0D			4D			8D			CD	
	0E			4E			8E			CE	
	0F			4F			8F			CF	
	10			50		ASD20CR0	90	RW		D0	
	11			51		ASD20CR1	91	RW		D1	
	12			52		ASD20CR2	92	RW		D2	
	13			53		ASD20CR3	93	RW		D3	
	14			54		ASC21CR0	94	RW		D4	
	15			55		ASC21CR1	95	RW		D5	
	16			56		ASC21CR2	96	RW	I2C_CFG	D6	RW
	17			57		ASC21CR3	97	RW	I2C_SCR	D7	#
	18			58			98		I2C_DR	D8	RW
	19			59			99		I2C_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C			DC	
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F			DF	
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W		61			A1		INT_MSK1	E1	RW
DBB00DR2	22	RW		62			A2		INT_VC	E2	RC
DBB00CR0	23	#	ARF_CR	63	RW		A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4		DEC_DH	E4	RC
DBB01DR1	25	W	ASY_CR	65	#		A5		DEC_DL	E5	RC
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCB02DR0	28	#		68			A8		MUL_X	E8	W
DCB02DR1	29	W		69			A9		MUL_Y	E9	W
DCB02DR2	2A	RW		6A			AA		MUL_DH	EA	R
DCB02CR0	2B	#		6B			AB		MUL_DL	EB	R
DCB03DR0	2C	#		6C			AC		ACC_DR1	EC	RW
DCB03DR1	2D	W		6D			AD		ACC_DR0	ED	RW
DCB03DR2	2E	RW		6E			AE		ACC_DR3	EE	RW
DCB03CR0	2F	#		6F			AF		ACC_DR2	EF	RW
	30		ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
	31		ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
	32		ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34		ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
	35		ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
	36		ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and must not be accessed. # Access is bit specific.

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 9. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage Temperature	-55	+25	+125	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25°C ± 25°C. Storage temperatures above 65°C degrades reliability. Maximum combined storage and operational time at +125°C is 7000 hours.
$T_{BAKETEMP}$	Bake Temperature	–	125	See package label	°C	
$T_{BAKETIME}$	Bake Time	See package label	–	72	Hours	
T_A	Ambient Temperature with Power Applied	-40	–	+125	°C	
Vdd	Supply Voltage on Vdd Relative to Vss	-0.5	–	+6.0	V	
V_{IO}	DC Input Voltage	Vss - 0.5	–	Vdd + 0.5	V	
V_{IOZ}	DC Voltage Applied to Tri-state	Vss - 0.5	–	Vdd + 0.5	V	
I_{MIO}	Maximum Current into any Port Pin	-25	–	+25	mA	
ESD	Electro Static Discharge Voltage	2000	–	–	V	Human Body Model ESD.
LU	Latch up Current	–	–	200	mA	

Operating Temperature

Table 10. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient Temperature	-40	–	+125	°C	
T_J	Junction Temperature	-40	–	+135	°C	The temperature rise from ambient to junction is package specific. See Thermal Impedances on page 29. The user must limit the power consumption to comply with this requirement.

DC Electrical Characteristics

DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 11. DC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
Vdd	Supply Voltage	4.75	–	5.25	V	See table titled DC POR and LVD Specifications on page 20
I_{DD}	Supply Current	–	5	8	mA	Conditions are Vdd = 5.25V, -40°C ≤ T_A ≤ 125°C, CPU = 3 MHz, 48 MHz disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz, Analog power = off.
I_{SB}	Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT.[6]	–	4	13	µA	Conditions are with internal low speed oscillator active, Vdd = 5.25V, -40°C ≤ T_A ≤ 55°C. Analog power = off.
I_{SBH}	Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT at high temperature.[6]	–	4	100	µA	Conditions are with internal slow speed oscillator active, Vdd = 5.25V, 55°C < T_A ≤ 125°C. Analog power = off.
I_{SBXTL}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and external crystal.[6]	–	6	15	µA	Conditions are with properly loaded, 1 µW max, 32.768 kHz crystal. Vdd = 5.25V, -40°C ≤ T_A ≤ 55°C. Analog power = off.
I_{SBXTLH}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and external crystal at high temperature.[6]	–	6	100	µA	Conditions are with properly loaded, 1µW max, 32.768 kHz crystal. Vdd = 5.25V, 55°C < T_A ≤ 125°C. Analog power = off.
V_{REF}	Reference Voltage (Bandgap)	1.25	1.3	1.35	V	Trimmed for appropriate Vdd.

DC General Purpose I/O Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance.

Table 12. DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull up Resistor	4	5.6	8	kΩ	
R_{PD}	Pull down Resistor	4	5.6	8	kΩ	
V_{OH}	High Output Level	3.5	–	–	V	I_{OH} = 10 mA, Vdd = 4.75 to 5.25V (maximum 40 mA on even port pins (for example, P0[2], P1[4]), maximum 40 mA on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined I_{OH} budget.
V_{OL}	Low Output Level	–	–	0.75	V	I_{OL} = 25 mA, Vdd = 4.75 to 5.25V (maximum 100 mA on even port pins (for example, P0[2], P1[4]), maximum 100 mA on odd port pins (for example, P0[3], P1[5])). 150 mA maximum combined I_{OL} budget.
I_{OH}	High Level Source Current	10	–	–	mA	V_{OH} ≥ Vdd-1.0V, see the limitations of the total current in the note for V_{OH}.
I_{OL}	Low Level Sink Current	25	–	–	mA	V_{OL} ≤ 0.75V, see the limitations of the total current in the note for V_{OL}.
V_{IL}	Input Low Level	–	–	0.8	V	

Note
6. Standby current includes all functions (POR, LVD, WDT, Sleep Timer) needed for reliable system operation. This must be compared with devices that have similar functions enabled.

Table 12. DC GPIO Specifications (continued)

Symbol	Description	Min	Typ	Max	Units	Notes
V_{IH}	Input High Level	2.1	–		V	
V_H	Input Hysterisis	–	60	–	mV	
I_{IL}	Input Leakage (Absolute Value)	–	1	–	nA	Gross tested to 1 μA
C_{IN}	Capacitive Load on Pins as Input	–	3.5	10	pF	Package and pin dependent. Temp = 25°C
C_{OUT}	Capacitive Load on Pins as Output	–	3.5	10	pF	Package and pin dependent. Temp = 25°C

DC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

The Operational Amplifier is a component of both the Analog Continuous Time (CT) PSoC blocks and the Analog Switched Capacitor (SC) PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time (CT) PSoC blocks.

Table 13. DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (absolute value) Low Power Input Offset Voltage (absolute value) Mid Power Input Offset Voltage (absolute value) High Power	– – –	1.6 1.3 1.2	11 9 9	mV mV mV	
TCV_{OSOA}	Input Offset Voltage Drift	–	7.0	35.0	μV/°C	
I_{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	200	–	pA	Gross tested to 1 μA
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C.
V_{CMOA}	Common Mode Voltage Range Common Mode Voltage Range (high power or high opamp bias)	0.0 0.5	– –	Vdd Vdd - 0.5	V –	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open Loop Gain Power = Low Power = Medium Power = High	 – – –	 80 80 80	 – – –	 dB dB dB	Specification is applicable at high power. For all other bias modes (except high power, high opamp bias), minimum is 60 dB.
$V_{OHIGHOA}$	High Output Voltage Swing (worst case internal load) Power = Low Power = Medium Power = High	 Vdd - 0.2 Vdd - 0.2 Vdd - 0.5	 – – –	 – – –	 V V V	
V_{OLOWOA}	Low Output Voltage Swing (worst case internal load) Power = Low Power = Medium Power = High	 – – –	 – – –	 0.2 0.2 0.5	 V V V	
I_{SOA}	Supply Current (including associated AGND buffer) Power = Low, Opamp Bias = Low Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = Low Power = High, Opamp Bias = High	 – – – – – –	 150 300 600 1200 2400 4600	 200 400 800 1600 3200 6400	 μA μA μA μA μA μA	
$PSRR_{OA}$	Supply Voltage Rejection Ratio	–	80	–	dB	Vss ≤ VIN ≤ (Vdd - 2.25) or (Vdd - 1.25V) ≤ VIN ≤ Vdd

AC Electrical Characteristics

AC Chip-Level Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 20. AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO24}	Internal Main Oscillator Frequency for 24 MHz	23.04[12]	24	24.96[12]	MHz	Trimmed using factory trim values.
F_{CPU1}	CPU Frequency (5V Vdd Nominal)	0.09[12]	12	12.48[12]	MHz	
F_{24M}	Digital PSoC Block Frequency	0	24	24.96[12, 13]	MHz	
F_{32K1}	Internal Low Speed Oscillator Frequency	15	32	64	kHz	This specification applies when the ILO has been trimmed.
F_{32KU}	Internal Low Speed Oscillator (ILO) Untrimmed Frequency	5	–	–	kHz	After a reset and before the M8C processor starts to execute, the ILO is not trimmed.
F_{32K2}	External Crystal Oscillator	–	32.768	–	kHz	Accuracy is capacitor and crystal dependent. 50% duty cycle.
F_{PLL}	PLL Frequency	–	23.986	–	MHz	A multiple (x732) of crystal frequency.
Jitter24M2	24 MHz Period Jitter (PLL)	–	–	800	ps	Refer to Figure 9 on page 22.
$T_{PLLSLEW}$	PLL Lock Time	0.5	–	10	ms	Refer to Figure 6 on page 22.
$T_{PLLSLEWSLOW}$	PLL Lock Time for Low Gain Setting	0.5	–	50	ms	Refer to Figure 7 on page 22.
T_{OS}	External Crystal Oscillator Startup to 1%	–	1700	2620	ms	Refer to Figure 8 on page 22.
T_{OSACC}	External Crystal Oscillator Startup to 100 ppm	–	2800	3800	ms	
Jitter32k	32 kHz Period Jitter	–	100	–	ns	Refer to Figure 10 on page 22.
T_{XRST}	External Reset Pulse Width	10	–	–	µs	
DC24M	24 MHz Duty Cycle	40	50	60	%	
DC_{ILO}	Internal Low Speed Oscillator (ILO) Duty Cycle	20	50	80	%	
Step24M	24 MHz Trim Step Size	–	50	–	kHz	
Jitter24M1P	24 MHz Period Jitter (IMO) Peak-to-Peak	–	600	–	ps	Refer to Figure 9 on page 22.
Jitter24M1R	24 MHz Period Jitter (IMO) Root Mean Squared	–	–	600	ps	
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.48[12]	MHz	
$SR_{POWERUP}$	Power Supply Slew Rate	–	–	250	V/ms	Vdd slew rate during power up.
$T_{POWERUP}$	Time between end of POR state and CPU code execution	–	16	100	ms	Power up from 0V.

Notes
12. Accuracy derived from Internal Main Oscillator with appropriate trim for Vdd range.
13. See the individual user module data sheets for information on maximum frequencies for user modules.

Figure 6. PLL Lock Timing Diagram

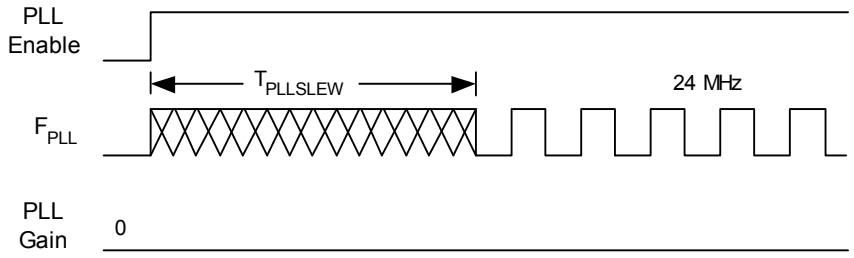


Figure 7. PLL Lock for Low Gain Setting Timing Diagram

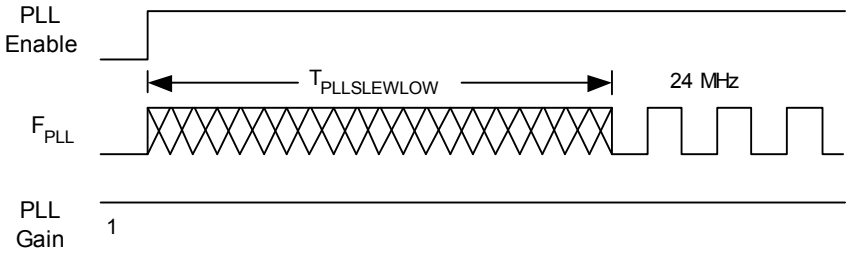


Figure 8. External Crystal Oscillator Startup Timing Diagram

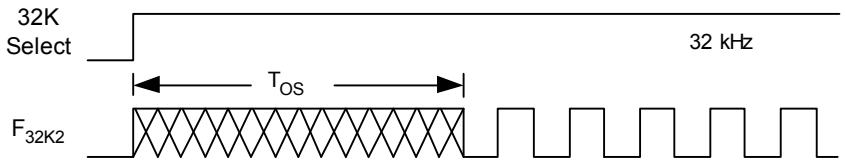


Figure 9. 24 MHz Period Jitter (IMO) Timing Diagram

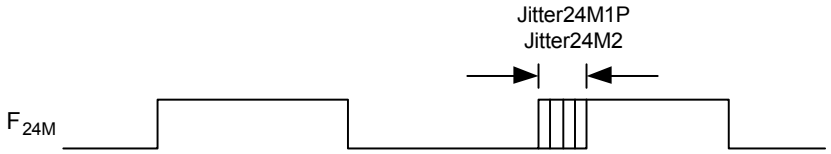
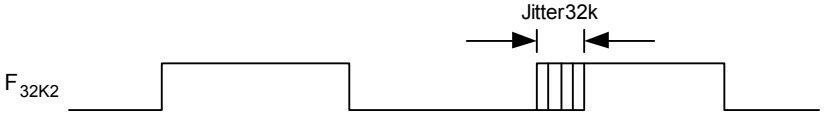


Figure 10. 32 kHz Period Jitter (ECO) Timing Diagram



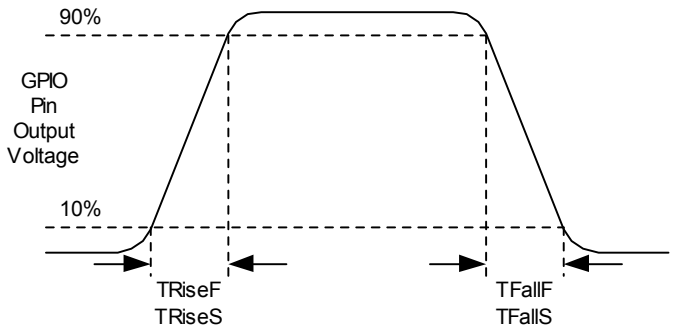
AC General Purpose I/O Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 21. AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO Operating Frequency	0	–	12.48[12]	MHz	Normal Strong Mode
TRiseF	Rise Time, Normal Strong Mode, Cload = 50 pF	2	–	22	ns	10% - 90%
TFallF	Fall Time, Normal Strong Mode, Cload = 50 pF	2	–	22	ns	10% - 90%
TRiseS	Rise Time, Slow Strong Mode, Cload = 50 pF	9	27	–	ns	10% - 90%
TFallS	Fall Time, Slow Strong Mode, Cload = 50 pF	9	22	–	ns	10% - 90%

Figure 11. GPIO Timing Diagram



AC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Note Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

Table 22. AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units
SR_{ROA}	Rising Slew Rate (20% to 80%) (10 pF load, Unity Gain)				
	Power = Low, Opamp Bias = Low	0.15	–	–	V/µs
	Power = Low, Opamp Bias = High	0.15	–	–	V/µs
	Power = Medium, Opamp Bias = Low	0.15	–	–	V/µs
	Power = Medium, Opamp Bias = High	1.7	–	–	V/µs
	Power = High, Opamp Bias = Low	1.7	–	–	V/µs
	Power = High, Opamp Bias = High	6.5	–	–	V/µs
SR_{FOA}	Falling Slew Rate (80% to 20%) (10 pF load, Unity Gain)				
	Power = Low, Opamp Bias = Low	0.01	–	–	V/µs
	Power = Low, Opamp Bias = High	0.01	–	–	V/µs
	Power = Medium, Opamp Bias = Low	0.01	–	–	V/µs
	Power = Medium, Opamp Bias = High	0.5	–	–	V/µs
	Power = High, Opamp Bias = Low	0.5	–	–	V/µs
	Power = High, Opamp Bias = High	4.0	–	–	V/µs
BW_{OA}	Gain Bandwidth Product				
	Power = Low, Opamp Bias = Low	0.75	–	–	MHz
	Power = Low, Opamp Bias = High	0.75	–	–	MHz
	Power = Medium, Opamp Bias = Low	0.75	–	–	MHz
	Power = Medium, Opamp Bias = High	3.1	–	–	MHz
	Power = High, Opamp Bias = Low	3.1	–	–	MHz
	Power = High, Opamp Bias = High	5.4	–	–	MHz

AC Low Power Comparator Specifications

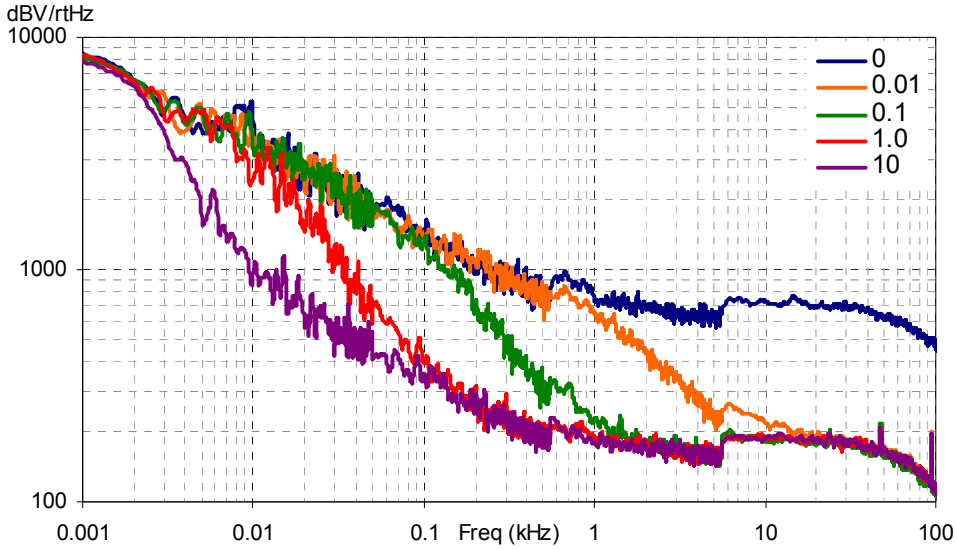
The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 23. AC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RLPC}	LPC response time	–	–	50	µs	≥ 50 mV overdrive comparator reference set within V_{REFLPC}.

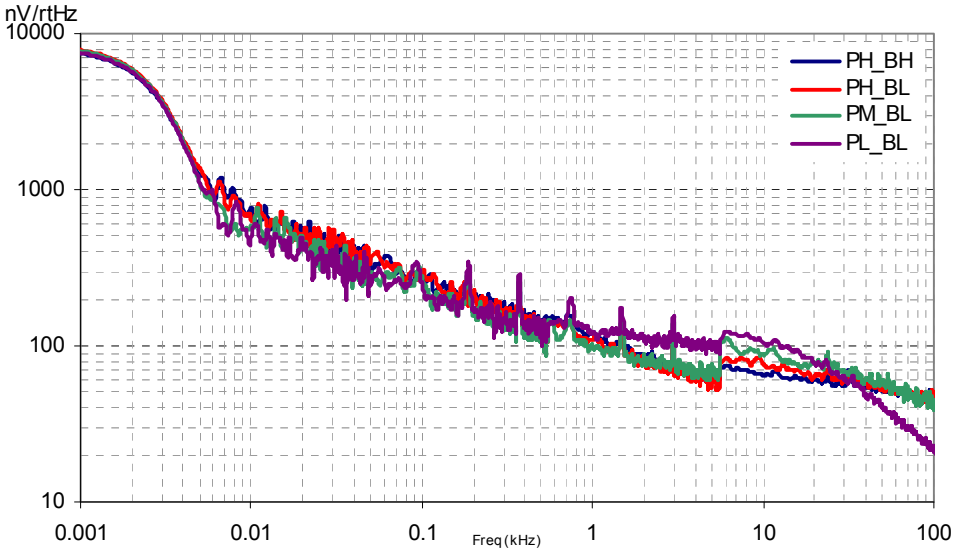
When bypassed by a capacitor on P2[4], the noise of the analog ground signal distributed to each block is reduced by a factor of up to 5 (14 dB). This is at frequencies above the corner frequency defined by the on-chip 8.1k resistance and the external capacitor.

Figure 12. Typical AGND Noise with P2[4] Bypass



At low frequencies, the opamp noise is proportional to 1/f, power independent, and determined by device geometry. At high frequencies, increased power level reduces the noise spectrum level.

Figure 13. Typical Opamp Noise



AC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 25. AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units
T_{ROB}	Rising Settling Time to 0.1%, 1V Step, 100 pF Load Power = Low Power = High	 – –	 – –	 3 3	 µs µs
T_{SOB}	Falling Settling Time to 0.1%, 1V Step, 100 pF Load Power = Low Power = High	 – –	 – –	 3 3	 µs µs
SR_{ROB}	Rising Slew Rate (20% to 80%), 1V Step, 100 pF Load Power = Low Power = High	 0.6 0.6	 – –	 – –	 V/µs V/µs
SR_{FOB}	Falling Slew Rate (80% to 20%), 1V Step, 100 pF Load Power = Low Power = High	 0.6 0.6	 – –	 – –	 V/µs V/µs
BW_{OB}	Small Signal Bandwidth, 20mV_{pp}, 3dB BW, 100 pF Load Power = Low Power = High	 0.8 0.8	 – –	 – –	 MHz MHz
BW_{OB}	Large Signal Bandwidth, 1V_{pp}, 3dB BW, 100 pF Load Power = Low Power = High	 300 300	 – –	 – –	 kHz kHz

AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 26. AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency	0.093	–	24.24	MHz	
–	High Period	20.6	–	–	ns	
–	Low Period	20.6	–	–	ns	
–	Power Up IMO to Switch	150	–	–	µs	

AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 125°C. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 27. AC Programming Specifications

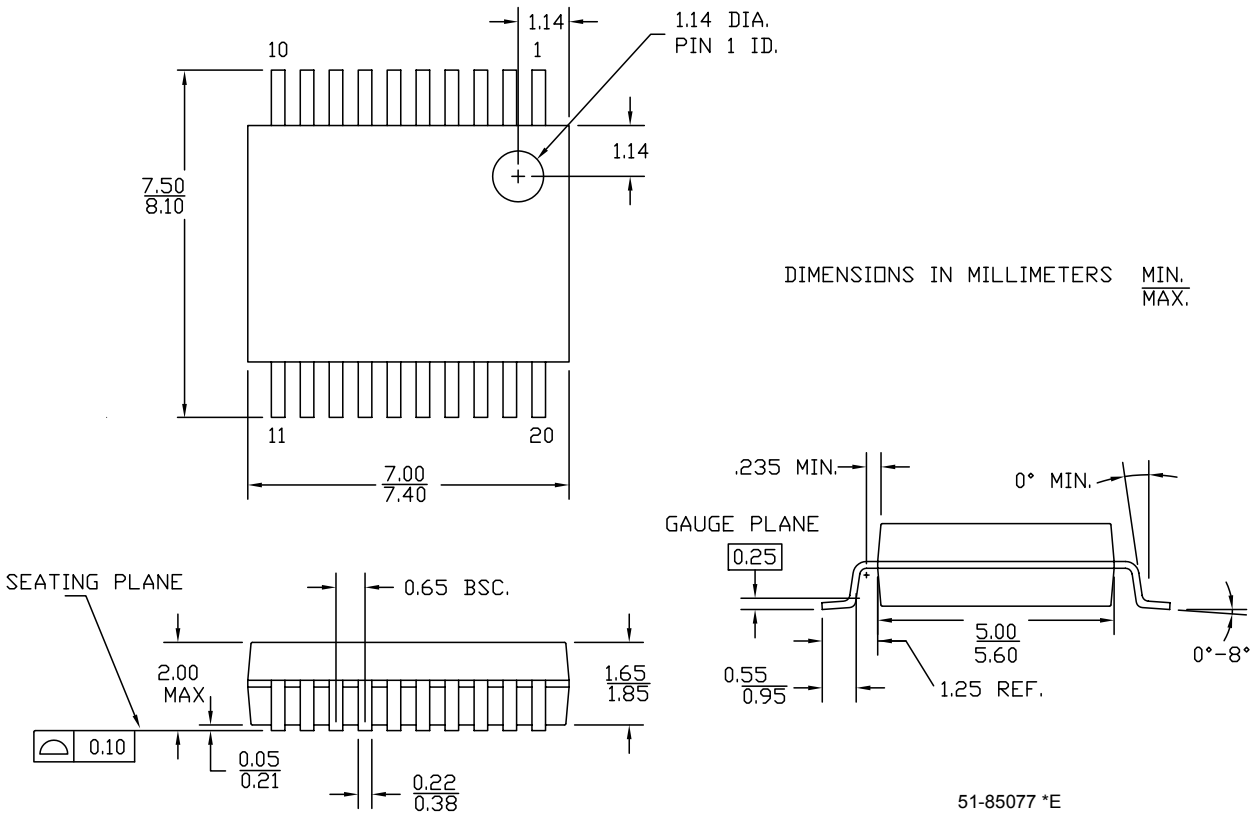
Symbol	Description	Min	Typ	Max	Units	Notes
T_{RSCLK}	Rise Time of SCLK	1	–	20	ns	
T_{FSCLK}	Fall Time of SCLK	1	–	20	ns	
T_{SSCLK}	Data Set up Time to Falling Edge of SCLK	40	–	–	ns	
T_{HSCLK}	Data Hold Time from Falling Edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
T_{ERASEB}	Flash Erase Time (Block)	–	20	80[9]	ms	
T_{WRITE}	Flash Block Write Time	–	80	320[9]	ms	
T_{DSCLK}	Data Out Delay from Falling Edge of SCLK	–	–	50	ns	
T_{PRGH}	Total Flash Block Program Time (T_{ERASEB} + T_{WRITE}), Hot	–	–	200[9]	ms	$T_J \geq 0°C$
T_{PRGC}	Total Flash Block Program Time (T_{ERASEB} + T_{WRITE}), Cold	–	–	400[9]	ms	$T_J < 0°C$

Packaging Information

This section illustrates the packaging specifications for the automotive CY8C24x23A PSoC device, along with the thermal impedances for each package and the typical package capacitance on crystal pins.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the emulator pod drawings at http://www.cypress.com.

Figure 15. 20-Pin (210-Mil) SSOP



Device Programmers

All device programmers can be purchased from the Cypress Online Store.

CY3210-MiniProg1

The CY3210-MiniProg1 kit allows a user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.

Note: CY3207ISSP needs special software and is not compatible with PSoC Programmer. This software is free and can be downloaded from http://www.cypress.com. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

Accessories (Emulation and Programming)

Table 29. Emulation and Programming Accessories

Part Number	Pin Package	Pod Kit[18]	Foot Kit[19]	Adapter[20]
CY8C24223A-12PVXE	20 SSOP	CY3250-24X23A	CY3250-20SSOP-FK	Adapters can be found at http://www.emulation.com.
CY8C24423A-12PVXE	28 SSOP	CY3250-24X23A	CY3250-28SSOP-FK	

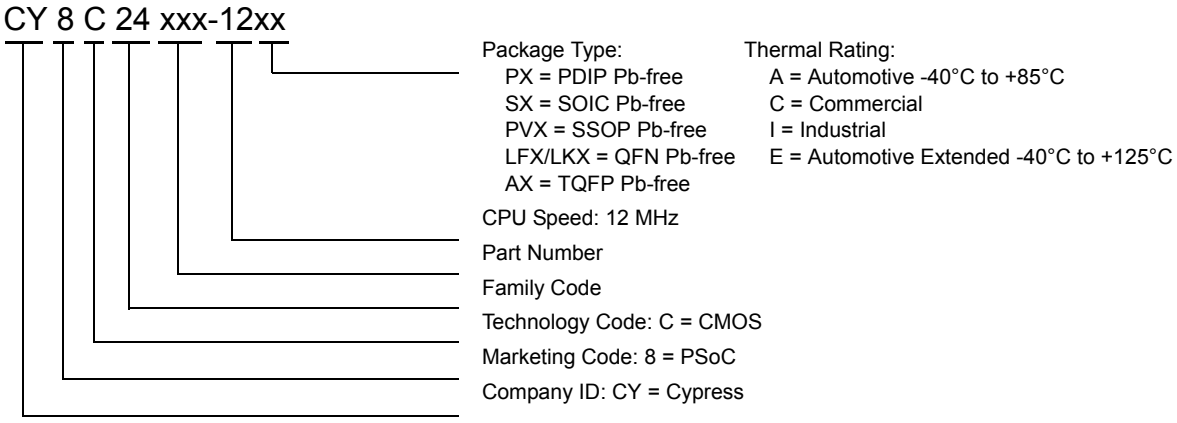
Notes
18. Pod kit contains an emulation pod, a flex-cable (connects the pod to the ICE), two feet, and device samples.
19. Foot kit includes surface mount feet that can be soldered to the target PCB.
20. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters can be found at http://www.emulation.com.

Ordering Information

The following table lists the automotive CY8C24x23A PSoC device group's key package features and ordering codes.

Package	Ordering Code	Flash (Bytes)	RAM (Bytes)	Switch Mode Pump	Temperature Range	Digital Blocks	Analog Blocks	Digital I/O Pins	Analog Inputs	Analog Outputs	XRES Pin
20 Pin (210 Mil) SSOP	CY8C24223A-12PVXE	4K	256	No	-40°C to +125°C	4	6	16	8	2	Yes
20 Pin (210 Mil) SSOP (Tape and Reel)	CY8C24223A-12PVXET	4K	256	No	-40°C to +125°C	4	6	16	8	2	Yes
28 Pin (210 Mil) SSOP	CY8C24423A-12PVXE	4K	256	No	-40°C to +125°C	4	6	24	12[1]	2	Yes
28 Pin (210 Mil) SSOP (Tape and Reel)	CY8C24423A-12PVXET	4K	256	No	-40°C to +125°C	4	6	24	12[1]	2	Yes

Ordering Code Definitions



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