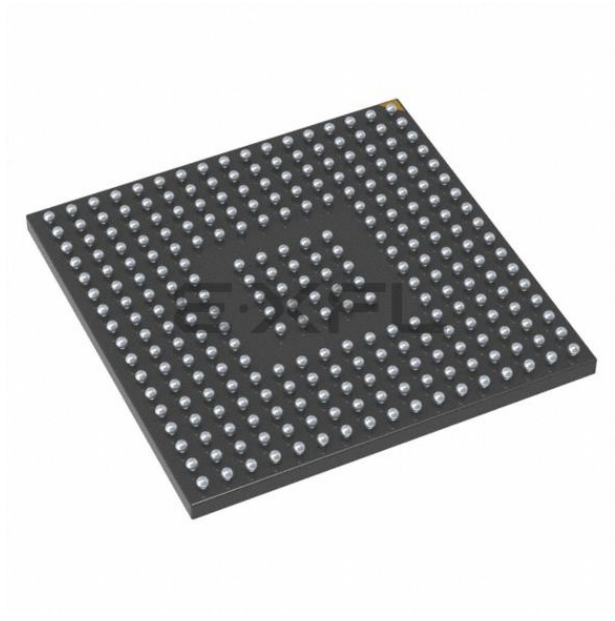

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	480MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MDIO, MMC/SD/SDIO, QSPI, SAI, SPDIF, SPI, SWPMI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	140
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1M x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 36x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	201-UFBGA
Supplier Device Package	176+25UFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32h743iik6

STM32H743xI devices operate in the –40 to +85 °C temperature range from a 1.62 to 3.6 V power supply. The supply voltage can drop down to 1.62 V by using an external power supervisor (see *Section 3.5.2: Power supply supervisor)* and connecting the PDR_ON pin to V_{SS}. Otherwise the supply voltage must stay above 1.71 V with the embedded power voltage detector enabled.

Dedicated supply inputs for USB (OTG_FS and OTG_HS) are available on all packages except LQFP100 to allow a greater power supply choice.

A comprehensive set of power-saving modes allows the design of low-power applications.

STM32H743xI devices are offered in 8 packages ranging from 100 pins to 240 pins/balls. The set of included peripherals changes with the device chosen.

These features make STM32H743xI microcontrollers suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances
- Mobile applications, Internet of Things
- Wearable devices: smart watches.

Figure 1 shows the general block diagram of the device family.

Table 2. STM32H743xI features and peripheral counts

Peripherals		STM32H743VI	STM32H743ZI	STM32H743AI	STM32H743II	STM32H743BI	STM32H743XI
Flash memory in Kbytes		2048					
SRAM in Kbytes	SRAM mapped onto AXI bus	512					
	SRAM1 (D2 domain)	128					
	SRAM2 (D2 domain)	128					
	SRAM3 (D2 domain)	32					
	SRAM4 (D3 domain)	64					
TCM RAM in Kbytes	ITCM RAM (instruction)	64					
	DTCM RAM (data)	128					
Backup SRAM (Kbytes)		4					
FMC		Yes					
Quad-SPI		Yes					
Ethernet		Yes					

The V_{CORE} domain is split into the following power domains that can be independently switch off.

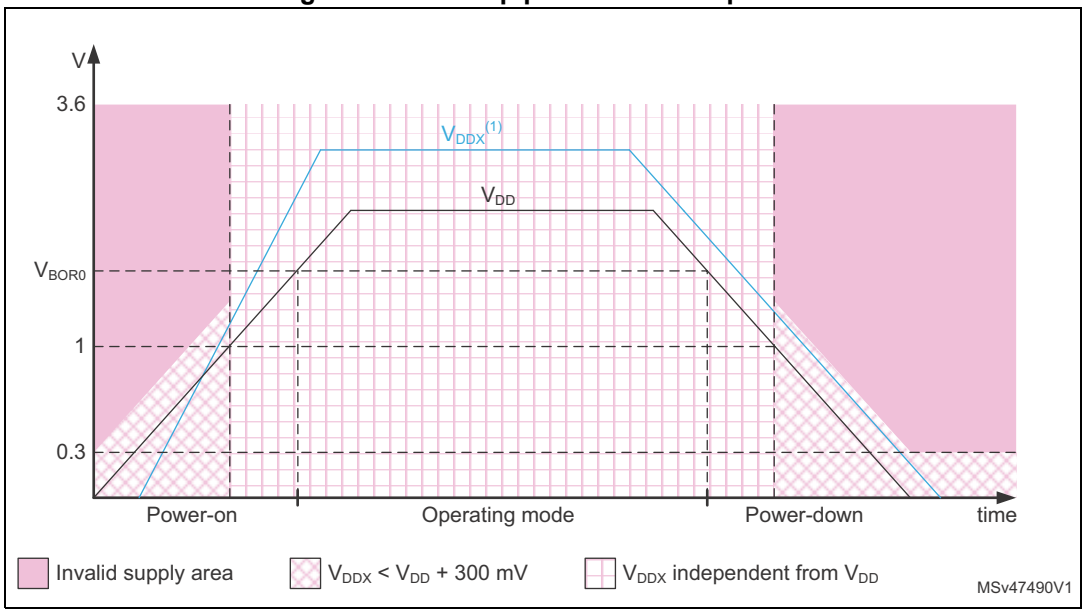
- D1 domain containing some peripherals and the Cortex®-M7 core.
- D2 domain containing a large part of the peripherals.
- D3 domain containing some peripherals and the system control.

During power-up and power-down phases, the following power sequence requirements must be respected (see *Figure 2*):

- When V_{DD} is below 1 V, other power supplies (V_{DDA}, $V_{DD33USB}$, $V_{DD50USB}$) must remain below V_{DD} + 300 mV.
- When V_{DD} is above 1 V, all power supplies are independent.

During the power-down phase, V_{DD} can temporarily become lower than other supplies only if the energy provided to the microcontroller remains below 1 mJ. This allows external decoupling capacitors to be discharged with different time constants during the power-down transient phase.

Figure 2. Power-up/power-down sequence



1. V_{DDx} refers to any power supply among V_{DDA}, $V_{DD33USB}$, $V_{DD50USB}$.

3.7 Reset and clock controller (RCC)

The clock and reset controller is located in D3 domain. The RCC manages the generation of all the clocks, as well as the clock gating and the control of the system and peripheral resets. It provides a high flexibility in the choice of clock sources and allows to apply clock ratios to improve the power consumption. In addition, on some communication peripherals that are capable to work with two different clock domains (either a bus interface clock or a kernel peripheral clock), the system frequency can be changed without modifying the baudrate.

3.7.1 Clock management

The devices embed four internal oscillators, two oscillators with external crystal or resonator, two internal oscillators with fast startup time and three PLLs.

The RCC receives the following clock source inputs:

- Internal oscillators:
  - 64 MHz HSI clock
  - 48 MHz RC oscillator
  - 4 MHz CSI clock
  - 32 kHz LSI clock
- External oscillators:
  - 4-48 MHz HSE clock
  - 32.768 kHz LSE clock

The RCC provides three PLLs: one for system clock, two for kernel clocks.

The system starts on the HSI clock. The user application can then select the clock configuration.

3.7.2 System reset sources

Power-on reset initializes all registers while system reset reinitializes the system except for the debug, part of the RCC and power controller status registers, as well as the backup power domain.

A system reset is generated in the following cases:

- Power-on reset (pwr_por_rst)
- Brownout reset
- Low level on NRST pin (external reset)
- Window watchdog
- Independent watchdog
- Software reset
- Low-power mode security reset
- Exit from Standby

3.25 LCD-TFT controller

The LCD-TFT display controller provides a 24-bit parallel digital RGB (Red, Green, Blue) and delivers all signals to interface directly to a broad range of LCD and TFT panels up to XGA (1024x768) resolution with the following features:

- 2 display layers with dedicated FIFO (64x64-bit)
- Color Look-Up table (CLUT) up to 256 colors (256x24-bit) per layer
- Up to 8 input color formats selectable per layer
- Flexible blending between two layers using alpha value (per pixel or constant)
- Flexible programmable parameters for each layer
- Color keying (transparency color)
- Up to 4 programmable interrupt events
- AXI master interface with burst of 16 words

3.26 JPEG Codec (JPEG)

The JPEG Codec can encode and decode a JPEG stream as defined in the ***ISO/IEC 10918-1*** specification. It provides an fast and simple hardware compressor and decompressor of JPEG images with full management of JPEG headers.

The JPEG codec main features are as follows:

- 8-bit/channel pixel depths
- Single clock per pixel encoding and decoding
- Support for JPEG header generation and parsing
- Up to four programmable quantization tables
- Fully programmable Huffman tables (two AC and two DC)
- Fully programmable minimum coded unit (MCU)
- Encode/decode support (non simultaneous)
- Single clock Huffman coding and decoding
- Two-channel interface: Pixel/Compress In, Pixel/Compressed Out
- Support for single greyscale component
- Ability to enable/disable header processing
- Fully synchronous design
- Configuration for High-speed decode mode

3.27 Random number generator (RNG)

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

3.28 Timers and watchdogs

The devices include one high-resolution timer, two advanced-control timers, ten general-purpose timers, two basic timers, five low-power timers, two watchdogs and a SysTick timer.

3.28.4 Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger and waveform generation. They can also be used as a generic 16-bit time base.

TIM6 and TIM7 support independent DMA request generation.

3.28.5 Low-power timers (LPTIM1, LPTIM2, LPTIM3, LPTIM4, LPTIM5)

The low-power timers have an independent clock and is running also in Stop mode if it is clocked by LSE, LSI or an external clock. It is able to wakeup the devices from Stop mode.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous / One-shot mode
- Selectable software / hardware input trigger
- Selectable clock source:
- Internal clock source: LSE, LSI, HSI or APB clock
- External clock source over LPTIM input (working even with no internal clock source running, used by the Pulse Counter Application)
- Programmable digital glitch filter
- Encoder mode

3.28.6 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

3.28.7 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in Debug mode.

3.28.8 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source.

Table 8. STM32H743xI pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
-	-	-	K3	H4	45	48	P3	PH4	I/O	FT_fa	-	I2C2_SCL, LCD_G5, OTG_HS_ULPI_NXT, LCD_G4, EVENTOUT	ADC3_INN14, ADC3_INP15
-	-	-	L3	J4	46	49	P4	PH5	I/O	FT_fa	-	I2C2_SDA, SPI5_NSS, FMC_SDNWE, EVENTOUT	ADC3_INN15, ADC3_INP16
25	K2	37	N3	R2	47	50	U2	PA3	I/O	FT_ha	-	TIM2_CH4, TIM5_CH4, LPTIM5_OUT, TIM15_CH2, USART2_RX, LCD_B2, OTG_HS_ULPI_D0, ETH_MII_COL, LCD_B5, EVENTOUT	ADC12_INP15
26	-	38	G2	K6	-	51	F2(4)	VSS	S	-	-	-	-
-	-	-	-	L4	48	-	-	VSS	S	-	-	-	-
27	-	39	-	K4	49	52	G5	VDD	S	-	-	-	-
28	G3	40	H6	N4	50	53	U3	PA4	I/O	TT_a	-	TIM5_ETR, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, SPI6_NSS, OTG_HS_SOF, DCMI_HSYNC, LCD_VSYNC, EVENTOUT	ADC12_INP18, DAC1_OUT1
29	H3	41	L4	P4	51	54	T3	PA5	I/O	TT_ha	-	TIM2_CH1/TIM2_ETR, TIM8_CH1N, SPI1_SCK/I2S1_CK, SPI6_SCK, OTG_HS_ULPI_CK, LCD_R4, EVENTOUT	ADC12_INN18, ADC12_INP19, DAC1_OUT2
30	J3	42	K5	P3	52	55	R3	PA6	I/O	FT_a	-	TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO/I2S1_SDI, SPI6_MISO, TIM13_CH1, TIM8_BKIN_COMP12, MDIOS_MDC, TIM1_BKIN_COMP12, DCMI_PIXCLK, LCD_G2, EVENTOUT	ADC12_INP3

Table 8. STM32H743xI pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
38	J5	59	H8	P8	69	80	T9	PE8	I/O	TT_ha	-	TIM1_CH1N, DFSDM_CKIN2, UART7_TX, QUADSPI_BK2_IO1, FMC_D5/FMC_DA5, COMP_2_OUT, EVENTOUT	OPAMP2_VINM
39	K5	60	J8	P9	70	81	P9	PE9	I/O	TT_ha	-	TIM1_CH1, DFSDM_CKOUT, UART7_RTS, QUADSPI_BK2_IO2, FMC_D6/FMC_DA6, EVENTOUT	OPAMP2_VINP, COMP_2_INP
-	-	61	C12	M9	71	82	J17	VSS	S	-	-	-	-
-	-	62	C13	N9	72	83	J13	VDD	S	-	-	-	-
40	G6	63	M8	R9	73	84	N9	PE10	I/O	FT_ha	-	TIM1_CH2N, DFSDM_DATIN4, UART7_CTS, QUADSPI_BK2_IO3, FMC_D7/FMC_DA7, EVENTOUT	COMP_2_INM
41	H6	64	N8	P10	74	85	P10	PE11	I/O	FT_ha	-	TIM1_CH2, DFSDM_CKIN4, SPI4_NSS, SAI2_SD_B, FMC_D8/FMC_DA8, LCD_G3, EVENTOUT	COMP_2_INP
42	J6	65	L8	R10	75	86	R10	PE12	I/O	FT_h	-	TIM1_CH3N, DFSDM_DATIN5, SPI4_SCK, SAI2_SCK_B, FMC_D9/FMC_DA9, COMP_1_OUT, LCD_B4, EVENTOUT	-
43	K6	66	K8	N11	76	87	T10	PE13	I/O	FT_h	-	TIM1_CH3, DFSDM_CKIN5, SPI4_MISO, SAI2_FS_B, FMC_D10/FMC_DA10, COMP_2_OUT, LCD_DE, EVENTOUT	-
-	-	-	L12	F7	-	-	K15	VSS	S	-	-	-	-
-	-	-	H13	-	-	-	K13	VDD	S	-	-	-	-

Table 8. STM32H743xI pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
44	G7	67	J9	P11	77	88	U10	PE14	I/O	FT_h	-	TIM1_CH4, SPI4_MOSI, SAI2_MCK_B, FMC_D11/FMC_DA11, LCD_CLK, EVENTOUT	-
45	H7	68	N9	R11	78	89	R11	PE15	I/O	FT_h	-	TIM1_BKIN, HDMI__TIM1_BKIN, FMC_D12/FMC_DA12, TIM1_BKIN_COMP12, LCD_R7, EVENTOUT	-
46	J7	69	L9	R12	79	90	P11	PB10	I/O	FT_f	-	TIM2_CH3, HRTIM_SCOUT, LPTIM2_IN1, I2C2_SCL, SPI2_SCK/I2S2_CK, DFSDM_DATIN7, USART3_TX, QUADSPI_BK1_NCS, OTG_HS_ULPI_D3, ETH_MII_RX_ER, LCD_G4, EVENTOUT	-
47	K7	70	M9	R13	80	91	P12	PB11	I/O	FT_f	-	TIM2_CH4, HRTIM_SCIN, LPTIM2_ETR, I2C2_SDA, DFSDM_CKIN7, USART3_RX, OTG_HS_ULPI_D4, ETH_MII_TX_EN/ETH_RMII_TX_EN, LCD_G5, EVENTOUT	-
48	F8	71	N10	M10	81	92	U11	VCAPVCAP	S	-	-	-	-
49	E4	-	-	K7	-	93	L15	VSS	S	-	-	-	-
-	-	-	M10	-	-	-	U12	VDDLDO	S	-	-	-	-
50	-	72	M1	N10	82	94	L13	VDD	S	-	-	-	-
-	-	-	-	-	-	95	R12	PJ5	I/O	FT	-	LCD_R6, EVENTOUT	-
-	-	-	-	M11	83	96	T11	PH6	I/O	FT	-	TIM12_CH1, I2C2_SMBA, SPI5_SCK, ETH_MII_RXD2, FMC_SDNE1, DCMI_D8, EVENTOUT	-
-	-	-	-	N12	84	97	U13	PH7	I/O	FT_fa	-	I2C3_SCL, SPI5_MISO, ETH_MII_RXD3, FMC_SDCKE1, DCMI_D9, EVENTOUT	-

Table 8. STM32H743xI pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
97	D4	141	D5	A4	169	200	C4	PE0	I/O	FT_h	-	LPTIM1_ETR, TIM4_ETR, HRTIM_SCIN, LPTIM2_ETR, UART8_RX, FDCAN1_RXFD_MODE, SAI2_MCK_A, FMC_NBL0, DCMI_D2, EVENTOUT	-
98	C4	142	D4	A3	170	201	B4	PE1	I/O	FT_h	-	LPTIM1_IN2, HRTIM_SCOUT, UART8_TX, FDCAN1_TXFD_MODE, FMC_NBL1, DCMI_D3, EVENTOUT	-
-	-	-	-	-	-	-	A7	VCAP	S	-	-	-	-
99	-	-	-	D5	-	202	-	VSS	S	-	-	-	-
-	F7	143	C4	C6	171	203	E7	PDR_ON	S	-	-	-	-
-	F4	-	B4	-	-	-	A6	VDDLDO	S	-	-	-	-
100	-	144	-	C5	172	204	-	VDD	S	-	-	-	-
-	-	-	-	D4	173	205	A4	PI4	I/O	FT_h	-	TIM8_BKIN, SAI2_MCK_A, TIM8_BKIN_COMP12, FMC_NBL2, DCMI_D5, LCD_B4, EVENTOUT	-
-	-	-	-	C4	174	206	A3	PI5	I/O	FT_h	-	TIM8_CH1, SAI2_SCK_A, FMC_NBL3, DCMI_VSYNC, LCD_B5, EVENTOUT	-
-	-	-	A4	C3	175	207	A2	PI6	I/O	FT_h	-	TIM8_CH2, SAI2_SD_A, FMC_D28, DCMI_D6, LCD_B6, EVENTOUT	-
-	-	-	E2	C2	176	208	B3	PI7	I/O	FT_h	-	TIM8_CH3, SAI2_FS_A, FMC_D29, DCMI_D7, LCD_B7, EVENTOUT	-
-	-	-	-	H9	-	-	-	VSS	S	-	-	-	-
-	-	-	-	K9	-	-	-	VSS	S	-	-	-	-
-	-	-	-	K10	-	-	-	VSS	S	-	-	-	-

1. When this pin/ball was previously configured as an oscillator, the oscillator function is kept during and after a reset. This is valid for all resets except for power-on reset.
2. This ball should remain floating.

Table 15. Port G alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/ HRTIM1	SAI1/TIM3/4/5/12/ HRTIM1	LPUART/ TIM8/ LPTIM2/3/4/5/HRTIM1/ DFSDM	I2C1/2/3/4/ USART1/ TIM15/ LPTIM2/ DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/ UART4/ DFSDM	SPI2/3/6/ USART1/2/3/6/UART7/ SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/ SDMMC1/ SPDIFRX	SAI4/ FDCAN1/2/ TIM13/14/ QUADSPI/ FMC/ SDMMC2/ LCD/SPDIFRX	SAI2/4/TIM8/ QUADSPI/ SDMMC2/ OTG1_HS/ OTG2_FS/ LCD	I2C4/UART7/SWPMI1/ TIM1/8/ DFSDM/ SDMMC2/ MDIOS/ETH	TIM1/8/FMC/SDMMC1/ MDIOS/ OTG1_FS/ LCD	TIM1/ DCMI/LCD/COMP	UART5/ LCD	SYS
Port G	PG0	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A10	-	-	EVENT-OUT
	PG1	-	-	-	-	-	-	-	-	-	-	-	-	FMC_A11	-	-	EVENT-OUT
	PG2	-	-	-	TIM8_BKIN	-	-	-	-	-	-	-	TIM8_BKIN_COMP12	FMC_A12	-	-	EVENT-OUT
	PG3	-	-	-	TIM8_BKIN2	-	-	-	-	-	-	-	TIM8_BKIN2_COMP12	FMC_A13	-	-	EVENT-OUT
	PG4	-	TIM1_BKIN2	-	-	-	-	-	-	-	-	-	TIM1_BKIN2_COMP12	FMC_A14/ FMC_BA0	-	-	EVENT-OUT
	PG5	-	TIM1_ETR	-	-	-	-	-	-	-	-	-	-	FMC_A15/ FMC_BA1	-	-	EVENT-OUT
	PG6	-	TIM17_BKIN	HRTIM_CHE1	-	-	-	-	-	-	-	QUADSPI_BK1_NCS	-	FMC_NE3	DCMI_D12	LCD_R7	EVENT-OUT
	PG7	-	-	HRTIM_CHE2	-	-	-	SAI1_MCLK_A	USART6_CK	-	-	-	-	FMC_INT	DCMI_D13	LCD_CLK	EVENT-OUT
	PG8	-	-	-	TIM8_ETR	-	SPI6_NSS	-	USART6_RTS	SPDIFRX_IN2	-	-	ETH_PPS_OUT	FMC_SDCLK	-	LCD_G7	EVENT-OUT
	PG9	-	-	-	-	-	SPI1_MISO/I2S1_SDI	-	USART6_RX	SPDIFRX_IN3	QUADSPI_BK2_IO2	SAI2_FS_B	-	FMC_NE2/ FMC_NCE	DCMI_VSYNC	-	EVENT-OUT
	PG10	-	-	HRTIM_FLT5	-	-	SPI1_NSS/ I2S1_WS	-	-	-	LCD_G3	SAI2_SD_B	-	FMC_NE3	DCMI_D2	LCD_B2	EVENT-OUT
	PG11	-	-	HRTIM_EEV4	-	-	SPI1_SCK/ I2S1_CK	-	-	SPDIFRX_IN0	-	SDMMC2_D2	ETH_MII_TX_EN/ ETH_RMII_TX_EN	-	DCMI_D3	LCD_B3	EVENT-OUT
	PG12	-	LPTIM1_IN1	HRTIM_EEV5	-	-	SPI6_MISO		USART6_RTS	SPDIFRX_IN1	LCD_B4	-	ETH_MII_TXD1/ETH_RMII_TXD1	FMC_NE4	-	LCD_B1	EVENT-OUT
	PG13	TRACED0	LPTIM1_OUT	HRTIM_EEV10	-	-	SPI6_SCK	-	USART6_CTS_NSS	-	-	-	ETH_MII_TXD0/ETH_RMII_TXD0	FMC_A24	-	LCD_R0	EVENT-OUT

Table 38. Peripheral current consumption in Run mode (continued)

Peripheral		I_{DD}(Typ)			Unit
		VOS1	VOS2	VOS3	
APB2	TIM1	5.1	4.8	4.3	µA/MHz
	TIM8	5.4	4.9	4.6	
	USART1 registers	2.7	2.6	2.5	
	USART1 kernel	0.1	0.1	0.1	
	USART6 registers	2.6	2.5	2.5	
	USART6 kernel	0.1	0.1	0.1	
	SPI1 registers	1.8	1.6	1.6	
	SPI1 kernel	1	0.8	0.6	
	SPI4 registers	1.6	1.5	1.5	
	SPI4 kernel	0.5	0.4	0.4	
	TIM15	3.1	2.8	2.7	
	TIM16	2.4	2.1	2.1	
	TIM17	2.2	2	1.9	
	SPI5 registers	1.8	1.7	1.7	
	SPI5 kernel	0.6	0.5	0.3	
	SAI1 registers	1.5	1.4	1.4	
	SAI1 kernel	2	1.7	1.5	
	SAI2 registers	1.5	1.5	1.3	
	SAI2 kernel	2.2	1.9	1.8	
	SAI3 registers	1.8	1.6	1.6	
	SAI3 kernel	2.5	2.3	2.1	
	DFSDM1 registers	6	5.4	5.2	
	DFSDM1 kernel	0.9	0.8	0.7	
	HRTIM	40	37	35	
	Bridge APB2	0.1	0.1	0.1	

Table 38. Peripheral current consumption in Run mode (continued)

Peripheral		I_{DD}(Typ)			Unit
		VOS1	VOS2	VOS3	
APB4	SYSCFG	1	0.7	0.7	µA/MHz
	LPUART1 registers	1.1	1.1	1.1	
	LPUART1 kernel	2.6	2.4	2.1	
	SPI6 registers	1.6	1.5	1.4	
	SPI6 kernel	0.2	0.2	0.2	
	I2C4 registers	0.1	0.1	0.1	
	I2C4 kernel	2.4	2.1	2	
	LPTIM2 registers	0.5	0.5	0.5	
	LPTIM2 kernel	2.3	2.1	1.8	
	LPTIM3 registers	0.5	0.5	0.5	
	LPTIM3 kernel	2	2.1	1.5	
	LPTIM4 registers	0.5	0.5	0.5	
	LPTIM4 kernel	2	2	1.9	
	LPTIM5 registers	0.5	0.5	0.5	
	LPTIM5 kernel	2	1.8	1.5	
	COMP1/2	0.7	0.5	0.5	
	VREFBUF	0.6	0.4	0.4	
	RTC	1.2	1.1	1.1	
	SAI4 registers	1.6	1.5	1.4	
	SAI4 kernel	1.3	1.3	1.2	
	Bridge APB4	0.1	0.1	0.1	

Table 39. Peripheral current consumption in Stop, Standby and VBAT mode

Symbol	Parameter	Conditions	Typ	Unit
			3 V	
I_{DD}	RTC+LSE low drive	-	2.32	µA
	RTC+LSE medium-low drive	-	2.4	
	RTC+LSE medium-high drive	-	2.7	
	RTC+LSE High drive	-	3	

6.3.8 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard I/O.

The external clock signal has to respect the *Table 59: I/O static characteristics*. However, the recommended clock input waveform is shown in *Figure 17*.

Table 41. High-speed external user clock characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	4	25	50	MHz
V_{SW} (V_{HSEH}–V_{HSEL})	OSC_IN amplitude	$0.7V_{DD}$	-	V_{DD}	V
V_{DC}	OSC_IN input voltage	V_{SS}	-	$0.3V_{SS}$	
$t_{W(HSE)}$	OSC_IN high or low time	7	-	-	ns

1. Guaranteed by design.

Figure 17. High-speed external clock source AC timing diagram

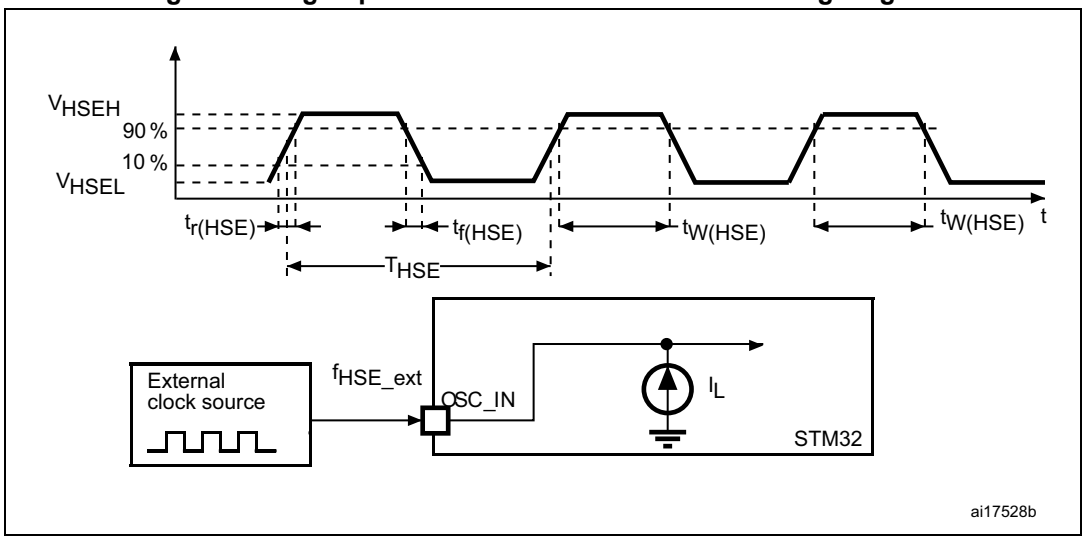


Figure 29. Synchronous non-multiplexed NOR/PSRAM read timings

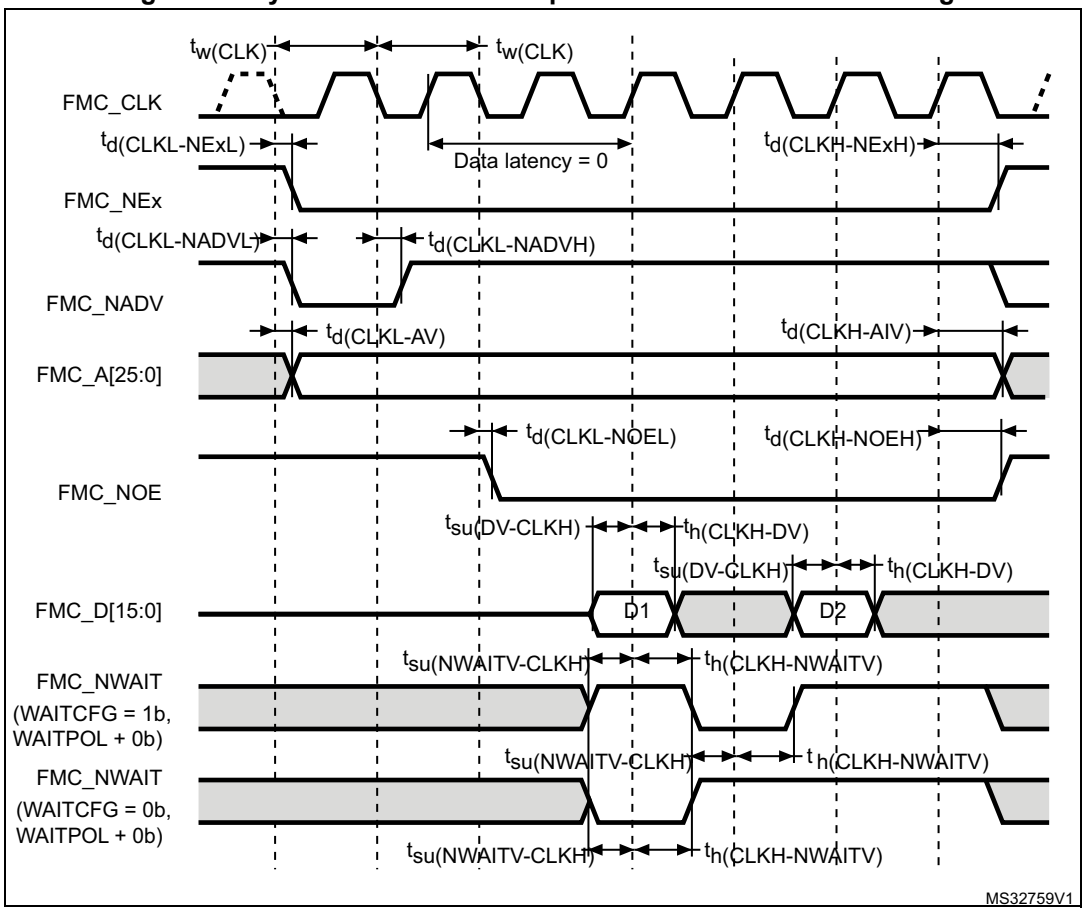


Table 74. Synchronous non-multiplexed NOR/PSRAM read timings(1)

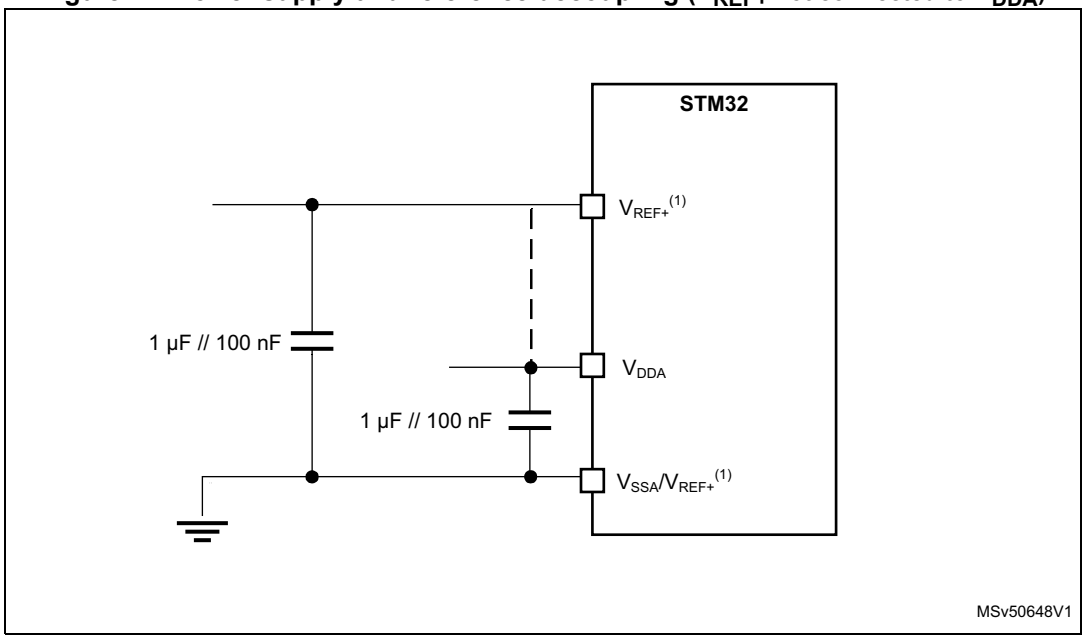
Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{fmc\_ker\_ck} - 1$	-	ns
$t_{(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	2	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	$T_{fmc\_ker\_ck} + 0.5$	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	0.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	2	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	$T_{fmc\_ker\_ck}$	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	1.5	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	$T_{fmc\_ker\_ck} + 0.5$	-	
$t_{su(DV-CLKH)}$	FMC_D[15:0] valid data before FMC_CLK high	2	-	
$t_{h(CLKH-DV)}$	FMC_D[15:0] valid data after FMC_CLK high	1	-	
$t_{(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	2	-	

1. Guaranteed by characterization results.

General PCB design guidelines

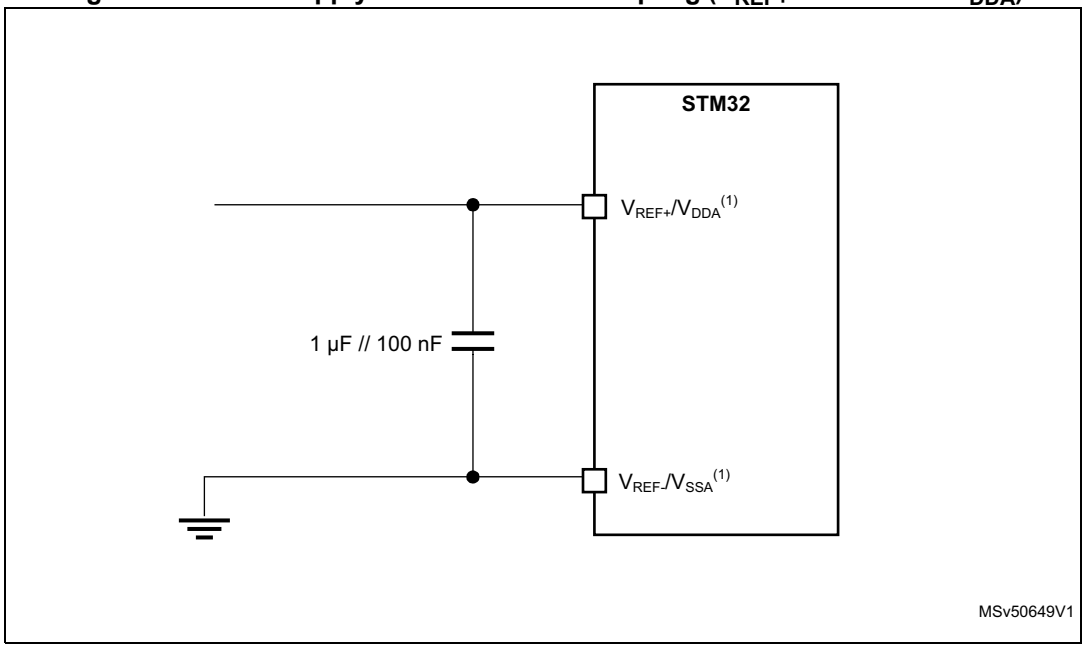
Power supply decoupling should be performed as shown in *Figure 41* or *Figure 42*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 100 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 41. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} input is available on all package whereas the V_{REF-} s available only on UFBGA176+25 and TFBGA240+25. When V_{REF-} is not available, it is internally connected to V_{DDA} and V_{SSA}.

Figure 42. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} input is available on all package whereas the V_{REF-} s available only on UFBGA176+25 and TFBGA240+25. When V_{REF-} is not available, it is internally connected to V_{DDA} and V_{SSA}.

6.3.24 V_{BAT} monitoring characteristics

Table 92. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	26	-	KΩ
Q	Ratio on V_{BAT} measurement	-	4	-	-
Er(1)	Error on Q	–10	-	+10	%
t_{S_vbat}(1)	ADC sampling time when reading V_{BAT} input	9	-	-	µs

1. Guaranteed by design.

Table 93. V_{BAT} charging characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VBRS in PWR_CR3= 0	-	5	-	KΩ
		VBRS in PWR_CR3= 1		1.5	-	

6.3.25 Voltage booster for analog switch

Table 94. Voltage booster for analog switch characteristics(1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD}	Supply voltage	-	1.62	2-6	3.6	V
$t_{SU(BOOST)}$	Booster startup time	-	-	-	50	µs
$I_{DD(BOOST)}$	Booster consumption	1.62 V ≤ V_{DD} ≤ 2.7 V	-	-	125	µA
		2.7 V < V_{DD} < 3.6 V	-	-	250	

1. Guaranteed by characterization results.

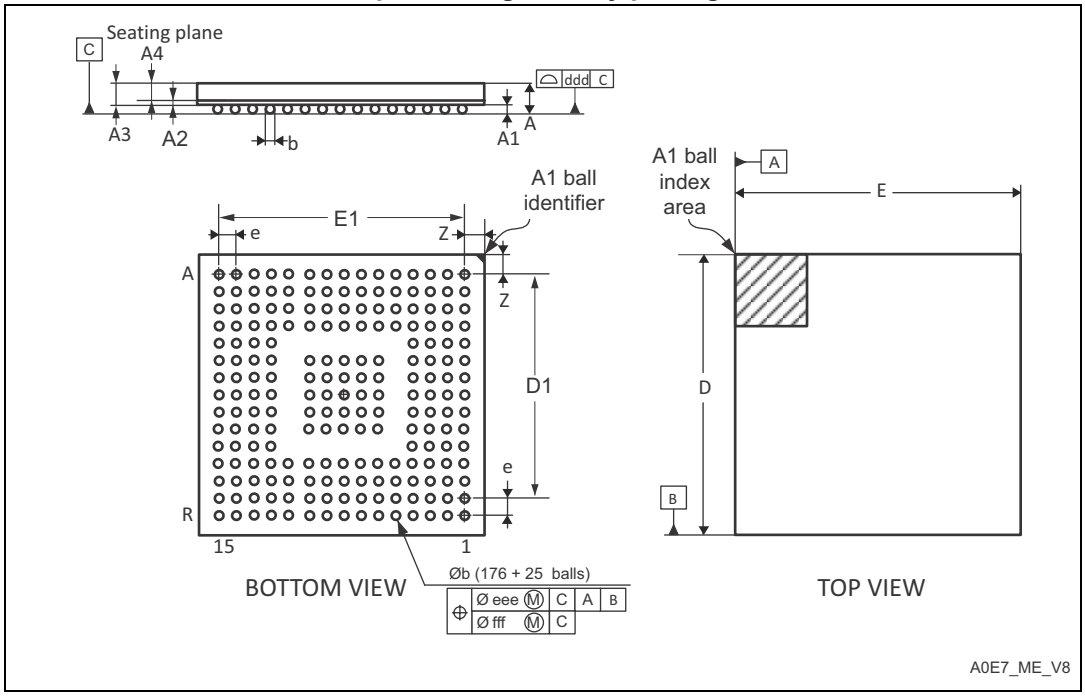
Table 96. OPAMP characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
en	Voltage noise density	at 1 KHz	output loaded with 4 kΩ	-	140	-	nV/√Hz
		at 10 KHz		-	55	-	
$I_{DDA(OPAMP)}$	OPAMP consumption from V_{DDA}	Normal mode	no Load, quiescent mode, follower	-	570	1000	µA
		High-speed mode		-	610	1200	

1. Guaranteed by design, unless otherwise specified.
2. R_{LOAD} is the resistive load connected to VSSA or to VDDA.
3. R2 is the internal resistance between the OPAMP output and th OPAMP inverting input. R1 is the internal resistance between the OPAMP inverting input and ground. PGA gain = 1 + R2/R1.

7.7 UFBGA176+25 package information

Figure 81. UFBGA176+25 - 201-ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 123. UFBGA176+25 - ball, 10 x 10 mm, 0.65 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.130	-	-	0.0051	-
A3	-	0.450	-	-	0.0177	-
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	9.850	10.000	10.150	0.3878	0.3937	0.3996
D1	-	9.100	-	-	0.3583	-
E	9.850	10.000	10.150	0.3878	0.3937	0.3996
E1	-	9.100	-	-	0.3583	-
e	-	0.650	-	-	0.0256	-
Z	-	0.450	-	-	0.0177	-
ddd	-	-	0.080	-	-	0.0031

Table 129. Document revision history

Date	Revision	Changes
18-May-2018	4 (continued)	Updated typical and maximum current consumption in *Table 36: Typical and maximum current consumption in Standby mode* and *Table 37: Typical and maximum current consumption in VBAT mode*. Added note to f_{LSI} in *Table 48: LSI oscillator characteristics*. Updated *Figure 21: VIL/VIH for all I/Os except BOOT0*. Added note in *Table 82: Quad-SPI characteristics in SDR mode*, *Table 83: Quad SPI characteristics in DDR mode* and *Table 84: Dynamics characteristics: Delay Block characteristics*. *Section 6.3.20: 16-bit ADC characteristics*: updated THD conditions in *Table 86: ADC accuracy*; removed formula to compute R_{AIN}. Changed decoupling capacitor value to 100 nF in *Section : General PCB design guidelines*.* Added note in *Table 87: DAC characteristics*, *Table 94: Voltage booster for analog switch characteristics*, *Table 97: DFSDM measured timing 1.62-3.6 V*, *Table 114: Dynamics characteristics: JTAG characteristics* and *Table 115: Dynamics characteristics: SWD characteristics*. Updated *Figure 73: LQFP144 marking example (package top view)*, *Figure 77: LQFP176 marking example (package top view)* and *Figure 80: LQFP208 marking example (package top view)*. Updated TFBGA240+25 package information to final mechanical data.
13-Jul-2018	5	Added description of power-up and power-down phases in *Section 3.5.1: Power supply scheme*. Removed ETH_TX_ER from *Table 8: STM32H743xI pin/ball definition* and *Table 9: Port A alternate functions* to *Table 19: Port K alternate functions*. Added note related to decoupling capacitor tolerance below *Figure 14: Power supply scheme*. Added note *2.* related to CEXT in *Table 24: VCAP operating conditions*. Updated *Table 45: HSI48 oscillator characteristics*, *Table 46: HSI oscillator characteristics* and *Table 47: CSI oscillator characteristics*. Renamed *Table 49* into “PLL characteristics (wide VCO frequency range)” and updated note *2.*. Added *Table 50: PLL characteristics (medium VCO frequency range)*. Updated T_{coeff} in *Table 89: VREFBUF characteristics*. Updated t_{S_vbat} in *Table 92: VBAT monitoring characteristics*. Updated *Table 96: OPAMP characteristics*.