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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M7 |
| Core Size | 32-Bit Single-Core |
| Speed | 480MHz |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MDIO, MMC/SD/SDIO, QSPI, SAI, SPDIF, SPI, SWPMI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT |
| Number of I/O | 140 |
| Program Memory Size | 2MB (2M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 1M x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.62V ~ 3.6V |
| Data Converters | A/D 36x16b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 176-LQFP |
| Supplier Device Package | 176-LQFP (24x24) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32h743iit6 |

## 3.3 Memories

### 3.3.1 Embedded Flash memory

The STM32H743xI devices embed up to 2 Mbytes of Flash memory that can be used for storing programs and data.

The Flash memory is organized as 266-bit Flash words memory that can be used for storing both code and data constants. Each word consists of:

- One Flash word (8 words, 32 bytes or 256 bits)
- 10 ECC bits.

The Flash memory is divided into two independent banks. Each bank is organized as follows:

- A 1-Mbyte user Flash memory block containing eight user sectors of 128 Kbytes(4 K Flash words)
- 128 Kbytes of System Flash memory from which the device can boot
- 2 Kbytes (64 Flash words) of user option bytes for user configuration

### 3.3.2 Embedded SRAM

All devices feature:

- 512 Kbytes of AXI-SRAM mapped onto AXI bus on D1 domain.
- SRAM1 mapped on D2 domain: 128 Kbytes
- SRAM2 mapped on D2 domain: 128 Kbytes
- SRAM3 mapped on D2 domain: 32 Kbytes
- SRAM4 mapped on D3 domain: 64 Kbytes
- 4 Kbytes of backup SRAM

  The content of this area is protected against possible unwanted write accesses, and is retained in Standby or $V_{BAT}$ mode.
- RAM mapped to TCM interface (ITCM and DTCM):

  Both ITCM and DTCM RAMs are 0 wait state memories. either They can be accessed either from the CPU or the MDMA (even in Sleep mode) through a specific AHB slave of the CPU(AHBP):
  - 64 Kbytes of ITCM-RAM (instruction RAM)

    This RAM is connected to ITCM 64-bit interface designed for execution of critical real-times routines by the CPU.
  - 128 Kbytes of DTCM-RAM (2x 64-Kbyte DTCM-RAMs on 2x32-bit DTCM ports)

    The DTCM-RAM could be used for critical real-time data, such as interrupt service routines or stack/heap memory. Both DTCM-RAMs can be used in parallel (for load/store operations) thanks to the Cortex®-M7 dual issue capability.

  The MDMA can be used to load code or data in ITCM or DTCM RAMs.

The $V_{CORE}$ domain is split into the following power domains that can be independently switch off.

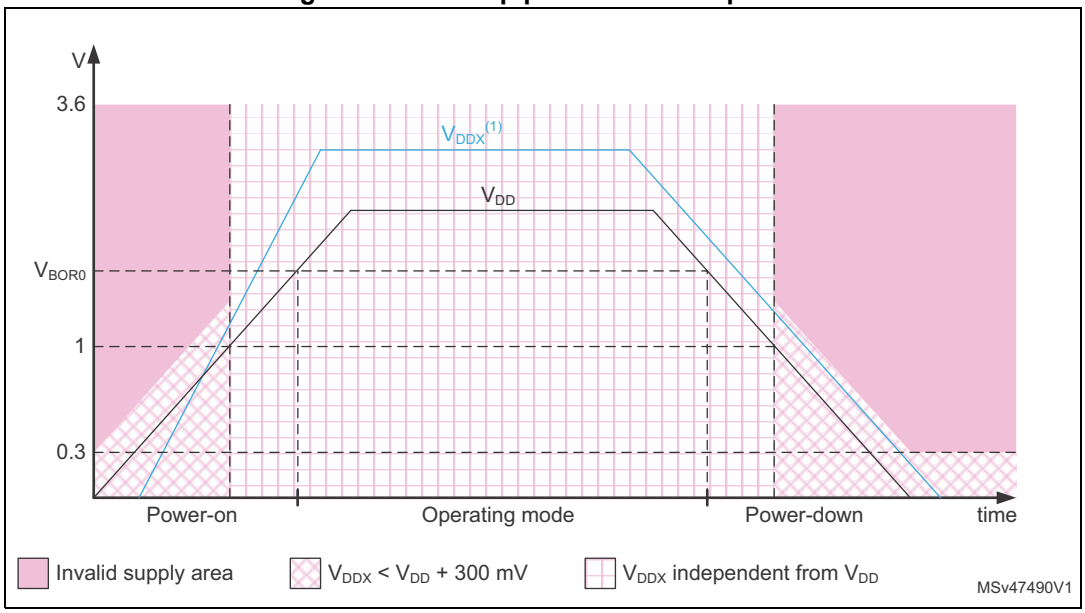
- D1 domain containing some peripherals and the Cortex®-M7 core.
- D2 domain containing a large part of the peripherals.
- D3 domain containing some peripherals and the system control.

During power-up and power-down phases, the following power sequence requirements must be respected (see *Figure 2*):

- When $V_{DD}$ is below 1 V, other power supplies ($V_{DDA}$, $V_{DD33USB}$, $V_{DD50USB}$) must remain below $V_{DD}$ + 300 mV.
- When $V_{DD}$ is above 1 V, all power supplies are independent.

During the power-down phase, $V_{DD}$ can temporarily become lower than other supplies only if the energy provided to the microcontroller remains below 1 mJ. This allows external decoupling capacitors to be discharged with different time constants during the power-down transient phase.

**Figure 2. Power-up/power-down sequence**




1. $V_{DDx}$ refers to any power supply among $V_{DDA}$, $V_{DD33USB}$, $V_{DD50USB}$.

### 3.5.2 Power supply supervisor

The devices have an integrated power-on reset (POR)/ power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry:

- Power-on reset (POR)

  The POR supervisor monitors $V_{DD}$ power supply and compares it to a fixed threshold. The devices remain in Reset mode when $V_{DD}$ is below this threshold,

- Power-down reset (PDR)

  The PDR supervisor monitors $V_{DD}$ power supply. A reset is generated when $V_{DD}$ drops below a fixed threshold.

  The PDR supervisor can be enabled/disabled through PDR_ON pin.

- Brownout reset (BOR)

  The BOR supervisor monitors $V_{DD}$ power supply. Three BOR thresholds (from 2.1 to 2.7 V) can be configured through option bytes. A reset is generated when $V_{DD}$ drops below this threshold.

### 3.5.3 Voltage regulator

The same voltage regulator supplies the 3 power domains (D1, D2 and D3). D1 and D2 can be independently switched off.

Voltage regulator output can be adjusted according to application needs through 5 power supply levels:

- Run mode (VOS1 to VOS3)
  - Scale 1: high performance
  - Scale 2: medium performance and consumption
  - Scale 3: optimized performance and low-power consumption
- Stop mode (SVOS3 to SVOS5)
  - Scale 3: peripheral with wakeup from Stop mode capabilities (UART, SPI, I2C, LPTIM) are operational
  - Scale 4 and 5 where the peripheral with wakeup from Stop mode is disabled

    The peripheral functionality is disabled but wakeup from Stop mode is possible through GPIO or asynchronous interrupt.

## 3.25 LCD-TFT controller

The LCD-TFT display controller provides a 24-bit parallel digital RGB (Red, Green, Blue) and delivers all signals to interface directly to a broad range of LCD and TFT panels up to XGA (1024x768) resolution with the following features:

- 2 display layers with dedicated FIFO (64x64-bit)
- Color Look-Up table (CLUT) up to 256 colors (256x24-bit) per layer
- Up to 8 input color formats selectable per layer
- Flexible blending between two layers using alpha value (per pixel or constant)
- Flexible programmable parameters for each layer
- Color keying (transparency color)
- Up to 4 programmable interrupt events
- AXI master interface with burst of 16 words

## 3.26 JPEG Codec (JPEG)

The JPEG Codec can encode and decode a JPEG stream as defined in the ***ISO/IEC 10918-1*** specification. It provides an fast and simple hardware compressor and decompressor of JPEG images with full management of JPEG headers.

The JPEG codec main features are as follows:

- 8-bit/channel pixel depths
- Single clock per pixel encoding and decoding
- Support for JPEG header generation and parsing
- Up to four programmable quantization tables
- Fully programmable Huffman tables (two AC and two DC)
- Fully programmable minimum coded unit (MCU)
- Encode/decode support (non simultaneous)
- Single clock Huffman coding and decoding
- Two-channel interface: Pixel/Compress In, Pixel/Compressed Out
- Support for single greyscale component
- Ability to enable/disable header processing
- Fully synchronous design
- Configuration for High-speed decode mode

## 3.27 Random number generator (RNG)

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

## 3.28 Timers and watchdogs

The devices include one high-resolution timer, two advanced-control timers, ten general-purpose timers, two basic timers, five low-power timers, two watchdogs and a SysTick timer.

### 3.28.2 Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1, TIM8) can be seen as three-phase PWM generators multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (Edge- or Center-aligned modes)
- One-pulse mode output

If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as 16-bit PWM generators, they have full modulation capability (0-100%).

The advanced-control timer can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

TIM1 and TIM8 support independent DMA request generation.

### 3.28.3 General-purpose timers (TIMx)

There are ten synchronizable general-purpose timers embedded in the STM32H743xI devices (see *Table 5* for differences).

- **TIM2, TIM3, TIM4, TIM5**

  The devices include 4 full-featured general-purpose timers: TIM2, TIM3, TIM4 and TIM5. TIM2 and TIM5 are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler while TIM3 and TIM4 are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. All timers feature 4 independent channels for input capture/output compare, PWM or One-pulse mode output. This gives up to 16 input capture/output compare/PWMs on the largest packages.

  TIM2, TIM3, TIM4 and TIM5 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers TIM1 and TIM8 via the Timer Link feature for synchronization or event chaining.

  Any of these general-purpose timers can be used to generate PWM outputs.

  TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

- **TIM12, TIM13, TIM14, TIM15, TIM16, TIM17**

  These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM13, TIM14, TIM16 and TIM17 feature one independent channel, whereas TIM12 and TIM15 have two independent channels for input capture/output compare, PWM or One-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers or used as simple timebases.

All USART have a clock domain independent from the CPU clock, allowing the USARTx to wake up the MCU from Stop mode.The wakeup from Stop mode is programmable and can be done on:

- Start bit detection
- Any received data frame
- A specific programmed data frame
- Specific TXFIFO/RXFIFO status when FIFO mode is enabled.

All USART interfaces can be served by the DMA controller.

**Table 6. USART features**

| USART modes/features(1) | USART1/2/3/6 | UART4/5/7/8 |
|---|---|---|
| Hardware flow control for modem | X | X |
| Continuous communication using DMA | X | X |
| Multiprocessor communication | X | X |
| Synchronous mode (Master/Slave) | X | - |
| Smartcard mode | X | - |
| Single-wire Half-duplex communication | X | X |
| IrDA SIR ENDEC block | X | X |
| LIN mode | X | X |
| Dual clock domain and wakeup from low power mode | X | X |
| Receiver timeout interrupt | X | X |
| Modbus communication | X | X |
| Auto baud rate detection | X | X |
| Driver Enable | X | X |
| USART data length | 7, 8 and 9 bits | |
| Tx/Rx FIFO | X | X |
| Tx/Rx FIFO size | 16 | |

1. X = supported.

## 3.32 Low-power universal asynchronous receiver transmitter (LPUART)

The device embeds one Low-Power UART (LPUART1). The LPUART supports asynchronous serial communication with minimum power consumption. It supports half duplex single wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

The LPUARTs embed a Transmit FIFO (TXFIFO) and a Receive FIFO (RXFIFO). FIFO mode is enabled by software and is disabled by default.

## 3.37 Management Data Input/Output (MDIO) slaves

The devices embed an MDIO slave interface it includes the following features:

- 32 MDIO Registers addresses, each of which is managed using separate input and output data registers:
  - 32 x 16-bit firmware read/write, MDIO read-only output data registers
  - 32 x 16-bit firmware read-only, MDIO write-only input data registers
- Configurable slave (port) address
- Independently maskable interrupts/events:
  - MDIO Register write
  - MDIO Register read
  - MDIO protocol error
- Able to operate in and wake up from Stop mode

## 3.38 SD/SDIO/MMC card host interfaces (SDMMC)

Two SDMMC host interfaces are available. They support *MultiMediaCard System Specification Version 4.51* in three different databus modes: 1 bit (default), 4 bits and 8 bits.

Both interfaces support the *SD memory card specifications version 4.1.* and the *SDIO card specification version 4.0.* in two different databus modes: 1 bit (default) and 4 bits.

Each SDMMC host interface supports only one SD/SDIO/MMC card at any one time and a stack of MMC Version 4.51 or previous.

The SDMMC host interface embeds a dedicated DMA controller allowing high-speed transfers between the interface and the SRAM.

## 3.39 Controller area network (FDCAN1, FDCAN2)

The controller area network (CAN) subsystem consists of two CAN modules, a shared message RAM memory and a clock calibration unit.

Both CAN modules (FDCAN1 and FDCAN2) are compliant with ISO 11898-1 (CAN protocol specification version 2.0 part A, B) and CAN FD protocol specification version 1.0.

FDCAN1 supports time triggered CAN (TTCAN) specified in ISO 11898-4, including event synchronized time-triggered communication, global system time, and clock drift compensation. The FDCAN1 contains additional registers, specific to the time triggered feature. The CAN FD option can be used together with event-triggered and time-triggered CAN communication.

A 10-Kbyte message RAM memory implements filters, receive FIFOs, receive buffers, transmit event FIFOs, transmit buffers (and triggers for TTCAN). This message RAM is shared between the two FDCAN1 and FDCAN2 modules.

The common clock calibration unit is optional. It can be used to generate a calibrated clock for both FDCAN1 and FDCAN2 from the HSI internal RC oscillator and the PLL, by evaluating CAN messages received by the FDCAN1.

**Table 8. STM32H743xI pin/ball definition**

| Pin/ball name | | | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP100 | TFBGA100 | LQFP144 | UFBGA169 | UFBGA176+25 | LQFP176 | LQFP208 | TFBGA240 +25 | | | | | | |
| 1 | A3 | 1 | A2 | A2 | 1 | 1 | C3 | PE2 | I/O | FT_h | - | TRACECLK, SAI1_CK1, SPI4_SCK, SAI1_MCLK_A, SAI4_MCLK_A, QUADSPI_BK1_IO2, SAI4_CK1, ETH_MII_TXD3, FMC_A23, EVENTOUT | - |
| 2 | B3 | 2 | B2 | A1 | 2 | 2 | D3 | PE3 | I/O | FT_h | - | TRACED0, TIM15_BKIN, SAI1_SD_B, SAI4_SD_B, FMC_A19, EVENTOUT | - |
| 3 | C3 | 3 | A1 | B1 | 3 | 3 | D2 | PE4 | I/O | FT_h | - | TRACED1, SAI1_D2, DFSDM_DATIN3, TIM15_CH1N, SPI4_NSS, SAI1_FS_A, SAI4_FS_A, SAI4_D2, FMC_A20, DCMI_D4, LCD_B0, EVENTOUT | - |
| 4 | D3 | 4 | C3 | B2 | 4 | 4 | D1 | PE5 | I/O | FT_h | - | TRACED2, SAI1_CK2, DFSDM_CKIN3, TIM15_CH1, SPI4_MISO, SAI1_SCK_A, SAI4_SCK_A, SAI4_CK2, FMC_A21, DCMI_D6, LCD_G0, EVENTOUT | - |
| 5 | E3 | 5 | C2 | B3 | 5 | 5 | E5 | PE6 | I/O | FT_h | - | TRACED3, TIM1_BKIN2, SAI1_D1, TIM15_CH2, SPI4_MOSI, SAI1_SD_A, SAI4_SD_A, SAI4_D1, SAI2_MCK_B, TIM1_BKIN2_COMP12, FMC_A22, DCMI_D7, LCD_G1, EVENTOUT | - |
| - | - | - | M4 | H10 | - | - | A1 | VSS | S | - | - | - | - |
| - | - | - | A3 | - | - | - | - | VDD | S | - | - | - | - |
| 6 | B2 | 6 | E3 | C1 | 6 | 6 | B1 | VBAT | S | - | - | - | - |
| - | - | - | - | J6 | - | - | B2 | VSS | - | - | - | - | - |
| - | - | - | - | D2 | 7 | 7 | E4 | PI8 | I/O | FT | - | EVENTOUT | RTC_TAMP_2/ RTC_TS/ WKUP3 |
| 7 | A2 | 7 | D3 | D1 | 8 | 8 | E3 | PC13 | I/O | FT | - | EVENTOUT | RTC_TAMP_1/ RTC_TS/ WKUP2 |
| - | - | - | - | J7 | - | - | B6 | VSS | - | - | - | - | - |

## Table 11. Port C alternate functions

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2/16/17/LPTIM1/HRTIM1 | SAI1/TIM3/4/5/12/HRTIM1 | LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM | I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM/CEC | SPI1/2/3/4/5/6/CEC | SPI2/3/SAI1/3/I2C4/UART4/DFSDM | SPI2/3/6/USART1/2/3/6/UART7/SDMMC1 | SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX | SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX | SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD | I2C4/UART7/SWPMI1/TIM1/8/DFSDM/SDMMC2/MDIOS/ETH | TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD | TIM1/DCMI/LCD/COMP | UART5/LCD | SYS |
| Port C | PC0 | - | - | - | DFSDM_CKIN0 | - | - | DFSDM_DATIN4 | - | SAI2_FS_B | - | OTG_HS_ULPI_STP | - | FMC_SDNWE | - | LCD_R5 | EVENT-OUT |
| | PC1 | TRACED0 | - | SAI1_D1 | DFSDM_DATIN0 | DFSDM_CKIN4 | SPI2_MOSI/I2S2_SDO | SAI1_SD_A | - | SAI4_SD_A | SDMMC2_CK | SAI4_D1 | ETH_MDC | MDIOS_MDC | - | - | EVENT-OUT |
| | PC2 | - | - | - | DFSDM_CKIN1 | - | SPI2_MISO/I2S2_SDI | DFSDM_CKOUT | - | - | - | OTG_HS_ULPI_DIR | ETH_MII_TXD2 | FMC_SDNE0 | - | - | EVENT-OUT |
| | PC3 | - | - | - | DFSDM_DATIN1 | - | SPI2_MOSI/I2S2_SDO | - | - | - | - | OTG_HS_ULPI_NXT | ETH_MII_TX_CLK | FMC_SDCKE0 | - | - | EVENT-OUT |
| | PC4 | - | - | - | DFSDM_CKIN2 | - | I2S1_MCK | - | - | - | SPDIFRX_IN2 | - | ETH_MII_RXD0/ETH_RMII_RXD0 | FMC_SDNE0 | - | - | EVENT-OUT |
| | PC5 | - | - | SAI1_D3 | DFSDM_DATIN2 | - | - | - | - | | SPDIFRX_IN3 | SAI4_D3 | ETH_MII_RXD1/ETH_RMII_RXD1 | FMC_SDCKE0 | COMP_1_OUT | - | EVENT-OUT |
| | PC6 | - | HRTIM_CHA1 | TIM3_CH1 | TIM8_CH1 | DFSDM_CKIN3 | I2S2_MCK | - | USART6_TX | SDMMC1_D0DIR | FMC_NWAIT | SDMMC2_D6 | - | SDMMC1_D6 | DCMI_D0 | LCD_HSYNC | EVENT-OUT |
| | PC7 | TRGIO | HRTIM_CHA2 | TIM3_CH2 | TIM8_CH2 | DFSDM_DATIN3 | - | I2S3_MCK | USART6_RX | SDMMC1_D123DIR | FMC_NE1 | SDMMC2_D7 | SWPMI_TX | SDMMC1_D7 | DCMI_D1 | LCD_G6 | EVENT-OUT |
| | PC8 | TRACED1 | HRTIM_CHB1 | TIM3_CH3 | TIM8_CH3 | - | - | - | USART6_CK | UART5_RTS | FMC_NE2/FMC_NCE | - | SWPMI_RX | SDMMC1_D0 | DCMI_D2 | - | EVENT-OUT |
| | PC9 | MCO2 | - | TIM3_CH4 | TIM8_CH4 | I2C3_SDA | I2S_CKIN | - | - | UART5_CTS | QUADSPI_BK1_IO0 | LCD_G3 | SWPMI_SUSPEND | SDMMC1_D1 | DCMI_D3 | LCD_B2 | EVENT-OUT |
| | PC10 | - | - | HRTIM_EEV1 | DFSDM_CKIN5 | - | - | SPI3_SCK/I2S3_CK | USART3_TX | UART4_TX | QUADSPI_BK1_IO1 | - | - | SDMMC1_D2 | DCMI_D8 | LCD_R2 | EVENT-OUT |
| | PC11 | - | - | HRTIM_FLT2 | DFSDM_DATIN5 | - | - | SPI3_MISO/I2S3_SDI | USART3_RX | UART4_RX | QUADSPI_BK2_NCS | - | - | SDMMC1_D3 | DCMI_D4 | - | EVENT-OUT |
| | PC12 | TRACED3 | - | HRTIM_EEV2 | - | - | - | SPI3_MOSI/I2S3_SDO | USART3_CK | UART5_TX | - | - | - | SDMMC1_CK | DCMI_D9 | - | EVENT-OUT |
| | PC13 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENT-OUT |

**Table 27. Embedded reference voltage (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{REFINT\_DIV1}$ | 1/4 reference voltage | - | - | 25 | - | % $V_{REFINT}$ |
| $V_{REFINT\_DIV2}$ | 1/2 reference voltage | - | - | 50 | - | |
| $V_{REFINT\_DIV3}$ | 3/4 reference voltage | - | - | 75 | - | |

1. The shortest sampling time for the application can be determined by multiple iterations.
2. Guaranteed by design.

**Table 28. Internal reference voltage calibration values**

| Symbol | Parameter | Memory address |
|---|---|---|
| $V_{REFIN\_CAL}$ | Raw data acquired at temperature of 30 °C, $V_{DDA}$ = 3.3 V | 1FF1E860 - 1FF1E861 |

### 6.3.6 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 15: Current consumption measurement scheme*.

All the run-mode current consumption measurements given in this section are performed with a CoreMark code.

#### Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode.
- All peripherals are disabled except when explicitly mentioned.
- The Flash memory access time is adjusted with the minimum wait states number, depending on the $f_{ACLK}$ frequency (refer to the table “Number of wait states according to CPU clock ($f_{rcc\_c\_ck}$) frequency and $V_{CORE}$ range” available in the reference manual).
- When the peripherals are enabled, the AHB clock frequency is the CPU frequency divided by 2 and the APB clock frequency is AHB clock frequency divided by 2.

The parameters given in *Table 29* to *Table 37* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 23: General operating conditions*.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

### On-chip peripheral current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- The I/O compensation cell is enabled.
- $f_{rcc\_c\_ck}$ is the CPU clock. $f_{PCLK} = f_{rcc\_c\_ck}/4$, and $f_{HCLK} = f_{rcc\_c\_ck}/2$.
  The given value is calculated by measuring the difference of current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
  - $f_{rcc\_c\_ck}$ = 400 MHz (Scale 1), $f_{rcc\_c\_ck}$ = 300 MHz (Scale 2), $f_{rcc\_c\_ck}$ = 200 MHz (Scale 3)
- The ambient operating temperature is 25 °C and $V_{DD}$=3.3 V.

**Table 52. Flash memory programming (single bank configuration nDBANK=1)**

| Symbol | Parameter | Conditions | Min(1) | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $t_{prog}$ | Word (266 bits) programming time | Program/erase parallelism x 8 | - | 290 | 580(2) | µs |
| | | Program/erase parallelism x 16 | - | 180 | 360 | |
| | | Program/erase parallelism x 32 | - | 130 | 260 | |
| | | Program/erase parallelism x 64 | - | 100 | 200 | |
| $t_{ERASE128KB}$ | Sector (128 KB) erase time | Program/erase parallelism x 8 | - | 2 | 4 | s |
| | | Program/erase parallelism x 16 | - | 1.8 | 3.6 | |
| | | Program/erase parallelism x 32 | - | | | |
| $t_{ME}$ | Mass erase time | Program/erase parallelism x 8 | - | 13 | 26 | |
| | | Program/erase parallelism x 16 | - | 8 | 16 | |
| | | Program/erase parallelism x 32 | - | 6 | 12 | |
| | | Program/erase parallelism x 64 | - | 5 | 10 | |
| $V_{prog}$ | Programming voltage | Program parallelism x 8 | 1.62 | - | 3.6 | V |
| | | Program parallelism x 16 | | | | |
| | | Program parallelism x 32 | | | | |
| | | Program parallelism x 64 | 1.8 | - | 3.6 | |

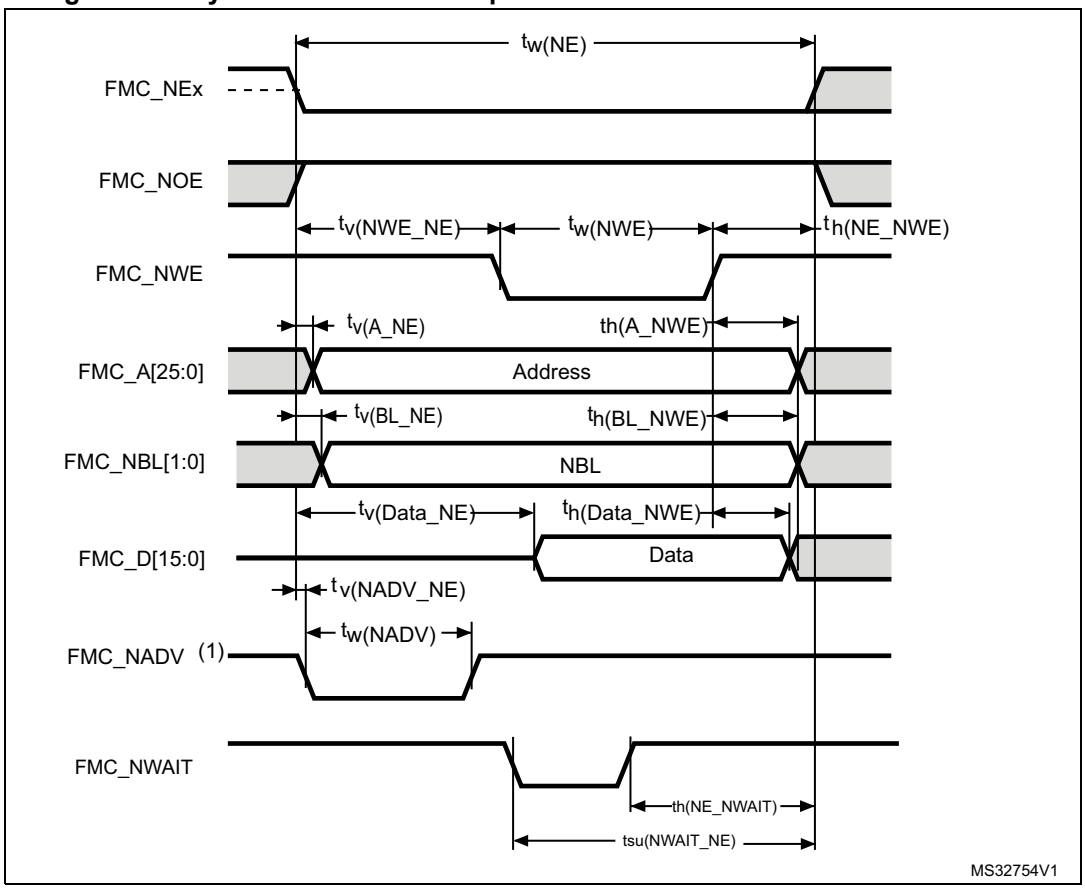
1. Guaranteed by characterization results.
2. The maximum programming time is measured after 10K erase operations.

**Table 53. Flash memory endurance and data retention**

| Symbol | Parameter | Conditions | Value | Unit |
|---|---|---|---|---|
| | | | Min(1) | |
| $N_{END}$ | Endurance | $T_J$ = –40 to +125 °C (6 suffix versions) | 10 | kcycles |
| $t_{RET}$ | Data retention | 1 kcycle at $T_A$ = 85 °C | 30 | Years |
| | | 10 kcycles at $T_A$ = 55 °C | 20 | |

1. Guaranteed by characterization results.

**Figure 24. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms**



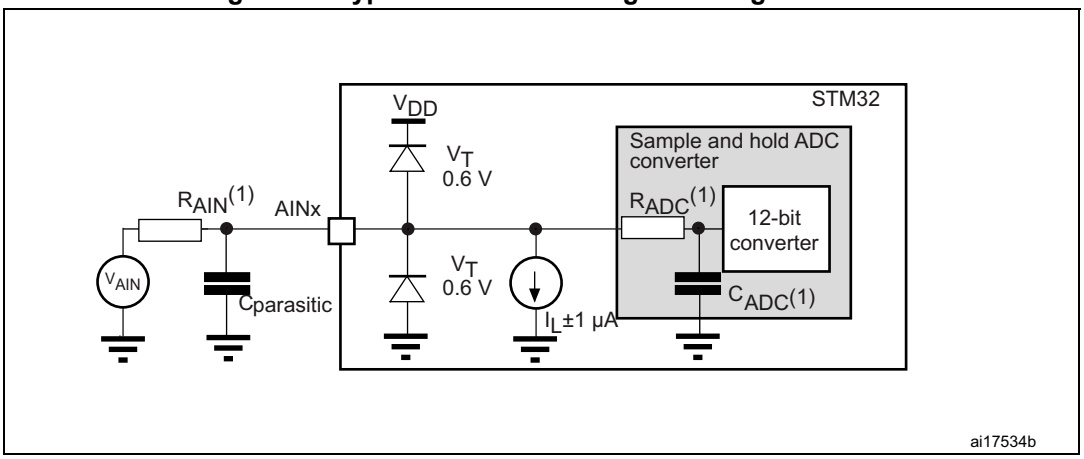

1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

**Table 66. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FMC_NE low time | $3T_{fmc\_ker\_ck} - 1$ | $3T_{fmc\_ker\_ck}$ | ns |
| $t_{v(NWE\_NE)}$ | FMC_NEx low to FMC_NWE low | $T_{fmc\_ker\_ck}$ | $T_{fmc\_ker\_ck} + 1$ | |
| $t_{w(NWE)}$ | FMC_NWE low time | $T_{fmc\_ker\_ck} - 0.5$ | $T_{fmc\_ker\_ck} + 0.5$ | |
| $t_{h(NE\_NWE)}$ | FMC_NWE high to FMC_NE high hold time | $T_{fmc\_ker\_ck}$ | - | |
| $t_{v(A\_NE)}$ | FMC_NEx low to FMC_A valid | - | 2 | |
| $t_{h(A\_NWE)}$ | Address hold time after FMC_NWE high | $T_{fmc\_ker\_ck} - 0.5$ | - | |
| $t_{v(BL\_NE)}$ | FMC_NEx low to FMC_BL valid | - | 0.5 | |
| $t_{h(BL\_NWE)}$ | FMC_BL hold time after FMC_NWE high | $T_{fmc\_ker\_ck} - 0.5$ | - | |
| $t_{v(Data\_NE)}$ | Data to FMC_NEx low to Data valid | - | $T_{fmc\_ker\_ck} + 2.5$ | |
| $t_{h(Data\_NWE)}$ | Data hold time after FMC_NWE high | $T_{fmc\_ker\_ck}+0.5$ | - | |
| $t_{v(NADV\_NE)}$ | FMC_NEx low to FMC_NADV low | - | 0 | |
| $t_{w(NADV)}$ | FMC_NADV low time | - | $T_{fmc\_ker\_ck} + 1$ | |

1. Guaranteed by characterization results.

**Figure 40. Typical connection diagram using the ADC**




1. Refer to *Table 85* for the values of $R_{AIN}$, $R_{ADC}$ and $C_{ADC}$.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 5 pF). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, $f_{ADC}$ should be reduced.

### 6.3.21 DAC electrical characteristics

**Table 87. DAC characteristics(1)**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage | - | | 1.8 | 3.3 | 3.6 | V |
| $V_{REF+}$ | Positive reference voltage | - | | 1.80 | - | $V_{DDA}$ | |
| $V_{REF-}$ | Negative reference voltage | - | | - | $V_{SSA}$ | - | |
| $R_L$ | Resistive Load | DAC output buffer ON | connected to $V_{SSA}$ | 5 | - | - | kΩ |
| | | | connected to $V_{DDA}$ | 25 | - | - | |
| $R_O$(2) | Output Impedance | DAC output buffer OFF | | 10.3 | 13 | 16 | |
| $R_{BON}$ | Output impedance sample and hold mode, output buffer ON | DAC output buffer ON | $V_{DD}$ = 2.7 V | - | - | 1.6 | kΩ |
| | | | $V_{DD}$ = 2.0 V | - | - | 2.6 | |
| $R_{BOFF}$ | Output impedance sample and hold mode, output buffer OFF | DAC output buffer OFF | $V_{DD}$ = 2.7 V | - | - | 17.8 | kΩ |
| | | | $V_{DD}$ = 2.0 V | - | - | 18.7 | |
| $C_L$(2) | Capacitive Load | DAC output buffer OFF | | - | - | 50 | pF |
| $C_{SH}$(2) | | Sample and Hold mode | | - | 0.1 | 1 | µF |
| $V_{DAC\_OUT}$ | Voltage on DAC_OUT output | DAC output buffer ON | | 0.2 | - | $V_{REF+}$ −0.2 | V |
| | | DAC output buffer OFF | | 0 | - | $V_{REF+}$ | |
| $t_{SETTLING}$ | Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches the final value of ±0.5LSB, ±1LSB, ±2LSB, ±4LSB, ±8LSB) | Normal mode, DAC output buffer OFF, ±1LSB $C_L$=10 pF | | - | 1.7(2) | 2(2) | µs |
| $t_{WAKEUP}$(3) | Wakeup time from off state (setting the Enx bit in the DAC Control register) until the ±1LSB final value | Normal mode, DAC output buffer ON, $C_L \leq 50$ pF, $R_L = 5$ kΩ | | - | 5 | 7.5 | µs |
| $V_{offset}$(2) | Middle code offset for 1 trim code step | $V_{REF+}$ = 3.6 V | | - | 850 | - | µV |
| | | $V_{REF+}$ = 1.8 V | | - | 425 | - | |

**Table 96. OPAMP characteristics(1) (continued)**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| en | Voltage noise density | at 1 KHz | output loaded with 4 kΩ | - | 140 | - | nV/√Hz |
| | | at 10 KHz | | - | 55 | - | |
| $I_{DDA(OPAMP)}$ | OPAMP consumption from $V_{DDA}$ | Normal mode | no Load, quiescent mode, follower | - | 570 | 1000 | µA |
| | | High-speed mode | | - | 610 | 1200 | |

1. Guaranteed by design, unless otherwise specified.
2. $R_{LOAD}$ is the resistive load connected to VSSA or to VDDA.
3. R2 is the internal resistance between the OPAMP output and th OPAMP inverting input. R1 is the internal resistance between the OPAMP inverting input and ground. PGA gain = 1 + R2/R1.

**Figure 60. Ethernet SMI timing diagram**

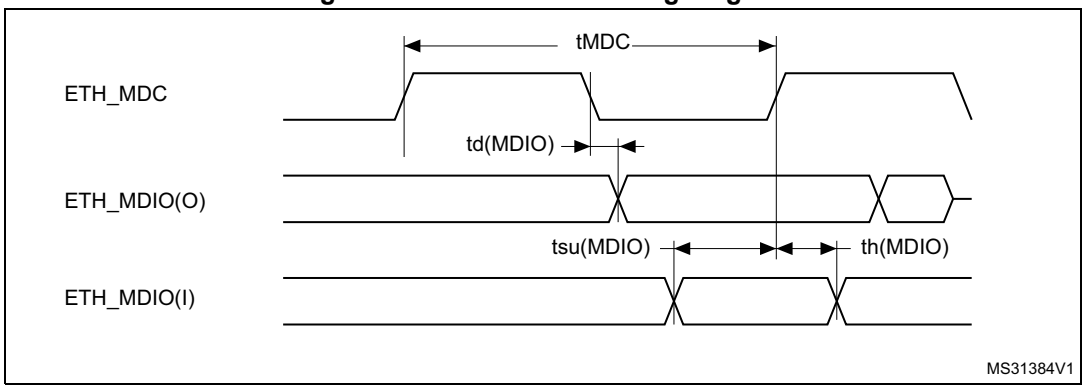



*Table 112* gives the list of Ethernet MAC signals for the RMII and *Figure 61* shows the corresponding timing diagram.

**Table 112. Dynamics characteristics: Ethernet MAC signals for RMII(1)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{su(RXD)}$ | Receive data setup time | 2 | - | - | ns |
| $t_{ih(RXD)}$ | Receive data hold time | 3 | - | - | |
| $t_{su(CRS)}$ | Carrier sense setup time | 2.5 | - | - | |
| $t_{ih(CRS)}$ | Carrier sense hold time | 2 | - | - | |
| $t_{d(TXEN)}$ | Transmit enable valid delay time | 4 | 4.5 | 7 | |
| $t_{d(TXD)}$ | Transmit data valid delay time | 7 | 7.5 | 11.5 | |

1. Guaranteed by characterization results.

**Figure 61. Ethernet RMII timing diagram**

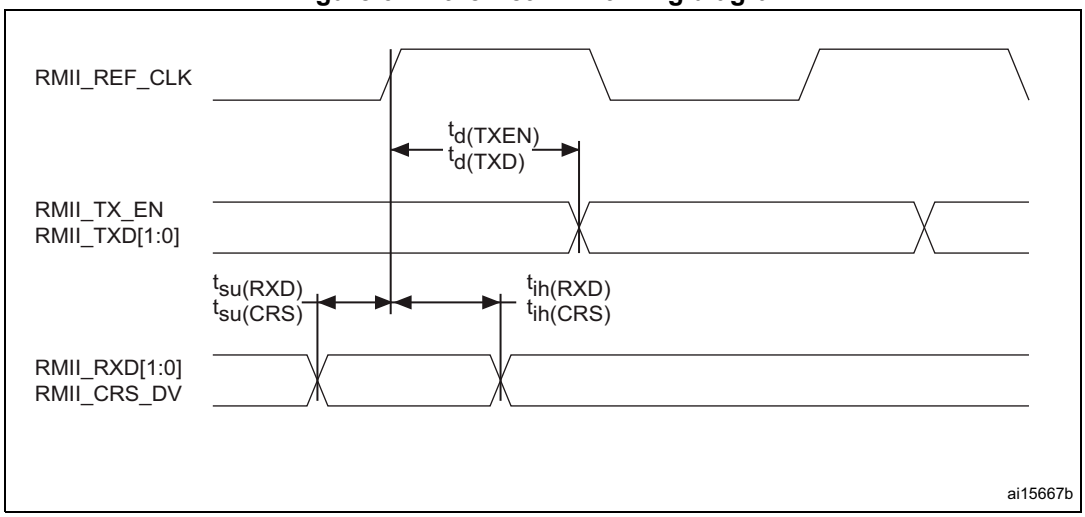



*Table 113* gives the list of Ethernet MAC signals for MII and *Figure 62* shows the corresponding timing diagram.

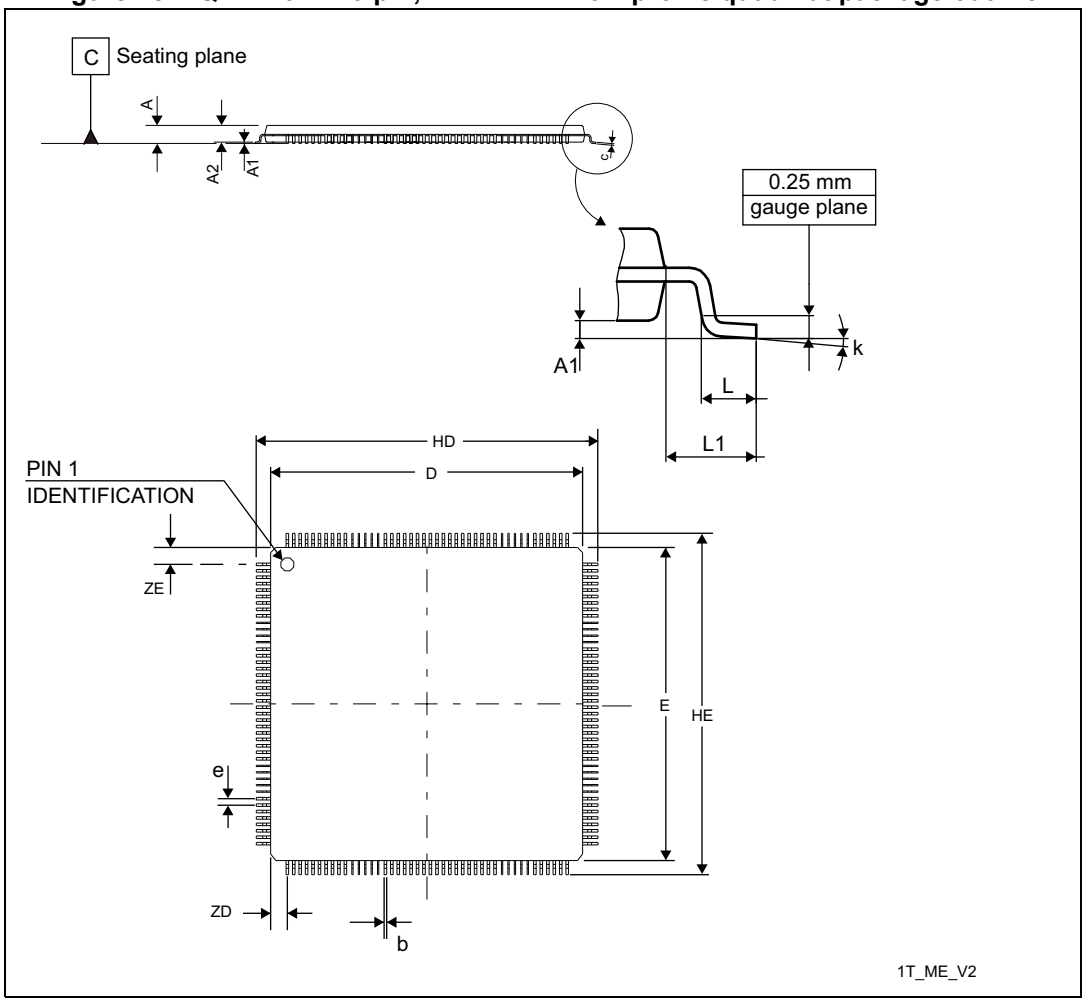
**Table 120. UFBGA169 - 169-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| F | 0.450 | 0.500 | 0.550 | 0.0177 | 0.0197 | 0.0217 |
| ddd | - | - | 0.100 | - | - | 0.0039 |
| eee | - | - | 0.150 | - | - | 0.0059 |
| fff | - | - | 0.050 | - | - | 0.0020 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

## 7.5 LQFP176 package information

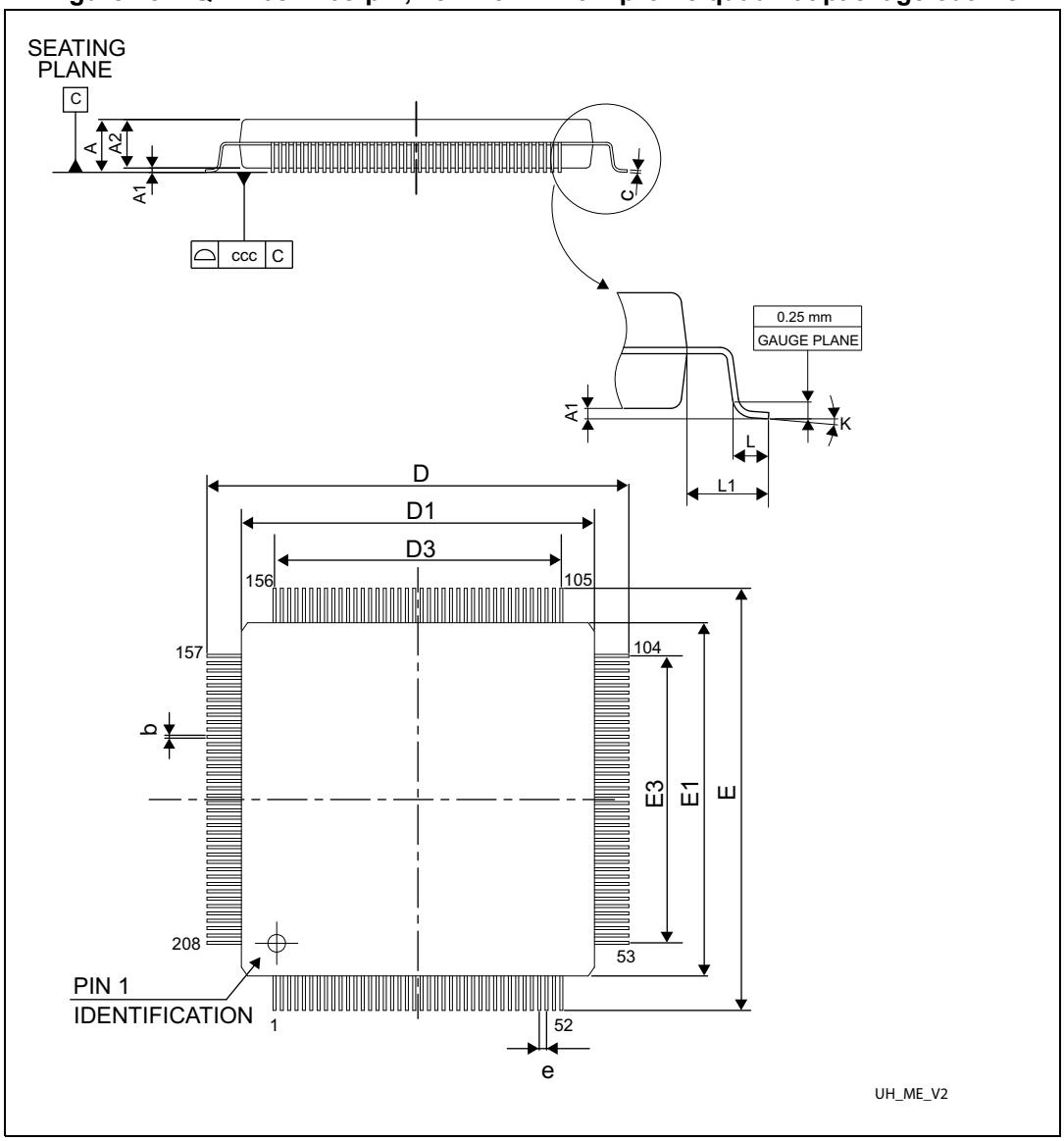
**Figure 75. LQFP176 - 176-pin, 24 x 24 mm low profile quad flat package outline**




1. Drawing is not to scale.

## 7.6 LQFP208 package information

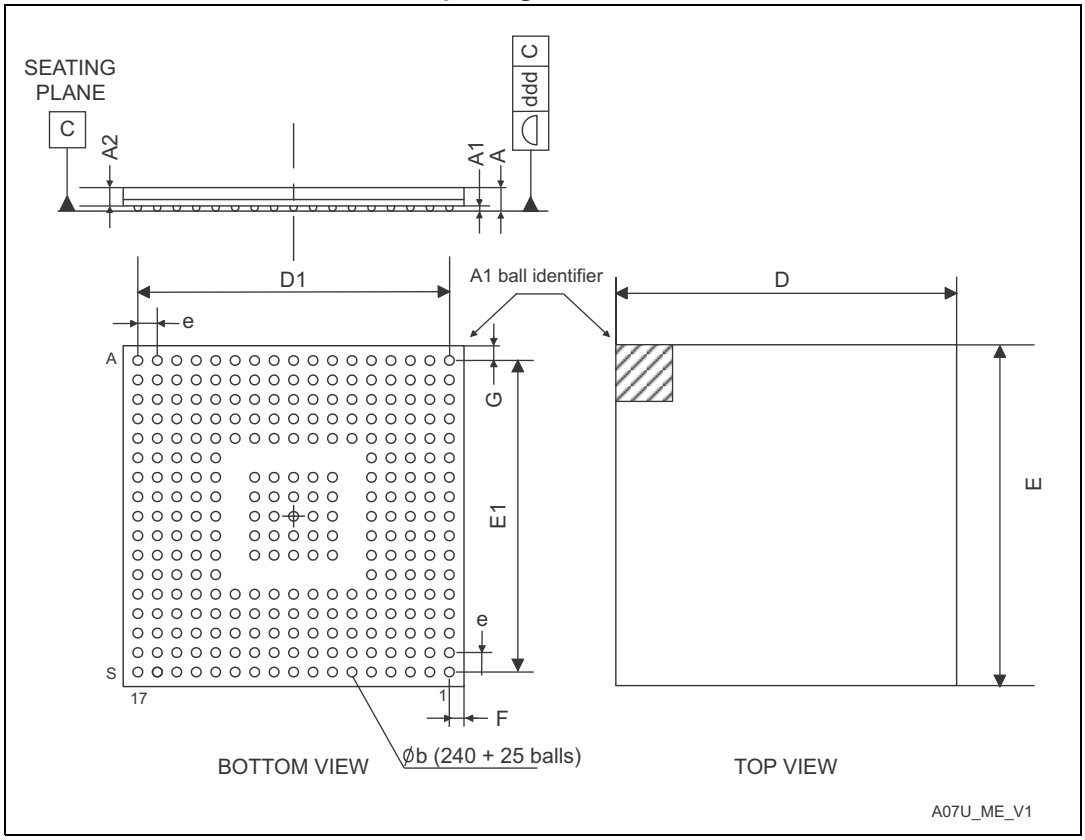
**Figure 78. LQFP208 - 208-pin, 28 x 28 mm low-profile quad flat package outline**




1. Drawing is not to scale.

## 7.8 TFBGA240+25 package information

**Figure 84. TFBGA - 240+25 ball, 14x14 mm, 0.8 mm pitch, fine pitch ball grid array package outline**




1. Dimensions are expressed in millimeters.