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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	480MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, IrDA, LINbus, MDIO, MMC/SD/SDIO, QSPI, SAI, SPDIF, SPI, SWPMI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, LCD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1M x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 36x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32h743vit6

Contents

1	Introduction	12
2	Description	13
3	Functional overview	18
3.1	Arm® Cortex®-M7 with FPU	18
3.2	Memory protection unit (MPU)	18
3.3	Memories	19
3.3.1	Embedded Flash memory	19
3.3.2	Embedded SRAM	19
3.4	Boot modes	20
3.5	Power supply management	20
3.5.1	Power supply scheme	20
3.5.2	Power supply supervisor	22
3.5.3	Voltage regulator	22
3.6	Low-power strategy	23
3.7	Reset and clock controller (RCC)	24
3.7.1	Clock management	24
3.7.2	System reset sources	24
3.8	General-purpose input/outputs (GPIOs)	25
3.9	Bus-interconnect matrix	25
3.10	DMA controllers	27
3.11	Chrom-ART Accelerator™ (DMA2D)	27
3.12	Nested vectored interrupt controller (NVIC)	28
3.13	Extended interrupt and event controller (EXTI)	28
3.14	Cyclic redundancy check calculation unit (CRC)	28
3.15	Flexible memory controller (FMC)	29
3.16	Quad-SPI memory interface (QUADSPI)	29
3.17	Analog-to-digital converters (ADCs)	29
3.18	Temperature sensor	30
3.19	V _{BAT} operation	30
3.20	Digital-to-analog converters (DAC)	31

5	Pin descriptions	48
6	Electrical characteristics	96
6.1	Parameter conditions	96
6.1.1	Minimum and maximum values	96
6.1.2	Typical values	96
6.1.3	Typical curves	96
6.1.4	Loading capacitor	96
6.1.5	Pin input voltage	96
6.1.6	Power supply scheme	97
6.1.7	Current consumption measurement	98
6.2	Absolute maximum ratings	98
6.3	Operating conditions	100
6.3.1	General operating conditions	100
6.3.2	VCAP external capacitor	101
6.3.3	Operating conditions at power-up / power-down	101
6.3.4	Embedded reset and power control block characteristics	102
6.3.5	Embedded reference voltage	103
6.3.6	Supply current characteristics	104
6.3.7	Wakeup time from low-power modes	117
6.3.8	External clock source characteristics	118
6.3.9	Internal clock source characteristics	122
6.3.10	PLL characteristics	124
6.3.11	Memory characteristics	126
6.3.12	EMC characteristics	128
6.3.13	Absolute maximum ratings (electrical sensitivity)	129
6.3.14	I/O current injection characteristics	130
6.3.15	I/O port characteristics	131
6.3.16	NRST pin characteristics	137
6.3.17	FMC characteristics	138
6.3.18	Quad-SPI interface characteristics	158
6.3.19	Delay block (DLYB) characteristics	160
6.3.20	16-bit ADC characteristics	160
6.3.21	DAC electrical characteristics	166
6.3.22	Voltage reference buffer characteristics	169
6.3.23	Temperature sensor characteristics	170
6.3.24	V _{BAT} monitoring characteristics	171

Table 45.	HSI48 oscillator characteristics	122
Table 46.	HSI oscillator characteristics	123
Table 47.	CSI oscillator characteristics	123
Table 48.	LSI oscillator characteristics	124
Table 49.	PLL characteristics (wide VCO frequency range)	124
Table 50.	PLL characteristics (medium VCO frequency range)	125
Table 51.	Flash memory characteristics	126
Table 52.	Flash memory programming (single bank configuration nDBANK=1)	127
Table 53.	Flash memory endurance and data retention	127
Table 54.	EMS characteristics	128
Table 55.	EMI characteristics	129
Table 56.	ESD absolute maximum ratings	129
Table 57.	Electrical sensitivities	130
Table 58.	I/O current injection susceptibility	130
Table 59.	I/O static characteristics	131
Table 60.	Output voltage characteristics	133
Table 61.	Output timing characteristics (HSLV OFF)	134
Table 62.	Output timing characteristics (HSLV ON)	136
Table 63.	NRST pin characteristics	137
Table 64.	Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings	140
Table 65.	Asynchronous non-multiplexed SRAM/PSRAM/NOR read - NWAIT timings	140
Table 66.	Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings	141
Table 67.	Asynchronous non-multiplexed SRAM/PSRAM/NOR write - NWAIT timings	142
Table 68.	Asynchronous multiplexed PSRAM/NOR read timings	143
Table 69.	Asynchronous multiplexed PSRAM/NOR read-NWAIT timings	143
Table 70.	Asynchronous multiplexed PSRAM/NOR write timings	144
Table 71.	Asynchronous multiplexed PSRAM/NOR write-NWAIT timings	145
Table 72.	Synchronous multiplexed NOR/PSRAM read timings	147
Table 73.	Synchronous multiplexed PSRAM write timings	149
Table 74.	Synchronous non-multiplexed NOR/PSRAM read timings	150
Table 75.	Synchronous non-multiplexed PSRAM write timings	151
Table 76.	Switching characteristics for NAND Flash read cycles	154
Table 77.	Switching characteristics for NAND Flash write cycles	154
Table 78.	SDRAM read timings	155
Table 79.	LPSDR SDRAM read timings	156
Table 80.	SDRAM write timings	157
Table 81.	LPSDR SDRAM write timings	157
Table 82.	Quad-SPI characteristics in SDR mode	158
Table 83.	Quad SPI characteristics in DDR mode	159
Table 84.	Dynamics characteristics: Delay Block characteristics	160
Table 85.	ADC characteristics	160
Table 86.	ADC accuracy	162
Table 87.	DAC characteristics	166
Table 88.	DAC accuracy	167
Table 89.	VREFBUF characteristics	169
Table 90.	Temperature sensor characteristics	170
Table 91.	Temperature sensor calibration values	170
Table 92.	V _{BAT} monitoring characteristics	171
Table 93.	V _{BAT} charging characteristics	171
Table 94.	Voltage booster for analog switch characteristics	171
Table 95.	COMP characteristics	172
Table 96.	OPAMP characteristics	173

List of figures

Figure 1.	STM32H743xI block diagram	17
Figure 2.	Power-up/power-down sequence	21
Figure 3.	STM32H743xI bus matrix	26
Figure 4.	LQFP100 pinout	48
Figure 5.	TFBGA100 pinout	49
Figure 6.	LQFP144 pinout	50
Figure 7.	UFBGA169 ballout	51
Figure 8.	LQFP176 pinout	52
Figure 9.	UFBGA176+25 ballout	53
Figure 10.	LQFP208 pinout	54
Figure 11.	TFBGA240+25 ballout	55
Figure 12.	Pin loading conditions	96
Figure 13.	Pin input voltage	96
Figure 14.	Power supply scheme	97
Figure 15.	Current consumption measurement scheme	98
Figure 16.	External capacitor C_{EXT}	101
Figure 17.	High-speed external clock source AC timing diagram	118
Figure 18.	Low-speed external clock source AC timing diagram	119
Figure 19.	Typical application with an 8 MHz crystal	121
Figure 20.	Typical application with a 32.768 kHz crystal	122
Figure 21.	VIL/VIH for all I/Os except BOOT0	132
Figure 22.	Recommended NRST pin protection	137
Figure 23.	Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms	139
Figure 24.	Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms	141
Figure 25.	Asynchronous multiplexed PSRAM/NOR read waveforms	142
Figure 26.	Asynchronous multiplexed PSRAM/NOR write waveforms	144
Figure 27.	Synchronous multiplexed NOR/PSRAM read timings	146
Figure 28.	Synchronous multiplexed PSRAM write timings	148
Figure 29.	Synchronous non-multiplexed NOR/PSRAM read timings	150
Figure 30.	Synchronous non-multiplexed PSRAM write timings	151
Figure 31.	NAND controller waveforms for read access	152
Figure 32.	NAND controller waveforms for write access	153
Figure 33.	NAND controller waveforms for common memory read access	153
Figure 34.	NAND controller waveforms for common memory write access	154
Figure 35.	SDRAM read access waveforms (CL = 1)	155
Figure 36.	SDRAM write access waveforms	156
Figure 37.	Quad-SPI timing diagram - SDR mode	159
Figure 38.	Quad-SPI timing diagram - DDR mode	159
Figure 39.	ADC accuracy characteristics (12-bit resolution)	163
Figure 40.	Typical connection diagram using the ADC	164
Figure 41.	Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})	165
Figure 42.	Power supply and reference decoupling (V_{REF+} connected to V_{DDA})	165
Figure 43.	12-bit buffered /non-buffered DAC	168
Figure 44.	Channel transceiver timing diagrams	178
Figure 45.	DCMI timing diagram	179
Figure 46.	LCD-TFT horizontal timing diagram	181
Figure 47.	LCD-TFT vertical timing diagram	181
Figure 48.	SPI timing diagram - slave mode and CPHA = 0	185

3.6 Low-power strategy

There are several ways to reduce power consumption on STM32H743xI:

- Decrease dynamic power consumption by slowing down the system clocks even in Run mode and individually clock gating the peripherals that are not used.
- Save power consumption when the CPU is idle, by selecting among the available low-power mode according to the user application needs. This allows achieving the best compromise between short startup time, low-power consumption, as well as available wakeup sources.

The devices feature several low-power modes:

- CSleep (CPU clock stopped)
- CStop (CPU sub-system clock stopped)
- DStop (Domain bus matrix clock stopped)
- Stop (System clock stopped)
- DStandby (Domain powered down)
- Standby (System powered down)

CSleep and CStop low-power modes are entered by the MCU when executing the WFI (Wait for Interrupt) or WFE (Wait for Event) instructions, or when the SLEEPONEXIT bit of the Cortex[®]-Mx core is set after returning from an interrupt service routine.

A domain can enter low-power mode (DStop or DStandby) when the processor, its subsystem and the peripherals allocated in the domain enter low-power mode.

If part of the domain is not in low-power mode, the domain remains in the current mode.

Finally the system can enter Stop or Standby when all EXTI wakeup sources are cleared and the power domains are in DStop or DStandby mode.

Table 3. System vs domain low-power mode

System power mode	D1 domain power mode	D2 domain power mode	D3 domain power mode
Run	DRun/DStop/DStandby	DRun/DStop/DStandby	DRun
Stop	DStop/DStandby	DStop/DStandby	DStop
Standby	DStandby	DStandby	DStandby

3.12 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller which is able to manage 16 priority levels, and handle up to 150 maskable interrupt channels plus the 16 interrupt lines of the Cortex[®]-M7 with FPU core.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor context automatically saved on interrupt entry, and restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

3.13 Extended interrupt and event controller (EXTI)

The EXTI controller performs interrupt and event management. In addition, it can wake up the processor, power domains and/or D3 domain from Stop mode.

The EXTI handles up to 89 independent event/interrupt lines split as 28 configurable events and 61 direct events .

Configurable events have dedicated pending flags, active edge selection, and software trigger capable.

Direct events provide interrupts or events from peripherals having a status flag.

3.14 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a programmable polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.40 Universal serial bus on-the-go high-speed (OTG_HS)

The devices embed two USB OTG high-speed (up to 480 Mbit/s) device/host/OTG peripheral. OTG-HS1 supports both full-speed and high-speed operations, while OTG-HS2 supports only full-speed operations. They both integrate the transceivers for full-speed operation (12 Mbit/s) and are able to operate from the internal HSI48 oscillator. OTG-HS1 features a UTMI low-pin interface (ULPI) for high-speed operation (480 Mbit/s). When using the USB OTG-HS1 in HS mode, an external PHY device connected to the ULPI is required.

The USB OTG HS peripherals are compliant with the USB 2.0 specification and with the OTG 2.0 specification. They have software-configurable endpoint setting and supports suspend/resume. The USB OTG controllers require a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator.

The main features are:

- Combined Rx and Tx FIFO size of 4 Kbytes with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 9 bidirectional endpoints (including EP0)
- 16 host channels with periodic OUT support
- Software configurable to OTG1.3 and OTG2.0 modes of operation
- USB 2.0 LPM (Link Power Management) support
- Battery Charging Specification Revision 1.2 support
- Internal FS OTG PHY support
- External HS or HS OTG operation supporting ULPI in SDR mode (OTG_HS1 only)
The OTG PHY is connected to the microcontroller ULPI port through 12 signals. It can be clocked using the 60 MHz output.
- Internal USB DMA
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected

3.41 Ethernet MAC interface with dedicated DMA controller (ETH)

The devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for ethernet LAN communications through an industry-standard medium-independent interface (MII) or a reduced medium-independent interface (RMII). The microcontroller requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). The PHY is connected to the device MII port using 17 signals for MII or 9 signals for RMII, and can be clocked using the 25 MHz (MII) from the microcontroller.

Table 8. STM32H743xI pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
15	F1	26	J1	M2	32	35	L2	PC0	I/O	FT_a	-	DFSDM_CKIN0, DFSDM_DATIN4, SAI2_FS_B, OTG_HS_ULPI_STP, FMC_SDNWE, LCD_R5, EVENTOUT	ADC123_ INP10
16	F2	27	J2	M3	33	36	M2	PC1	I/O	FT_ha	-	TRACED0, SAI1_D1, DFSDM_DATIN0, DFSDM_CKIN4, SPI2_MOSI/I2S2_SDO, SAI1_SD_A, SAI4_SD_A, SDMMC2_CK, SAI4_D1, ETH_MDC, MDIOS_MDC, EVENTOUT	ADC123_ INN10, ADC123_ INP11, RTC_TAMP_3/ WKUP5
-	-	-	-	-	-	-	M3 ⁽⁵⁾	PC2	I/O	FT_a	-	DFSDM_CKIN1, SPI2_MISO/I2S2_SDI, DFSDM_CKOUT, OTG_HS_ULPI_DIR, ETH_MII_TXD2, FMC_SDNE0, EVENTOUT	ADC123_ INN11, ADC123_ INP12
17 ⁽⁶⁾	E2 ⁽⁶⁾	28 ⁽⁶⁾	K2 ⁽⁶⁾	M4 ⁽⁶⁾	34 ⁽⁶⁾	37 ⁽⁶⁾	R1 ⁽⁵⁾	PC2_C	ANA	TT_a	-	-	ADC3_INN1, ADC3_INP0
-	-	-	-	-	-	-	M4 ⁽⁵⁾	PC3	I/O	FT_a	-	DFSDM_DATIN1, SPI2_MOSI/I2S2_SDO, OTG_HS_ULPI_NXT, ETH_MII_TX_CLK, FMC_SDCKE0, EVENTOUT	ADC12_INN12, ADC12_INP13
18 ⁽⁶⁾	F3 ⁽⁶⁾	29 ⁽⁶⁾	K1 ⁽⁶⁾	M5 ⁽⁶⁾	35 ⁽⁶⁾	38 ⁽⁶⁾	R2 ⁽⁵⁾	PC3_C	ANA	TT_a	-	-	ADC3_INP1
-	F5	30	-	G3	36	39	E11	VDD	S	-	-	-	-
-	E6	-	B3	J10	-	-	C13	VSS	S	-	-	-	-
19	G1	31	J3	M1	37	40	P1	VSSA	S	-	-	-	-
-	-	-	-	N1	-	-	N1	VREF-	S	-	-	-	-
20	-(7)	32	L2	P1	38	41	M1	VREF+	S	-	-	-	-
21	H1	33	L1	R1	39	42	L1	VDDA	S	-	-	-	-

Table 8. STM32H743xl pin/ball definition (continued)

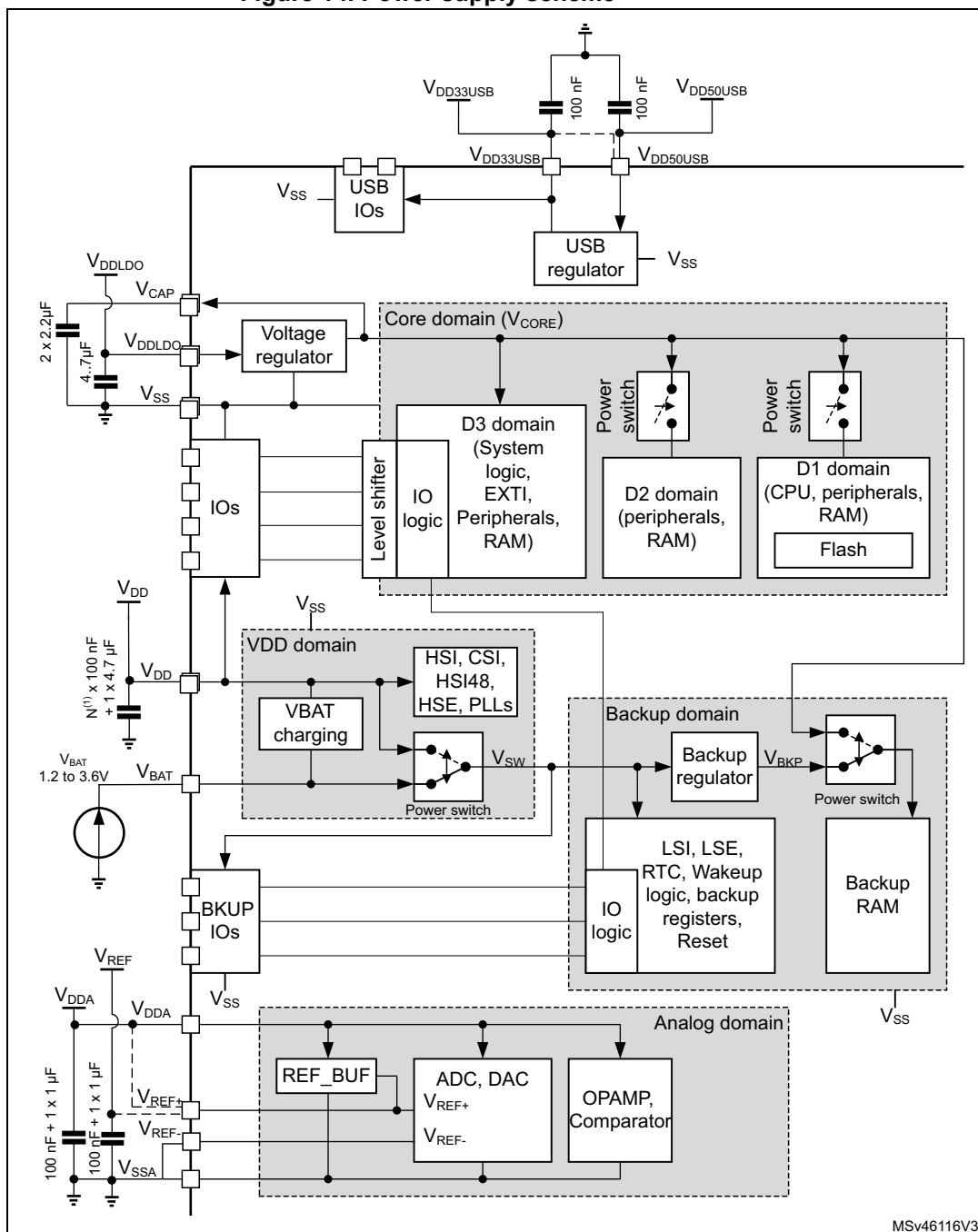
Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
-	-	-	-	M12	85	98	T13	PH8	I/O	FT_fh a	-	TIM5_ETR, I2C3_SDA, FMC_D16, DCMI_HSYNC, LCD_R2, EVENTOUT	-
-	-	-	-	F8	-	-	M15	VSS	S	-	-	-	-
-	-	-	L13	-	-	-	M13	VDD	S	-	-	-	-
-	-	-	-	M13	86	99	R13	PH9	I/O	FT_h	-	TIM12_CH2, I2C3_SMBA, FMC_D17, DCMI_D0, LCD_R3, EVENTOUT	-
-	-	-	K9	L13	87	100	P13	PH10	I/O	FT_h	-	TIM5_CH1, I2C4_SMBA, FMC_D18, DCMI_D1, LCD_R4, EVENTOUT	-
-	-	-	L10	L12	88	101	P14	PH11	I/O	FT_fh	-	TIM5_CH2, I2C4_SCL, FMC_D19, DCMI_D2, LCD_R5, EVENTOUT	-
-	-	-	K10	K12	89	102	R14	PH12	I/O	FT_fh	-	TIM5_CH3, I2C4_SDA, FMC_D20, DCMI_D3, LCD_R6, EVENTOUT	-
-	-	-	-	H12	90	-	N16	VSS	S	-	-	-	-
-	-	-	N11	J12	91	103	P17	VDD	S	-	-	-	-
51	K8	73	N12	P12	92	104	T14	PB12	I/O	FT_u	-	TIM1_BKIN, I2C2_SMBA, SPI2_NSS/I2S2_WS, DFSDM_DATIN1, USART3_CK, FDCAN2_RX, OTG_HS_ULPI_D5, ETH_MII_TXD0/ETH_RMII_TXD0, OTG_HS_ID, TIM1_BKIN_COMP12, UART5_RX, EVENTOUT	
52	J8	74	L11	P13	93	105	U14	PB13	I/O	FT_u	-	TIM1_CH1N, LPTIM2_OUT, SPI2_SCK/I2S2_CK, DFSDM_CKIN1, USART3_CTS_NSS, FDCAN2_TX, OTG_HS_ULPI_D6, ETH_MII_TXD1/ETH_RMII_TXD1, UART5_TX, EVENTOUT	OTG_HS_VBUS

**Table 11. Port C alternate functions (continued)**

Port	AF0		AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
	SYS		TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM/CEC	SP11/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD	I2C4/UART7/SWPMI1/TIM1/8/DFSDM/SDMMC2/MDIOS/ETH	TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD	TIM1/DCMI/LCD/COMP	UART5/LCD	SYS
Port C	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT-OUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT-OUT

6.1.6 Power supply scheme

Figure 14. Power supply scheme



1. N corresponds to the number of VDD pins available on the package.
2. A tolerance of +/- 20% is acceptable on decoupling capacitors.

Caution: Each power supply pair (V_{DD}/V_{SS} , V_{DDA}/V_{SSA} ...) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure good operation of the

Table 50. PLL characteristics (medium VCO frequency range)⁽¹⁾ (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Jitter	Cycle-to-cycle jitter ⁽³⁾	-	VCO = 150 MHz	-	145	-	+/- ps
			VCO = 300 MHz	-	91	-	
			VCO = 400 MHz	-	64	-	
			VCO = 420 MHz	-	63	-	
	Period jitter	$f_{\text{PLL_OUT}} = 50 \text{ MHz}$	VCO = 150 MHz	-	55	-	+/- ps
			VCO = 400 MHz	-	30	-	
	Long term jitter	Normal mode	VCO = 150 MHz	-	-	-	%
			VCO = 300 MHz	-	-	-	
			VCO = 400 MHz	-	+/-0.3	-	
$I(\text{PLL})^{(2)}$	PLL power consumption on V_{DD}	VCO freq = 420MHz	VDD	-	440	1150	μA
			VCORE	-	530	-	
		VCO freq = 150MHz	VDD	-	180	500	
			VCORE	-	200	-	

1. Guaranteed by design unless otherwise specified.

2. Guaranteed by characterization results.

3. Integer mode only.

6.3.11 Memory characteristics

Flash memory

The characteristics are given at $T_J = -40$ to 125°C unless otherwise specified.

The devices are shipped to customers with the Flash memory erased.

Table 51. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	Write / Erase 8-bit mode	-	6.5	-	mA
		Write / Erase 16-bit mode	-	11.5	-	
		Write / Erase 32-bit mode	-	20	-	
		Write / Erase 64-bit mode	-	35	-	

Table 52. Flash memory programming (single bank configuration nDBANK=1)

Symbol	Parameter	Conditions	Min ⁽¹⁾	Typ	Max ⁽¹⁾	Unit
t_{prog}	Word (266 bits) programming time	Program/erase parallelism x 8	-	290	580 ⁽²⁾	μs
		Program/erase parallelism x 16	-	180	360	
		Program/erase parallelism x 32	-	130	260	
		Program/erase parallelism x 64	-	100	200	
$t_{\text{ERASE128KB}}$	Sector (128 KB) erase time	Program/erase parallelism x 8	-	2	4	s
		Program/erase parallelism x 16	-	1.8	3.6	
		Program/erase parallelism x 32	-			
t_{ME}	Mass erase time	Program/erase parallelism x 8	-	13	26	
		Program/erase parallelism x 16	-	8	16	
		Program/erase parallelism x 32	-	6	12	
		Program/erase parallelism x 64	-	5	10	
V_{prog}	Programming voltage	Program parallelism x 8	1.62	-	3.6	V
		Program parallelism x 16				
		Program parallelism x 32				
		Program parallelism x 64	1.8	-	3.6	

1. Guaranteed by characterization results.

2. The maximum programming time is measured after 10K erase operations.

Table 53. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value	Unit
			Min ⁽¹⁾	
N_{END}	Endurance	$T_J = -40$ to $+125$ °C (6 suffix versions)	10	kcycles
t_{RET}	Data retention	1 kcycle at $T_A = 85$ °C	30	Years
		10 kcycles at $T_A = 55$ °C	20	

1. Guaranteed by characterization results.

6.3.15 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in [Table 59: I/O static characteristics](#) are derived from tests performed under the conditions summarized in [Table 23: General operating conditions](#). All I/Os are CMOS and TTL compliant (except for BOOT0).

Table 59. I/O static characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{IL}^{(1)}$	I/O input low level voltage except BOOT0	$1.62\text{ V} < V_{DD} < 3.6\text{ V}$	-	-	$0.3 \times V_{DD}$	V
	I/O input low level voltage except BOOT0		-	-	$0.4 \times V_{DD} - 0.1$	
	BOOT0 I/O input low level voltage		-	-	$0.19 \times V_{DD} + 0.1$	
$V_{IH}^{(1)}$	I/O input high level voltage except BOOT0	$1.62\text{ V} < V_{DD} < 3.6\text{ V}$	$0.7 \times V_{DD}$	-	-	V
	I/O input low level voltage except BOOT0		$0.47 \times V_{DD} + 0.25$	-	-	
	BOOT0 I/O input high level voltage		$0.17 \times V_{DD} + 0.6$	-	-	
$V_{HYS}^{(1)}$	TT_XX, FT_XXX and NRST I/O input hysteresis	$1.62\text{ V} < V_{DD} < 3.6\text{ V}$	-	250	-	mV
	BOOT0 I/O input hysteresis		-	200	-	
R_{PU}	Weak pull-up equivalent resistor ⁽²⁾	$V_{IN} = V_{SS}$	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistor ⁽²⁾	$V_{IN} = V_{DD}^{(3)}$	30	40	50	
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Guaranteed by design.

2. The pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

3. Max(VDDXXX) is the maximum value of all the I/O supplies.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for FT I/Os is shown in [Figure 21](#).

6.3.16 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see [Table 59: I/O static characteristics](#)).

Unless otherwise specified, the parameters given in [Table 63](#) are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in [Table 23: General operating conditions](#).

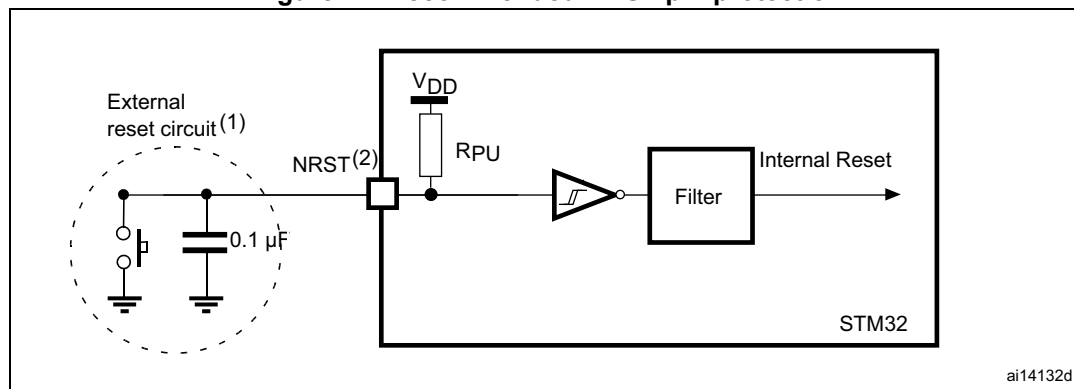
Table 63. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{PU}^{(2)}$	Weak pull-up equivalent resistor ⁽¹⁾	$V_{IN} = V_{SS}$	30	40	50	k Ω
$V_{F(NRST)}^{(2)}$	NRST Input filtered pulse	$1.71\text{ V} < V_{DD} < 3.6\text{ V}$	-	-	50	ns
$V_{NF(NRST)}^{(2)}$	NRST Input not filtered pulse	$1.71\text{ V} < V_{DD} < 3.6\text{ V}$	300	-	-	
		$1.62\text{ V} < V_{DD} < 3.6\text{ V}$	1000	-	-	

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

2. Guaranteed by design.

Figure 22. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in [Table 63](#). Otherwise the reset is not taken into account by the device.

Table 68. Asynchronous multiplexed PSRAM/NOR read timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{fmc_ker_ck} - 1$	$3T_{fmc_ker_ck} + 1$	ns
$t_{v(NOE_NE)}$	FMC_NEx low to FMC_NOE low	$2T_{fmc_ker_ck}$	$2T_{fmc_ker_ck} + 0.5$	
$t_{w(NOE)}$	FMC_NOE low time	$T_{fmc_ker_ck} - 1$	$T_{fmc_ker_ck} + 1$	
$t_{h(NE_NOE)}$	FMC_NOE high to FMC_NE high hold time	0	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	0.5	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	0	0.5	
$t_{w(NADV)}$	FMC_NADV low time	$T_{fmc_ker_ck} - 0.5$	$T_{fmc_ker_ck} + 1$	
$t_{h(AD_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high	$T_{fmc_ker_ck} + 0.5$	-	
$t_{h(A_NOE)}$	Address hold time after FMC_NOE high	$T_{fmc_ker_ck} - 0.5$	-	
$t_{h(BL_NOE)}$	FMC_BL time after FMC_NOE high	0	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	0.5	
$t_{su(Data_NE)}$	Data to FMC_NEx high setup time	$T_{fmc_ker_ck} - 2$	-	
$t_{su(Data_NOE)}$	Data to FMC_NOE high setup time	$T_{fmc_ker_ck} - 2$	-	
$t_{h(Data_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{h(Data_NOE)}$	Data hold time after FMC_NOE high	0	-	

1. Guaranteed by characterization results.

Table 69. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings⁽¹⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{fmc_ker_ck} - 1$	$8T_{fmc_ker_ck}$	ns
$t_{w(NOE)}$	FMC_NWE low time	$5T_{fmc_ker_ck} - 1.5$	$5T_{fmc_ker_ck} + 0.5$	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{fmc_ker_ck} + 3$	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{fmc_ker_ck}$	-	

1. Guaranteed by characterization results.

6.3.18 Quad-SPI interface characteristics

Unless otherwise specified, the parameters given in [Table 82](#) and [Table 83](#) for Quad-SPI are derived from tests performed under the ambient temperature, $f_{\text{rcc_c_ck}}$ frequency and V_{DD} supply voltage conditions summarized in [Table 23: General operating conditions](#), with the following configuration:

- Output speed is set to $\text{OSPEEDRy}[1:0] = 11$
- Measurement points are done at CMOS levels: $0.5V_{\text{DD}}$
- I/O compensation cell enabled
- HSLV activated when $V_{\text{DD}} \leq 2.7 \text{ V}$

Refer to [Section 6.3.15: I/O port characteristics](#) for more details on the input/output alternate function characteristics.

Table 82. Quad-SPI characteristics in SDR mode⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$F_{\text{ck1/t(CK)}}$	Quad-SPI clock frequency	$2.7 \text{ V} \leq V_{\text{DD}} < 3.6 \text{ V}$ $C_L = 20 \text{ pF}$	-	-	133	MHz
		$1.62 \text{ V} < V_{\text{DD}} < 3.6 \text{ V}$ $C_L = 15 \text{ pF}$	-	-	100	
$t_{\text{w(CKH)}}$	Quad-SPI clock high and low time	-	$t_{\text{(CK)}/2} - 0.5$	-	$t_{\text{(CK)}/2}$	ns
$t_{\text{w(CKL)}}$			$t_{\text{(CK)}/2}$	-	$t_{\text{(CK)}/2} + 0.5$	
$t_{\text{s(IN)}}$	Data input setup time	-	1.5	-	-	
$t_{\text{h(IN)}}$	Data input hold time		2	-	-	
$t_{\text{v(OUT)}}$	Data output valid time	-	-	1.5	2	
$t_{\text{h(OUT)}}$	Data output hold time	-	0.5	-	-	

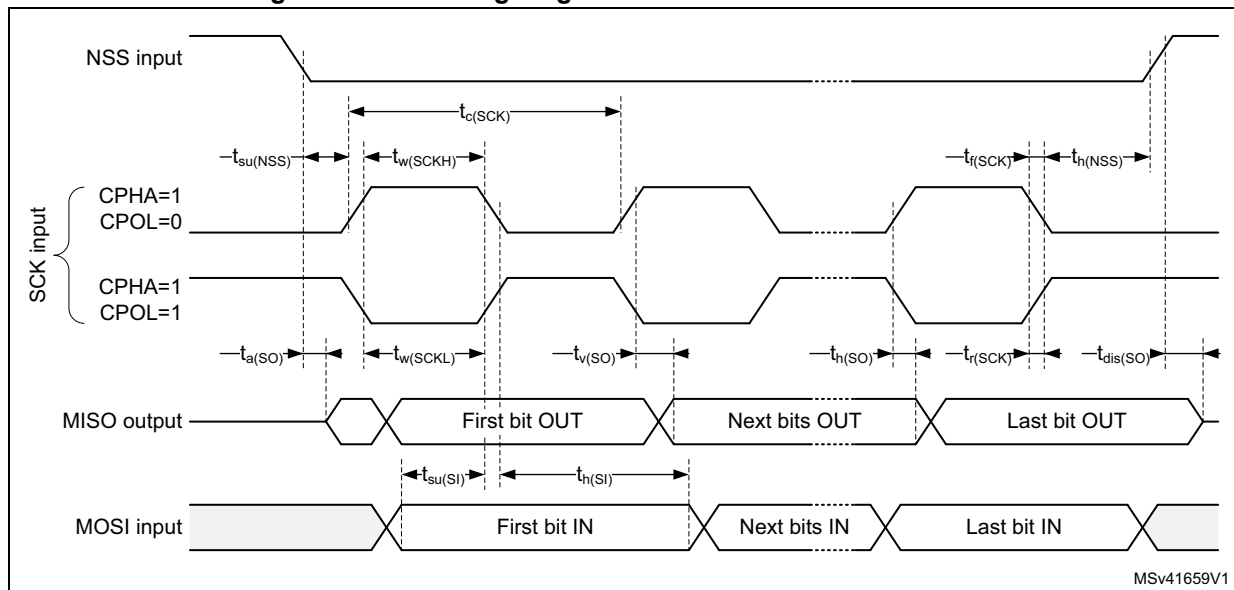
1. Guaranteed by characterization results.

Table 85. ADC characteristics⁽¹⁾ (continued)

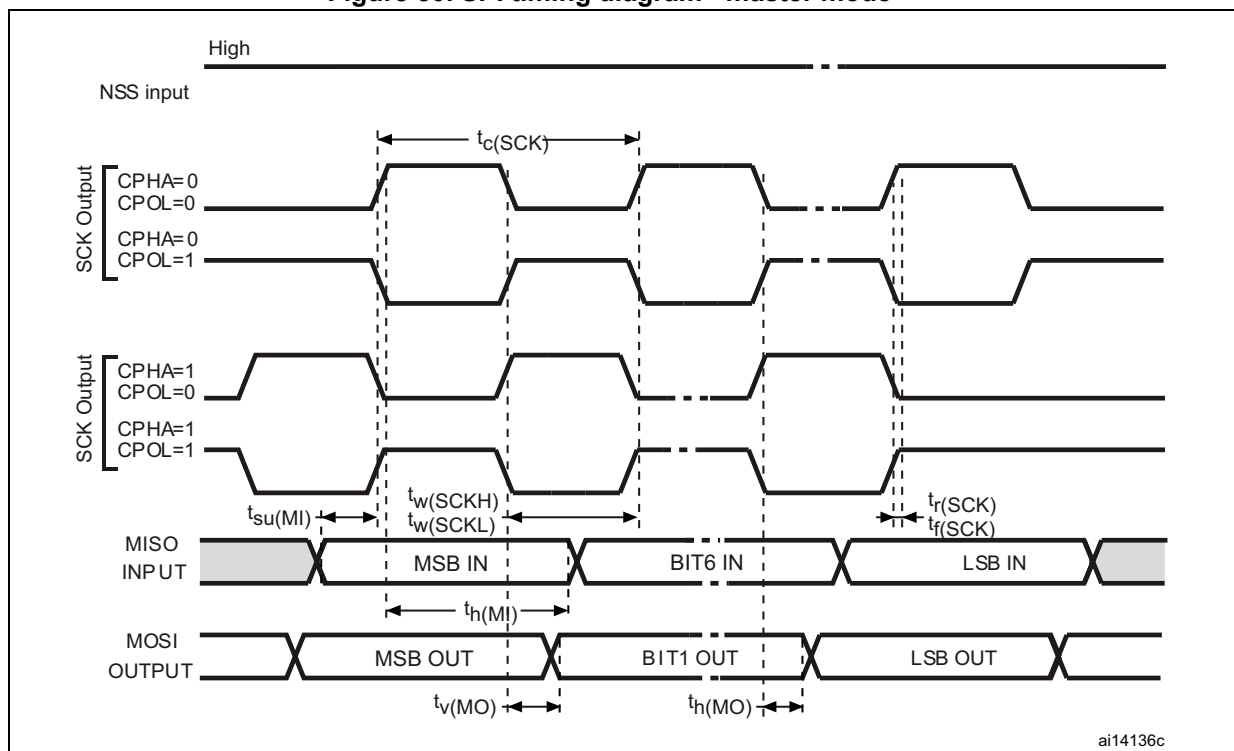
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f _{TRIG}	External trigger frequency	f _{ADC} = 36 MHz	-	-	3.6	MHz
		16-bit resolution	-	-	10	1/f _{ADC}
V _{AIN} ⁽²⁾	Conversion voltage range	-	0	-	V _{REF+}	V
V _{CMIV}	Common mode input voltage	-	V _{REF} /2-10%	V _{REF} /2	V _{REF} /2+10%	
R _{AIN}	External input impedance	-	-	-	50	kΩ
C _{ADC}	Internal sample and hold capacitor	-	-	4	-	pF
t _{ADCREG_STUP}	ADC LDO startup time	-	-	5	10	μs
t _{STAB}	ADC power-up time	LDO already started	1			conversion cycle
t _{CAL}	Offset and linearity calibration time	-	16384			1/f _{ADC}
t _{OFF_CAL}	Offset calibration time	-	1280			
t _{LATR}	Trigger conversion latency for regular and injected channels without aborting the conversion	CKMODE = 00	1.5	2	2.5	
		CKMODE = 01	-	-	2	
		CKMODE = 10			2.25	
		CKMODE = 11			2.125	
t _{LATRINJ}	Trigger conversion latency for regular and injected channels when a regular conversion is aborted	CKMODE = 00	2.5	3	3.5	
		CKMODE = 01	-	-	3	
		CKMODE = 10	-	-	3.25	
		CKMODE = 11	-	-	3.125	
t _S	Sampling time	-	1.5	-	640.5	
t _{CONV}	Total conversion time (including sampling time)	N-bit resolution	t _S + 0.5 + N/2 (9 to 648 cycles in 14-bit mode)			

1. Guaranteed by design.

2. Depending on the package, V_{REF+} can be internally connected to V_{DDA} and V_{REF-} to V_{SSA}.

Figure 49. SPI timing diagram - slave mode and CPHA = 1⁽¹⁾

1. Measurement points are done at $0.5V_{DD}$ and with external $C_L = 30$ pF.

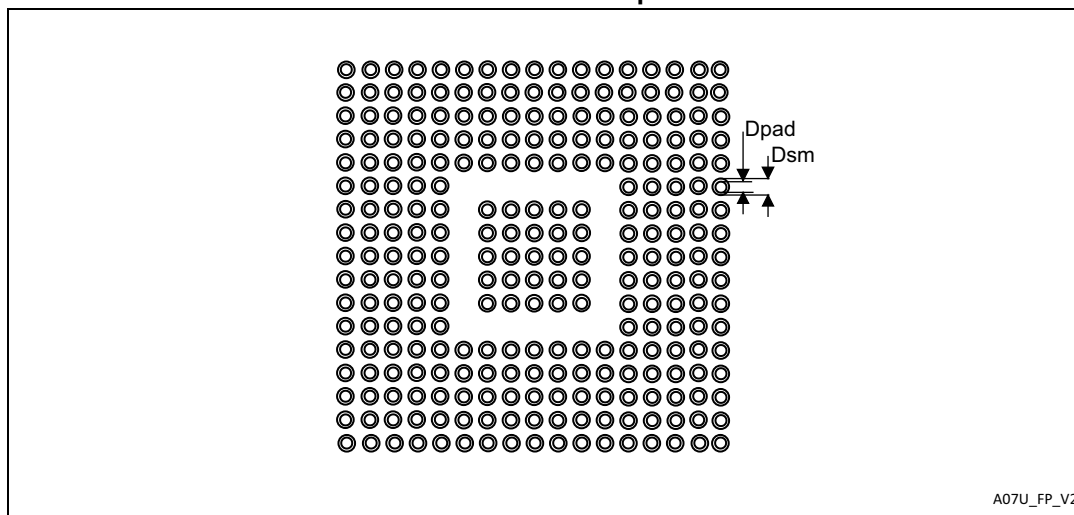
Figure 50. SPI timing diagram - master mode⁽¹⁾

1. Measurement points are done at $0.5V_{DD}$ and with external $C_L = 30$ pF.

Table 125. TFBG - 240 +25 ball, 14x14 mm, 0.8 mm pitch, fine pitch ball grid array mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.100	-	-	0.0433
A1	0.150	-	-	0.0059	-	-
A2	-	0.760	-	-	0.0299	-
b	0.350	0.400	0.450	0.0138	0.0157	0.0177
D	13.850	14.000	14.150	0.5453	0.5512	0.5571
D1	-	12.800	-	-	0.5039	-
E	13.850	14.000	14.150	0.5453	0.5512	0.5571
E1	-	12.800	-	-	0.5039	-
e	-	0.800	-	-	0.0315	-
F	-	0.600	-	-	0.0236	-
G	-	0.600	-	-	0.0236	-
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 85. TFBGA - 240+25 ball, 14x14 mm 0.8 mm pitch recommended footprint

1. Dimensions are expressed in millimeters.