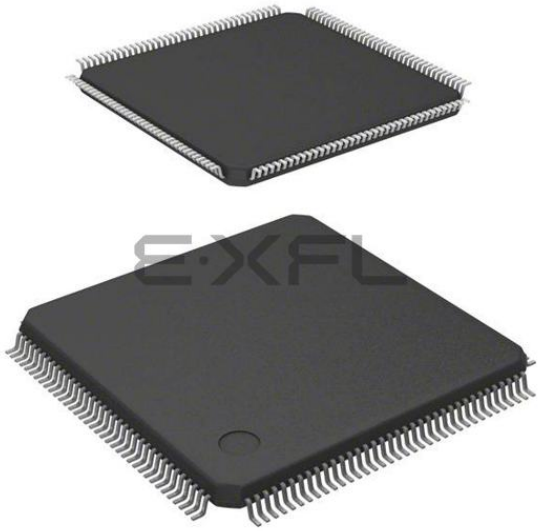

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	480MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MDIO, MMC/SD/SDIO, QSPI, SAI, SPDIF, SPI, SWPMI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	114
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1M x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 36x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32h743zit6

Contents

3.8 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

After reset, all GPIOs (except debug pins) are in Analog mode to reduce power consumption (refer to GPIOs register reset values in the device reference manual).

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.9 Bus-interconnect matrix

The devices feature an AXI bus matrix, two AHB bus matrices and bus bridges that allow interconnecting bus masters with bus slaves (see *Figure 3*).

3.25 LCD-TFT controller

The LCD-TFT display controller provides a 24-bit parallel digital RGB (Red, Green, Blue) and delivers all signals to interface directly to a broad range of LCD and TFT panels up to XGA (1024x768) resolution with the following features:

- 2 display layers with dedicated FIFO (64x64-bit)
- Color Look-Up table (CLUT) up to 256 colors (256x24-bit) per layer
- Up to 8 input color formats selectable per layer
- Flexible blending between two layers using alpha value (per pixel or constant)
- Flexible programmable parameters for each layer
- Color keying (transparency color)
- Up to 4 programmable interrupt events
- AXI master interface with burst of 16 words

3.26 JPEG Codec (JPEG)

The JPEG Codec can encode and decode a JPEG stream as defined in the ***ISO/IEC 10918-1*** specification. It provides an fast and simple hardware compressor and decompressor of JPEG images with full management of JPEG headers.

The JPEG codec main features are as follows:

- 8-bit/channel pixel depths
- Single clock per pixel encoding and decoding
- Support for JPEG header generation and parsing
- Up to four programmable quantization tables
- Fully programmable Huffman tables (two AC and two DC)
- Fully programmable minimum coded unit (MCU)
- Encode/decode support (non simultaneous)
- Single clock Huffman coding and decoding
- Two-channel interface: Pixel/Compress In, Pixel/Compressed Out
- Support for single greyscale component
- Ability to enable/disable header processing
- Fully synchronous design
- Configuration for High-speed decode mode

3.27 Random number generator (RNG)

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

3.28 Timers and watchdogs

The devices include one high-resolution timer, two advanced-control timers, ten general-purpose timers, two basic timers, five low-power timers, two watchdogs and a SysTick timer.

Table 8. STM32H743xI pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
58	G9	80	J10	N14	99	111	R15	PD11	I/O	FT_h	-	LPTIM2_IN2, I2C4_SMBA, USART3_CTS_NSS, QUADSPI_BK1_IO0, SAI2_SD_A, FMC_A16, EVENTOUT	-
59	K10	81	K13	N13	100	112	R16	PD12	I/O	FT_fh	-	LPTIM1_IN1, TIM4_CH1, LPTIM2_IN1, I2C4_SCL, USART3_RTS, QUADSPI_BK1_IO1, SAI2_FS_A, FMC_A17, EVENTOUT	-
60	J10	82	J11	M15	101	113	R17	PD13	I/O	FT_fh	-	LPTIM1_OUT, TIM4_CH2, I2C4_SDA, QUADSPI_BK1_IO3, SAI2_SCK_A, FMC_A18, EVENTOUT	-
-	-	83	-	K8	102	114	T12	VSS	S	-	-	-	-
-	-	84	-	J13	103	115	N11	VDD	S	-	-	-	-
61	H8	85	J13	M14	104	116	P16	PD14	I/O	FT_h	-	TIM4_CH3, SAI3_MCLK_B, UART8_CTS, FMC_D0/FMC_DA0, EVENTOUT	-
62	G8	86	J12	L14	105	117	P15	PD15	I/O	FT_h	-	TIM4_CH4, SAI3_MCLK_A, UART8_RTS, FMC_D1/FMC_DA1, EVENTOUT	-
-	-	-	-	-	-	118	N15	PJ6	I/O	FT	-	TIM8_CH2, LCD_R7, EVENTOUT	-
-	-	-	-	-	-	119	N14	PJ7	I/O	FT	-	TRGIN, TIM8_CH2N, LCD_G0, EVENTOUT	-
-	-	-	-	-	-	-	N10	VDD	S		-		-
-	-	-	-	F10	-	-	R8	VSS	S		-		-
-	-	-	-	-	-	120	N13	PJ8	I/O	FT	-	TIM1_CH3N, TIM8_CH1, UART8_TX, LCD_G1, EVENTOUT	-
-	-	-	-	-	-	121	M14	PJ9	I/O	FT	-	TIM1_CH3, TIM8_CH1N, UART8_RX, LCD_G2, EVENTOUT	-

Table 8. STM32H743xI pin/ball definition (continued)

Pin/ball name								Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25						
-	-	-	-	-	-	122	L14	PJ10	I/O	FT	-	TIM1_CH2N, TIM8_CH2, SPI5_MOSI, LCD_G3, EVENTOUT	-
-	-	-	-	-	-	123	K14	PJ11	I/O	FT	-	TIM1_CH2, TIM8_CH2N, SPI5_MISO, LCD_G4, EVENTOUT	-
-	-	-	-	-	-	124	N8	VDD	S		-		-
-	-	-	-	G6	-	125	U1	VSS	S	-	-	-	-
-	-	-	-	-	-	-	N17 (2)	NC	-	-	-	-	-
-	-	-	-	-	-	-	M16 (2)	NC	-	-	-	-	-
-	-	-	-	-	-	-	M17 (2)	NC	-	-	-	-	-
-	-	-	-	-	-	-	L7	VSS	S	-	-	-	-
-	-	-	-	-	-	-	L16(2)	NC	-	-	-	-	-
-	-	-	-	-	-	-	L17(2)	NC	-	-	-	-	-
-	-	-	-	-	-	-	K16 (2)	NC	-	-	-	-	-
-	-	-	-	-	-	-	K17 (2)	NC	-	-	-	-	-
-	-	-	-	-	-	-	L8	VSS	S	-	-	-	-
-	-	-	-	-	-	126	J14	PK0	I/O	FT	-	TIM1_CH1N, TIM8_CH3, SPI5_SCK, LCD_G5, EVENTOUT	-
-	-	-	-	-	-	127	J15	PK1	I/O	FT	-	TIM1_CH1, TIM8_CH3N, SPI5_NSS, LCD_G6, EVENTOUT	-
-	-	-	-	-	-	128	H17	PK2	I/O	FT	-	TIM1_BKIN, TIM8_BKIN, TIM8_BKIN_COMP12, TIM1_BKIN_COMP12, LCD_G7, EVENTOUT	-
-	-	87	H9	L15	106	129	H16	PG2	I/O	FT_h	-	TIM8_BKIN, TIM8_BKIN_COMP12, FMC_A12, EVENTOUT	-
-	-	88	H10	K15	107	130	H15	PG3	I/O	FT_h	-	TIM8_BKIN2, TIM8_BKIN2_COMP12, FMC_A13, EVENTOUT	-
-	-	-	-	G7	-	-	-	VSS	S	-	-	-	-

Table 17. Port I alternate functions

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS	TIM1/2/16/17/LPTIM1/HRTIM1	SAI1/TIM3/4/5/12/HRTIM1	LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM	I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM/CEC	SPI1/2/3/4/5/6/CEC	SPI2/3/SAI1/3/I2C4/UART4/DFSDM	SPI2/3/6/USART1/2/3/6/UART7/SDMMC1	SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX	SAI4/FDCAN1/2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX	SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD	I2C4/UART7/SWPMI1/TIM1/8/DFSDM/SDMMC2/MDIOS/ETH	TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD	TIM1/DCMI/LCD/COMP	UART5/LCD	SYS
Port I	PI0	-	-	TIM5_CH4	-	-	SPI2_NSS/I2S2_WS	-	-	-	FDCAN1_RXFD_MODE	-	-	FMC_D24	DCMI_D13	LCD_G5	EVENT-OUT
	PI1	-	-	-	TIM8_BKIN2	-	SPI2_SCK/I2S2_CK	-	-	-	-	-	TIM8_BKIN2_COMP12	FMC_D25	DCMI_D8	LCD_G6	EVENT-OUT
	PI2	-	-	-	TIM8_CH4	-	SPI2_MISO/I2S2_SDI	-	-	-	-	-	-	FMC_D26	DCMI_D9	LCD_G7	EVENT-OUT
	PI3	-	-	-	TIM8_ETR	-	SPI2_MOSI/I2S2_SDO	-	-	-	-	-	-	FMC_D27	DCMI_D10	-	EVENT-OUT
	PI4	-	-	-	TIM8_BKIN	-	-	-	-	-	-	SAI2_MCK_A	TIM8_BKIN_COMP12	FMC_NBL2	DCMI_D5	LCD_B4	EVENT-OUT
	PI5	-	-	-	TIM8_CH1	-	-	-	-	-	-	SAI2_SCK_A	-	FMC_NBL3	DCMI_VSYNC	LCD_B5	EVENT-OUT
	PI6	-	-	-	TIM8_CH2	-	-	-	-	-	-	SAI2_SD_A	-	FMC_D28	DCMI_D6	LCD_B6	EVENT-OUT
	PI7	-	-	-	TIM8_CH3	-	-	-	-	-	-	SAI2_FS_A	-	FMC_D29	DCMI_D7	LCD_B7	EVENT-OUT
	PI8	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT-OUT
	PI9	-	-	-	-	-	-	-	-	UART4_RX	FDCAN1_RX	-	-	FMC_D30	-	LCD_VSYNC	EVENT-OUT
	PI10	-	-	-	-	-	-	-	-	-	FDCAN1_RXFD_MODE	-	ETH_MII_RX_ER	FMC_D31	-	LCD_HSYNC	EVENT-OUT
	PI11	-	-	-	-	-	-	-	-	-	LCD_G6	OTG_HS_ULPI_DIR	-	-	-	-	EVENT-OUT
	PI12	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_HSYNC	EVENT-OUT
	PI13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_VSYNC	EVENT-OUT
	PI14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_CLK	EVENT-OUT
	PI15	-	-	-	-	-	-	-	-	-	LCD_G2	-	-	-	-	LCD_R0	EVENT-OUT

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of junction temperature, supply voltage and frequencies by tests in production on 100% of the devices with an junction temperature at T_J = 25 °C and $T_J = T_{Jmax}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_J = 25 °C, V_{DD} = 3.3 V (for the 1.7 V ≤ V_{DD} ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 12*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 13*.

Figure 12. Pin loading conditions

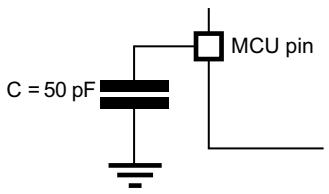


Figure 13. Pin input voltage

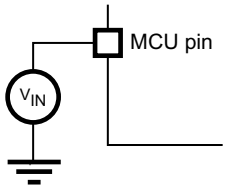


Table 21. Current characteristics

Symbols	Ratings	Max	Unit
ΣIV_{DD}	Total current into sum of all V_{DD} power lines (source)(1)	620	mA
ΣIV_{SS}	Total current out of sum of all V_{SS} ground lines (sink)(1)	620	
IV_{DD}	Maximum current into each V_{DD} power pin (source)(1)	100	
IV_{SS}	Maximum current out of each V_{SS} ground pin (sink)(1)	100	
I_{IO}	Output current sunk by any I/O and control pin	20	
$\Sigma I_{(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	140	
	Total output current sourced by sum of all I/Os and control pins(2)	140	
$I_{INJ(PIN)}$(3)(4)	Injected current on FT_xxx, TT_xx, RST and B pins except PA4, PA5	−5/+0	
	Injected current on PA4, PA5	−0/0	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/Os and control pins)(5)	±25	

1. All main power (V_{DD}, V_{DDA}, $V_{DD33USB}$) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supplies, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to *Table 20: Voltage characteristics* for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 22. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	− 65 to +150	°C
T_J	Maximum junction temperature	125	

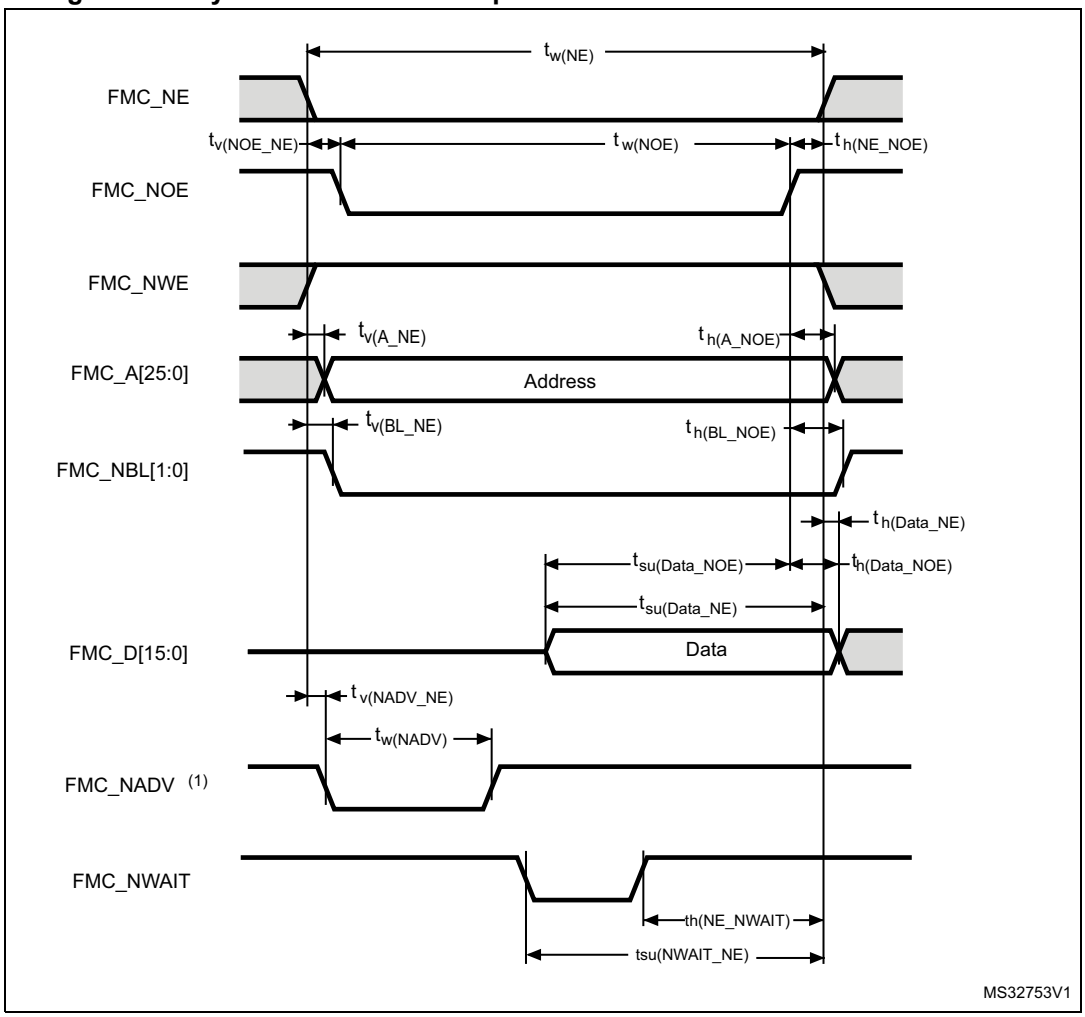
6.3.4 Embedded reset and power control block characteristics

The parameters given in *Table 26* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 23: General operating conditions*.

Table 26. Reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(1)	Reset temporization after BOR0 released	-	-	377	-	µs
V_{BOR0}	Brown-out reset threshold 0	Rising edge(1)	1.62	1.67	1.71	V
		Falling edge	1.58	1.62	1.68	
V_{BOR1}	Brown-out reset threshold 1	Rising edge	2.04	2.10	2.15	
		Falling edge	1.95	2.00	2.06	
V_{BOR2}	Brown-out reset threshold 2	Rising edge	2.34	2.41	2.47	
		Falling edge	2.25	2.31	2.37	
V_{BOR3}	Brown-out reset threshold 3	Rising edge	2.63	2.70	2.78	
		Falling edge	2.54	2.61	2.68	
V_{PVD0}	Programmable Voltage Detector threshold 0	Rising edge	1.90	1.96	2.01	
		Falling edge	1.81	1.86	1.91	
V_{PVD1}	Programmable Voltage Detector threshold 1	Rising edge	2.05	2.10	2.16	
		Falling edge	1.96	2.01	2.06	
V_{PVD2}	Programmable Voltage Detector threshold 2	Rising edge	2.19	2.26	2.32	
		Falling edge	2.10	2.15	2.21	
V_{PVD3}	Programmable Voltage Detector threshold 3	Rising edge	2.35	2.41	2.47	
		Falling edge	2.25	2.31	2.37	
V_{PVD4}	Programmable Voltage Detector threshold 4	Rising edge	2.49	2.56	2.62	
		Falling edge	2.39	2.45	2.51	
V_{PVD5}	Programmable Voltage Detector threshold 5	Rising edge	2.64	2.71	2.78	
		Falling edge	2.55	2.61	2.68	
V_{PVD6}	Programmable Voltage Detector threshold 6	Rising edge	2.78	2.86	2.94	
		Falling edge in Run mode	2.69	2.76	2.83	
$V_{hyst\_BOR\_PVD}$	Hysteresis voltage of BOR (unless BOR0) and PVD	Hysteresis in Run mode	-	100	-	mV
$I_{DD\_BOR\_PVD}$(1)	BOR(2) (unless BOR0) and PVD consumption from V_{DD}	-	-		0.630	µA

Figure 23. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms



1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

Table 72. Synchronous multiplexed NOR/PSRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$2T_{fmc\_ker\_ck} - 1$	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x=0..2)	-	1	
$t_{d(CLKH\_NExH)}$	FMC_CLK high to FMC_NEx high (x= 0…2)	$T_{fmc\_ker\_ck} + 0.5$	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	1.	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x=16…25)	-	2.5	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x=16…25)	$T_{fmc\_ker\_ck}$	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	1.5	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	$T_{fmc\_ker\_ck} - 0.5$	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	3	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0	-	
$t_{su(ADV-CLKH)}$	FMC_A/D[15:0] valid data before FMC_CLK high	2	-	
$t_{h(CLKH-ADV)}$	FMC_A/D[15:0] valid data after FMC_CLK high	1	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	2	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	2	-	

1. Guaranteed by characterization results.

Figure 28. Synchronous multiplexed PSRAM write timings

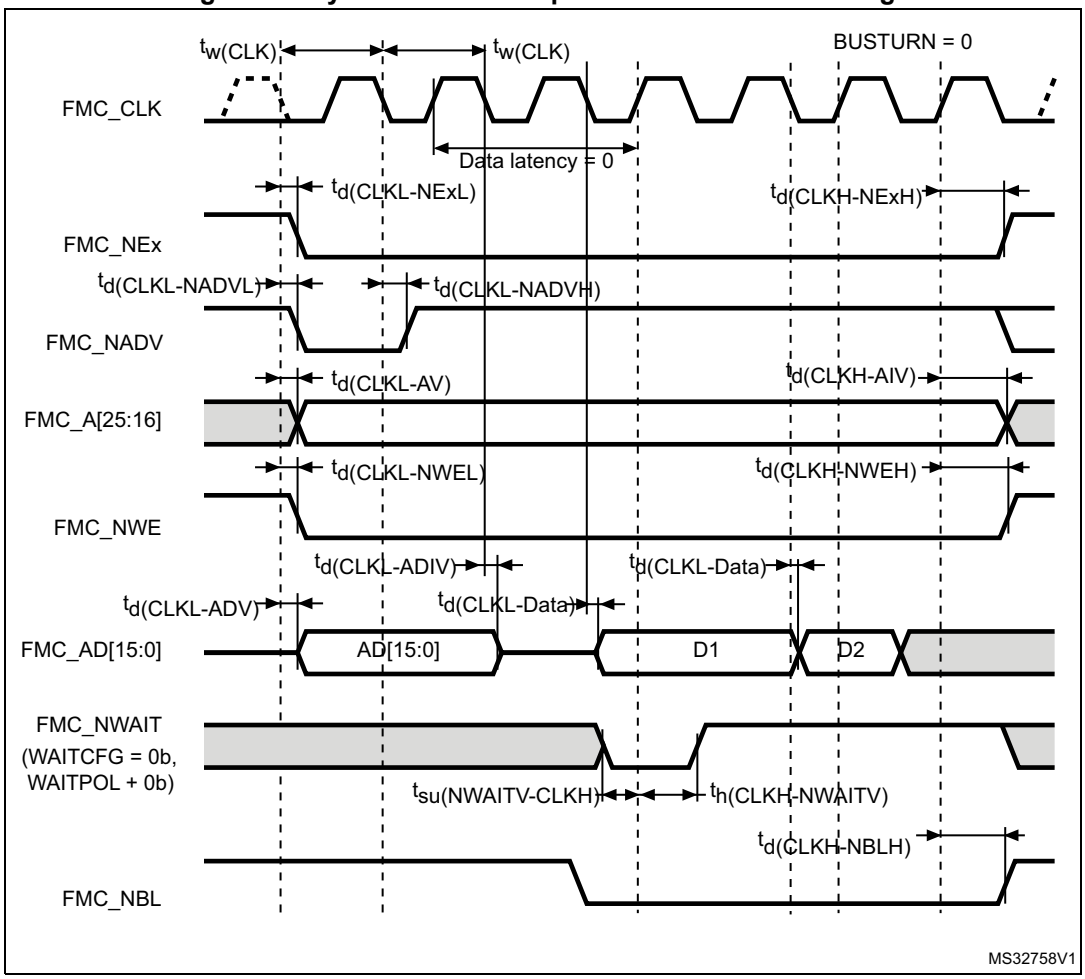


Table 80. SDRAM write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{fmc\_ker\_ck} - 1$	$2T_{fmc\_ker\_ck} + 0.5$	ns
$t_{d(SDCLKL\ \_Data)}$	Data output valid time	-	3	
$t_{h(SDCLKL\ \_Data)}$	Data output hold time	0	-	
$t_{d(SDCLKL\_Add)}$	Address valid time	-	1.5	
$t_{d(SDCLKL\_SDNWE)}$	SDNWE valid time	-	1.5	
$t_{h(SDCLKL\_SDNWE)}$	SDNWE hold time	0.5	-	
$t_{d(SDCLKL\_\ SDNE)}$	Chip select valid time	-	1.5	
$t_{h(SDCLKL\text{-}\_SDNE)}$	Chip select hold time	0.5	-	
$t_{d(SDCLKL\_SDNRAS)}$	SDNRAS valid time	-	1	
$t_{h(SDCLKL\_SDNRAS)}$	SDNRAS hold time	0.5	-	
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS valid time	-	1	
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS hold time	0.5	-	

1. Guaranteed by characterization results.

Table 81. LPSDR SDRAM write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	$2T_{fmc\_ker\_ck} - 1$	$2T_{fmc\_ker\_ck} + 0.5$	ns
$t_{d(SDCLKL\ \_Data)}$	Data output valid time	-	2.5	
$t_{h(SDCLKL\ \_Data)}$	Data output hold time	0	-	
$t_{d(SDCLKL\_Add)}$	Address valid time	-	2.5	
$t_{d(SDCLKL\text{-}SDNWE)}$	SDNWE valid time	-	2.5	
$t_{h(SDCLKL\text{-}SDNWE)}$	SDNWE hold time	0	-	
$t_{d(SDCLKL\text{-}\ SDNE)}$	Chip select valid time	-	3	
$t_{h(SDCLKL\text{-}\ SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL\text{-}SDNRAS)}$	SDNRAS valid time	-	1.5	
$t_{h(SDCLKL\text{-}SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL\text{-}SDNCAS)}$	SDNCAS valid time	-	1.5	
$t_{d(SDCLKL\text{-}SDNCAS)}$	SDNCAS hold time	0	-	

1. Guaranteed by characterization results.

6.3.27 Operational amplifiers characteristics

Table 96. OPAMP characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage Range	-	2	3.3	3.6	V
CMIR	Common Mode Input Range	-	0	-	V_{DDA}	
VI_{OFFSET}	Input offset voltage	25°C, no load on output	-	-	±1.5	mV
		All voltages and temperature, no load	-	-	±2.5	
ΔVI_{OFFSET}	Input offset voltage drift	-	-	±3.0	-	µV/°C
TRIMOFFSETP TRIMLPOFFSETP	Offset trim step at low common input voltage ($0.1*V_{DDA}$)	-	-	1.1	1.5	mV
TRIMOFFSETN TRIMLPOFFSETN	Offset trim step at high common input voltage ($0.9*V_{DDA}$)	-	-	1.1	1.5	
I_{LOAD}	Drive current	-	-	-	500	µA
I_{LOAD_PGA}	Drive current in PGA mode	-	-	-	270	
C_{LOAD}	Capacitive load	-	-	-	50	pF
CMRR	Common mode rejection ratio	-	-	80	-	dB
PSRR	Power supply rejection ratio	$C_{LOAD} \leq 50pf$ / $R_{LOAD} \geq 4\ k\Omega$(2) at 1 kHz, $V_{com}=V_{DDA}/2$	50	66	-	dB
GBW	Gain bandwidth for high supply range	-	4	7.3	12.3	MHz
SR	Slew rate (from 10% and 90% of output voltage)	Normal mode	-	3	-	V/µs
		High-speed mode	-	30	-	
AO	Open loop gain	-	59	90	129	dB
φm	Phase margin	-	-	55	-	°
GM	Gain margin	-	-	12	-	dB

Table 96. OPAMP characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
en	Voltage noise density	at 1 KHz	output loaded with 4 kΩ	-	140	-	nV/√Hz
		at 10 KHz		-	55	-	
$I_{DDA(OPAMP)}$	OPAMP consumption from V_{DDA}	Normal mode	no Load, quiescent mode, follower	-	570	1000	µA
		High-speed mode		-	610	1200	

1. Guaranteed by design, unless otherwise specified.
2. R_{LOAD} is the resistive load connected to VSSA or to VDDA.
3. R2 is the internal resistance between the OPAMP output and th OPAMP inverting input. R1 is the internal resistance between the OPAMP inverting input and ground. PGA gain = 1 + R2/R1.

Table 97. DFSDM measured timing 1.62-3.6 V(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{wh(CKIN)}$ $t_{wl(CKIN)}$	Input clock high and low time	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.62 < V_{DD} < 3.6 V	TCKIN/2 - 0.5	$T_{CKIN}/2$	-	ns
t_{su}	Data input setup time	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.62 < V_{DD} < 3.6 V	4	-	-	
t_h	Data input hold time	SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.62 < V_{DD} < 3.6 V	0.5	-	-	
$T_{Manchester}$	Manchester data period (recovered clock period)	Manchester mode (SITP[1:0]=2,3), Internal clock mode (SPICKSEL[1:0]≠0), 1.62 < V_{DD} < 3.6 V	(CKOUTDIV+1) * $T_{DFSDMCLK}$	-	(2*CKOUTDIV) * $T_{DFSDMCLK}$	

1. Guaranteed by characterization results.

USB OTG_FS characteristics

The USB interface is fully compliant with the USB specification version 2.0 and is USB-IF certified (for Full-speed device operation).

Table 109. USB OTG_FS electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{DD33USB}$	USB transceiver operating voltage	-	3.0(1)	-	3.6	V
R_{PUI}	Embedded USB_DP pull-up value during idle	-	900	1250	1600	Ω
R_{PUR}	Embedded USB_DP pull-up value during reception	-	1400	2300	3200	
Z_{DRV}	Output driver impedance(2)	Driver high and low	28	36	44	

1. The USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7 to 3.0 V voltage range.
2. No external termination series resistors are required on USB_DP (D+) and USB_DM (D-); the matching impedance is already included in the embedded driver.

USB OTG_HS characteristics

Unless otherwise specified, the parameters given in *Table 110* for ULPI are derived from tests performed under the ambient temperature, $f_{rcc\_c\_ck}$ frequency and V_{DD} supply voltage conditions summarized in *Table 23: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 20 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$.

Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output characteristics.

Table 110. Dynamic characteristics: USB ULPI(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{SC}	Control in (ULPI_DIR, ULPI_NXT) setup time	-	0.5	-	-	ns
t_{HC}	Control in (ULPI_DIR, ULPI_NXT) hold time	-	6.5	-	-	
t_{SD}	Data in setup time	-	2.5	-	-	
t_{HD}	Data in hold time	-	0	-	-	
t_{DC}/t_{DD}	Data/control output delay	2.7 V < V_{DD} < 3.6 V, C_L = 20 pF	-	6.5	8.5	
		-	-	6.5	13	
		1.7 V < V_{DD} < 3.6 V, C_L = 15 pF	-			

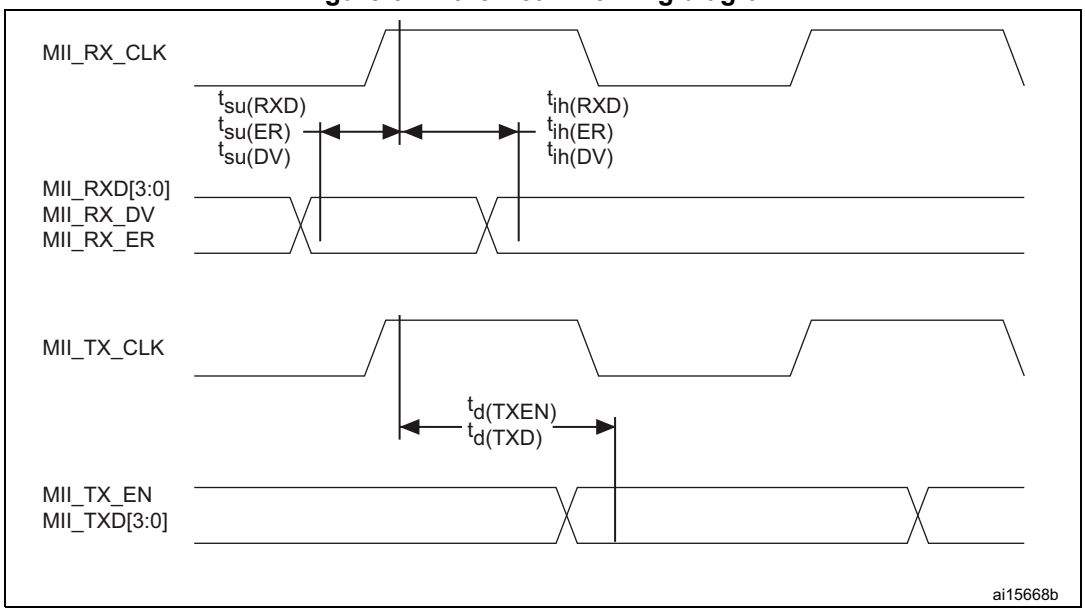
1. Guaranteed by characterization results.

Table 113. Dynamics characteristics: Ethernet MAC signals for MII(1)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	2	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	3	-	-	
$t_{su(DV)}$	Data valid setup time	1.5	-	-	
$t_{ih(DV)}$	Data valid hold time	1	-	-	
$t_{su(ER)}$	Error setup time	1.5	-	-	
$t_{ih(ER)}$	Error hold time	0.5	-	-	
$t_{d(TXEN)}$	Transmit enable valid delay time	4.5	6.5	11	
$t_{d(TXD)}$	Transmit data valid delay time	7	7.5	15	

1. Guaranteed by characterization results.

Figure 62. Ethernet MII timing diagram



6.3.33 JTAG/SWD interface characteristics

Unless otherwise specified, the parameters given in *Table 114* and *Table 115* for JTAG/SWD are derived from tests performed under the ambient temperature, $f_{rcc\_c\_ck}$ frequency and V_{DD} supply voltage summarized in *Table 23: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 0x10
- Capacitive load C=30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.15: I/O port characteristics* for more details on the input/output characteristics.

Table 114. Dynamics characteristics: JTAG characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{pp}	T_{CK} clock frequency	2.7 V <V_{DD}< 3.6 V	-	-	37	MHz
$1/t_{c(TCK)}$		1.62 V <V_{DD}< 3.6 V	-	-	27.5	
$ti_{su(TMS)}$	TMS input setup time	-	2	-	-	ns
$ti_{h(TMS)}$	TMS input hold time	-	1	-	-	
$ti_{su(TDI)}$	TDI input setup time	-	1.5	-	-	
$ti_{h(TDI)}$	TDI input hold time	-	1	-	-	
$t_{ov\ (TDO)}$	TDO output valid time	2.7 V <V_{DD}< 3.6 V	-	8	13.5	
		1.62 V <V_{DD}< 3.6 V	-	8	18	
$t_{oh(TDO)}$	TDO output hold time	-	7	-	-	

1. Guaranteed by characterization results.

Table 115. Dynamics characteristics: SWD characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{pp}	SWCLK clock frequency	2.7 V <V_{DD}< 3.6 V	-	-	71	MHz
$1/t_{c(SWCLK)}$		1.62 V <V_{DD}< 3.6 V	-	-	55.5	
$ti_{su(SWDIO)}$	SWDIO input setup time	-	2.5	-	-	ns
$ti_{h(SWDIO)}$	SWDIO input hold time	-	1	-	-	
$t_{ov\ (SWDIO)}$	SWDIO output valid time	2.7 V <V_{DD}< 3.6 V	-	8.5	14	
		1.62 V <V_{DD}< 3.6 V	-	8.5	18	
$t_{oh(SWDIO)}$	SWDIO output hold time	-	8	-	-	

1. Guaranteed by characterization results.

9 Revision history

Table 129. Document revision history

Date	Revision	Changes
22-Jun-2017	1	Initial release.
27-Sep-2017	2	Updated list of features. Changed datasheet status to “production data”. Added UFBGA169 and TFBGA100 packages and well as notes related their status on cover page and in *Table 2: STM32H743xI features and peripheral counts*. Differentiated number of GPIOs for each package in *Table 2: STM32H743xI features and peripheral counts*. Updated *Error code correction (ECC)* in *Section 3.3.2: Embedded SRAM*. Change PWR_CR3 into PWR_D3CR in *Section 3.5.1: Power supply scheme*. Updated *Section 3.12: Nested vectored interrupt controller (NVIC)*. Added ADC sampling rate values in *Section 3.17: Analog-to-digital converters (ADCs)*. Added *Table 4: DFSDM implementation* in *Section 3.23: Digital filter for sigma-delta modulators (DFSDM)* Changed PC2/3 to PC2/3_C and VDD33USB to VDD in *Figure 4: LQFP100 pinout*. Changed PC2/3 to PC2/3_C in *Figure 6: LQFP144 pinout*. Changed PC2/3 to PC2/3_C in *Figure 8: LQFP176 pinout*. Changed PC2/3 to PC2/3_C in *Figure 10: LQFP208 pinout*. *Table 8: STM32H743xI pin/ball definition*: – Modified PA7, PC4, PC5, PB1, PG1, PE7, PE8 and PE9 I/O structure – TFBGA240 +25: removed duplicate occurrence of F1, F2 and P17 pin; added notes related to F1, F2, G2 pin connection; added note on E1, L16, L17, M16, M17, K16, K17, N17. – UFBGA176+25: changed G10 pin name to VSS. – Added note to VREF+ pin. Added current consumption corresponding to 125 °C ambient temperature in *Section 6.3.6: Supply current characteristics*. Removed CRYP peripheral from *Table 38: Peripheral current consumption in Run mode*. Replaced FMC_CLK by FMC_SDCLK in *Section : SDRAM waveforms and timings*. Changed description of the last five f_S values and updated $t_{LATRINJ}$in *Table 85: ADC characteristics*. For TFBGA100, TFBGA240+25 and UFBGA169, updated thermal resistance power-junction in *Table 127: Thermal characteristics* as well as power dissipation in *Table 23: General operating conditions*.